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Robust digital voltage mode control of buck converter with enhanced tracking performance

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ABSTRACT

The digital voltage controller of power converters is used because it has many advantages over its analog counterparts. Thus, in this paper, a controller of digital voltage mode is designed and analyzed for a non-isolated DC-DC buck converter in continuous conduction mode (CCM). First, an analog controller is designed using a Bode plot to achieve the desired stability margins in the frequency domain. Next, the analog controller is discretized using bilinear transformation with the pre-warping method. The characteristics of the discretized compensator can be maintained close to the corresponding analog compensator as long as a proper sampling time is selected. The digital control scheme is simulated with a nonlinear DC-DC buck converter model in MATLAB/Simulink to investigate the controller performance. The simulation results demonstrated the validation of the proposed digital voltage-mode control design approach. The developed digital controller eliminates DC error by tracking the reference voltage, achieving a fast transient response, maintaining specified stability margins, and effectively rejecting large disturbances.

1. Introduction

Power converters are employed in many appliances such as portable communication devices [1], airborne electronics [2], grid-connected systems [3], motor speed control [4], [5], electric vehicles [6], maximum power point tracking of photovoltaic systems [7] and Internet of Think (IoT) applications [8]. Since the buck converter (BC) is subjected to variations in input and load, suitable control circuits are required to regulate the output voltage and to keep up the system's stability. The analog voltage and current-mode control (CMC) of power converters have been discussed in [9], which suits low-cost industrial applications. On the other hand, digital controllers are proposed for systems-on-chip applications due to their advantages over their analog counterparts. For instance, digitally controlled DC-DC converters are featured with programmability, flexibility, insensitivity to parameter variation, and low power consumption [10], [11]. The digital CMC of DC-DC-converter has been introduced in many literatures [12]-[15]. In [12], the adaptive slope compensation with digital-clamping-current-control is discussed and implemented through a digital signal processing (DSP) chip. The effect of slope compensation on power factor (PF) and harmonics was studied using an interleaved buck converter for different input voltage and load conditions. The proposed controller achieves PF correction, reduced harmonics, and increased efficiency under all conditions. In [13], a two-loop digital architecture of an average CMC buck converter is introduced, which is realized through a hardware description language.

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Nomenclature:

d	small signal duty cycle
D	D duty-cycle
d_T , $\bar{d}_T$	time intervals at which the switch (S) is ON and OFF
f_c	crossover frequency
i_l	small signal inductor current
i_o	small signal load current
r	load resistor
r_C	equivalent-series-resistances of capacitor
r_{DS}	on resistance of the switch
r_F	forward-resistance of the diode
r_L	equivalent-series-resistances of inductor
$T(s)$	compensated-loop gain
$T_c(z)$	digital compensator
T_{CS}	closed-loop compensated system
T_k	loop gain
T_m	Pulse width modulator transfer function
T_p	transfer function
T_S	sampling time
v_C	capacitor-voltage
V_F	offset-voltage of the diode
v_i	small signal ac input voltage
v_I	input-voltage
v_o	small signal ac output voltage
v_O	output-voltage
V_r	reference voltage
V_{Tm}	ramp voltage of PWM
w_m	frequency at the required phase boost
w_0	frequency of the analogue compensator
w_{pc}, w_{zc}	pole and zero of the analogue compensator

Greek symbols

β	output voltage sensor gain
ϕ_m	phase boost
ϕ_{T_k}	phase of the loop-gain

Abbreviation

BC	buck converter
C	capacitor
D1	diode
CMC	current-mode control
DPWM	digital pulse width modulation
DSP	digital signal processing
DVMC	digital voltage-mode controller
FPGA	field programmable gate array (FPGA)
IoT	Internet of Think (IoT)
L	inductor (L)
PF	power factor
PO	peak overshoot
PU	peak undershoot
RPPM	random pulse position modulation
S	MOSFET
ZOH	zero-order-hold

The new controller gives the benefit of precise regulation of the output voltage as the load increases and decreases. In [14], a parallel digital CMC algorithm for BC was implemented on a field programmable gate array (FPGA). The system results in fast voltage regulation at different values of input voltage and load states. In [15], predictive control of digital average voltage and digital average current has been implemented with BC through a DSP chip. The proposed system has many benefits such as more voltage regulation, a wide stable range, fast load transient response, and overcurrent protection. Alternatively, a digital voltage-mode controller (DVMC) has been suggested for DC-DC converters, in which only the sensed output voltage is required for the feedback loop. In ref. [16], the digital PID compensator of the buck-boost converter was implemented using duty-locking control through an FPGA implementation. The results show that the method increases efficiency and provides stable and reliable output voltage in all transition regions. While in ref. [17] introduced enhanced duty-cycle-overlap control of buck-boost converter to overcome unstable output voltage that occurs when transitioning from buck to boost mode. In ref. [18], random pulse position modulation (RPPM) scheme is combined with digital pulse width modulation (DPWM) for a buck converter. The proposed controller is implemented in FPGA. Experimental results show that the proposed controller can achieve low steady-state conduction noise and fast response at load transients. Other research efforts proposed the digital PI compensator with FPGA implementation using a voltage-mode digital pulse skipping modulator to improve the efficiency and stability of a prototype buck converter [19]. In [20] a multi-mode controller including digital PWM and pulse frequency modulation (PFM) technology is used for buck and boost converter. The proposed system was implemented using an FPGA device to achieve stable behavior and increase efficiency. An alternative implementation of the DVCM voltage-mode controller for a fourth-order buck converter is introduced in [21] using a dsPIC30F6010 microcontroller. The controller offers good dynamic performance and keeps a steady-state ripple current within the limits. Ref. [22] gives the VMC of a buck converter based on the sliding mode control scheme. The system is implemented in Matlab/Simulink. and tested under different input voltages and loads. The system exposed good performance under all conditions. The previous endeavors have discussed stability analysis, implementation aspects, and control system performance. However, the digital compensator design approach has not been reported in detail. Motivated by the research efforts, a DVMC system is developed for a buck converter to improve relative stability and enhance tracking performance. The s-domain digital compensator is designed according to [23] and digitized using bilinear transformation with a pre-warping method [24], which guarantees the system stability and eliminates the frequency response distortion. The digital compensator is simulated with a nonlinear BC model using MATLAB/SIMULINK to investigate the tracking performance, characteristics of rapid response, and relative stability of the digital control system. This article is arranged as follows: Section 2 discusses the modeling of BC. Section 3 gives the design of a digital compensator. Section 4 presents the simulation results and section 5 presents conclusions.

2. Modeling of DC-DC BC

Figure 1 depicts a BC circuit that includes a capacitor (C), an inductor (L), a MOSFET (S), a diode (D1), and a load resistor (r) [25]. Two averaged models are explained in the following subsections.

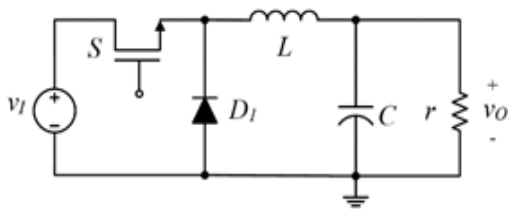


Figure 1. BC circuit

2.1. Large-signal average circuit

Figure 2 illustrates the large-signal averaged circuit of the BC in CCM. The circuit of the converter can be derived using Kirchhoff's laws [26], which leads to:

$$\left.\begin{aligned}\frac{dv_C}{dt}&=\frac{1}{C}[i_L-i_O],\\ \frac{di_L}{dt}&=\frac{1}{L}\left[(V_I-r_{DS}i_L)d_T+(V_F-r_Fi_L)\bar{d}_T-r_Li_L-v_O\right]\end{aligned}\right\} \quad (1)$$

$$v_O=v_C+r_C\times(i_L-i_O) \quad (2)$$

where v_C is a capacitor voltage, i_L is an inductor-current, i_O is the load-current, v_I is the input-voltage, r_{DS} is the on-resistance of the switch, r_F and V_F are forward-resistance and offset-voltage of the diode, r_L, and r_C are the equivalent-series-resistances of inductor and capacitor respectively, and v_O is the output-voltage. The time intervals at which the switch (S) is ON and OFF are d_T and $\bar{d}_T$, respectively, where $d_T \in [0, 1]$.

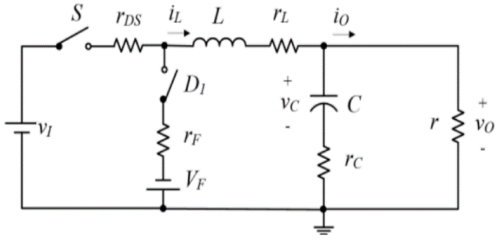


Figure 2. Large-signal circuit of BC

2.2. Small-signal average circuit

Figure 3 shows a small signal BC circuit [3]. The symbols R and D stand for load-resistor and duty-cycle, respectively. Small-signal ac values for input voltage, output voltage, duty cycle, inductor current, and load current are specified as v_i, v_o, d, i_l, and i_o, respectively. The equivalence resistance (r_{eq}) in the inductor branch is equal to:

$$r_{eq}=Dr_{DS}+r_F(1-D)+r_L \quad (3)$$

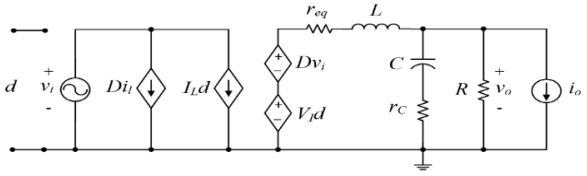


Figure 3. Small-signal circuit of BC.

According to [23], the transfer function (T_p) is derived from Fig. 3, which gives:

$$T_p(s)=\frac{v_o(s)}{d(s)}=\frac{V_fRr_C}{L(R+r_C)}\frac{s+\frac{1}{Cr_C}}{s^2+s\left(\frac{C(Rr_C+Rr_{eq}+r_Cr_{eq})+L}{LC(R+r_C)}\right)+\frac{R+r_{eq}}{LC(R+r_C)}} \quad (4)$$

The transfer function in (4), represents the linearized buck model that is utilized to design a voltage-mode compensator.

3. DVMC Design

3.1. Compensator design in s-domain

The pulse-width modulator transfer function (T_m) and output voltage sensor gain (β) are given by [23]:

$$\left.\begin{aligned}T_m&=\frac{1}{V_{Tm}}\\ \beta&=\frac{V_r}{V_o}\end{aligned}\right\} \quad (5)$$

where V_{Tm} is ramp voltage of PWM and V_r is the reference voltage. The loop gain (T_k) of a BC controlled in voltage mode without a compensator is:

$$T_k=\beta T_mT_p \quad (6)$$

Since the loop gain at low frequencies is 0 dB, a compensator is required to increase the DC gain and maintain sufficient stability margins. If the magnitude of T_k at the desired crossover frequency (f_c) is obtained from Fig.3 in dB, then the magnitude of $T_k(f_c)$ can be computed as:

$$|T_k(f_c)|=10^{T_k(f_c)dB/20} \quad (7)$$

The required phase boost (ϕ_m) that achieves the desired phase margin (PM) is determined according to the following equation:

$$\emptyset_m=PM-\emptyset_{Tk}(f_c)-90^o \quad (8)$$

where, $\phi_{T_k}(f_c)$ is the phase of the loop-gain T_k at f_c.
Next, the factor K is determined by:

$$K=\tan\left(\frac{\phi_m}{4}+45°\right) \quad (9)$$

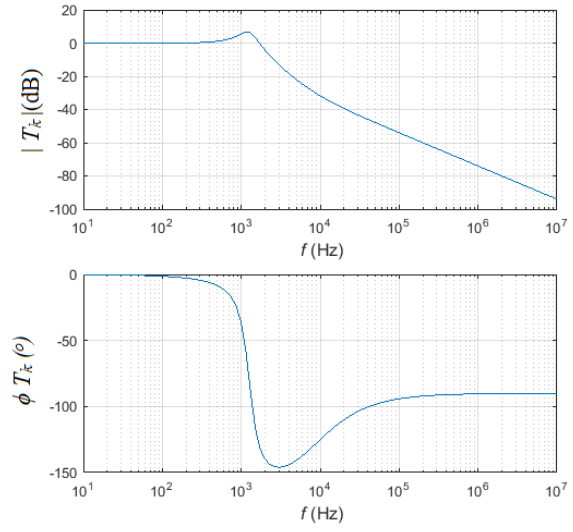


Figure 4. Bode-plot of the uncompensated loop-gain T_k

From which the pole w_{pc} and zero w_{zc} of the analogy compensator are computed:

$$\left.\begin{aligned}\omega_{zc}&=\frac{\omega_m}{K}\\ \omega_{pc}&=K\omega_m\end{aligned}\right\} \tag{10}$$

where, ω_m is the frequency at the required phase boost (ϕ_m). Hence, the transfer function of the analog compensator is:

$$T_c(s)=\frac{K\omega_c}{|T_k(f_c)|}\frac{(s+\omega_{zc})}{s(s+\omega_{pc})} \tag{11}$$

Fig. 4 gives the Bode-plot of T_k , while Fig. 5 shows the Bode-plot of the compensator $T_c(s)$.

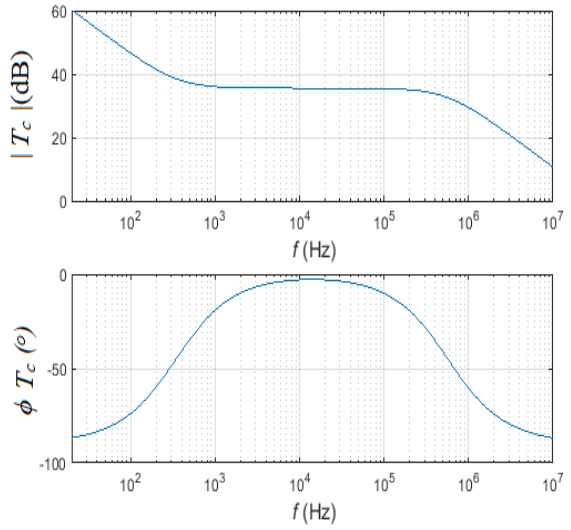


Figure 5. Bode plot of the analogy compensator $T_C(s)$

3.2. Transformation to digital compensator

The analogy compensator in (11) can be mapped onto a digital compensator $T_c(z)$ using the bilinear transformation with the pre-warping method [24], which is given by:

$$T_c(z)=T_c(s)\big|_{s=c\left[\frac{z-1}{z+1}\right]} \tag{12}$$

The parameter c is defined as

$$c=\frac{\omega_o}{\tan\left(\frac{\omega_o T_s}{2}\right)} \tag{13}$$

where T_s is the sampling time and ω_o is the 3dB frequency of the analogy compensator. The T_s is chosen based on the system bandwidth such that

$$T_s\leq\frac{1}{10f_b} \tag{14}$$

4. Results and discussions

4.1. The digital control design and relative stability

The analog compensator is considered for a typical BC with circuit features specified in Table 1 to achieve zero DC error and a phase margin greater than 45°.

Table 1. BC parameters [23].

Description	Variable	Value
Inductance	L	301 µH
Capacitance	C	51.2 µF
Load Resistance	R	(10 - 100) Ω
Inductor ESR	rL	0.050 Ω
Capacitor ESR	rC	0.391 Ω
MOSFET On-Resistance	rDS	0.180 Ω
Diode Forward Resistance	rF	0.022 Ω
Diode Threshold Voltage	VF	0.700 V
Input Voltage	VI	28 V
Output Voltage	VO	14 V
Switching Frequency	fs	100 kHz

The feedback network gain (β) and ramp voltage (V_{Tm}) are set to 0.3571 and 10 V respectively. The frequencies f_c and f_m are assumed to be 14 kHz. The analogy compensator is designed as illustrated in section 3, yielding.

$$T_c(\mathrm{s})=2.147\times10^8\frac{(s+2159)}{s(s+3.583\times10^6)} \tag{15}$$

Figure 6 displays the Bode-plot of the compensated-loop gain T(s). The phase margin is 59.8° as can be seen. Figure 7 gives the system bandwidth as determined by the Bode-plot of the closed-loop compensated system (T_{CS}) which is approximately 19 kHz. The analog compensator in (15) can be translated to the z-domain if the sampling time (T_s) is set to 2 μs in accordance with (14), which gives the proposed digital compensator

$$T_c(\mathrm{z})=46.934\frac{(z-0.9957)(z+1)}{(z-1)(z+0.5636)} \tag{16}$$

The zero-order-hold (ZOH) transfer function and adjusted loop gain can be transformed to the z-domain to obtain,

$$T(z)=0.12276\frac{(z+1)(z-0.9957)(z-0.9049)}{(z-1)(z+0.5636)(z^2-1.992z+0.9927)} \tag{17}$$

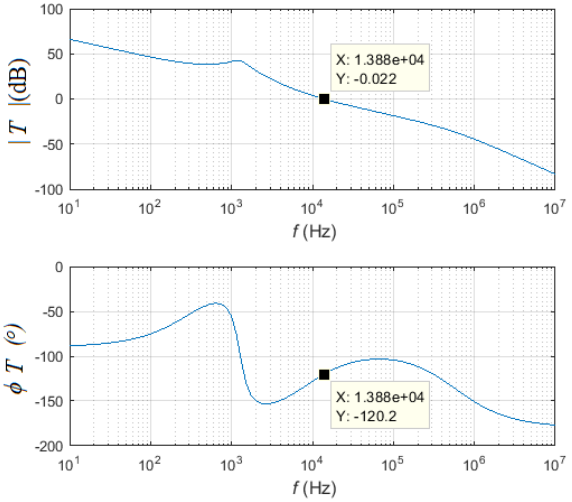


Figure 6. Bode-plot of the T(s).

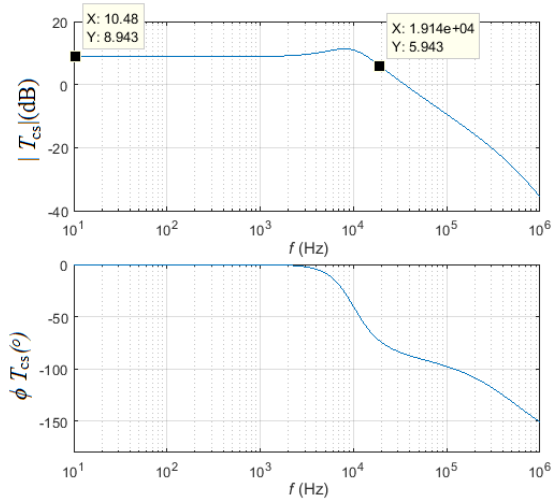
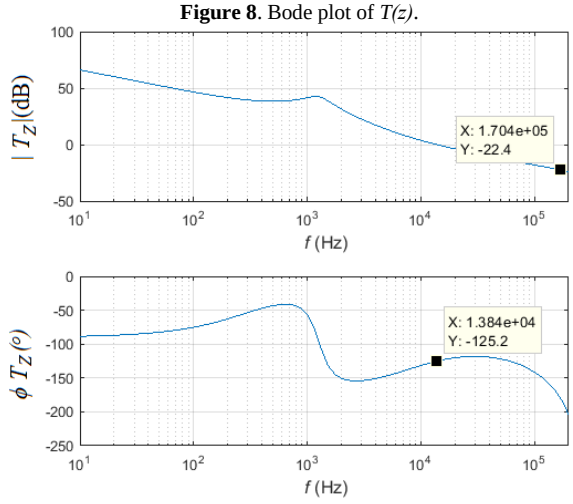


Figure 7. Bode-plot of (T_{CS}).

The Bode-plot of the digital compensated-loop gain $T(z)$ is given in Fig. 8, from which the gain and phase margins are 22.4 dB and 54.8°, respectively. Obviously, the phase margin of the digital control system is slightly degraded owing to the sampling effect. Therefore, it is recommended to overdesign the stability margins of the analogy compensator to maintain the desired relative stability in the digitized compensator.

Figure 8. Bode plot of *T(z)*.



4.2. Steady-state performance

The digital controller used voltage mode with BC is simulated in MATLAB as shown in Fig. 9. The A/D converter subsystem, which has a 10-bit resolution over a 2 V range, consists of a transport delay, a ZOH, a saturation block, and a quantizer. The transport delay block has a 2 μs time delay, whereas the saturation block has maximum and minimum bounds of +1 and -1, respectively. The quantization interval is 1/512, while the ZOH sampling time is 2 μs. The DPWM subsystem has a 10-bit resolution over the 1V range, which contains a quantizer with a quantization interval of 1/1024 and a saturation block with 9.9 and 0.1 saturation limits. The BC model given in Equations (1) and (2) is coded using MATLAB s-function.

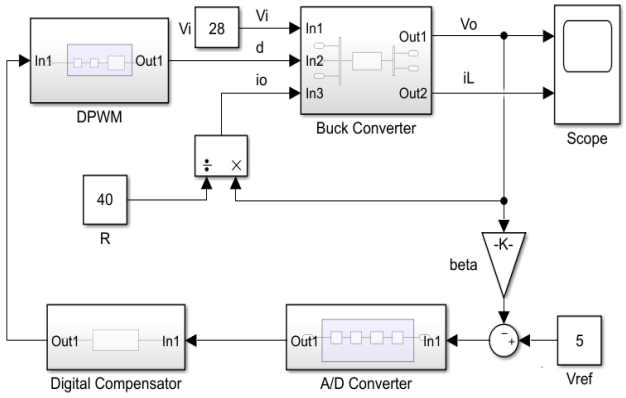


Figure 9. MATLAB/SIMULINK model of DVMC buck converter in CCM.

The simulation is performed using an *Automatic* solver with *Variable* step size. Figure 10 represents the steady-state waveforms of a control voltage (V_{GS}), V_O, and i_L at steady-state. It can be noticed that the converter runs in CCM during the nominal operating condition (V_I = 28 V and R = 40 Ω), where the DC value of the output voltage is 14 V and the duty cycle is 0.5.

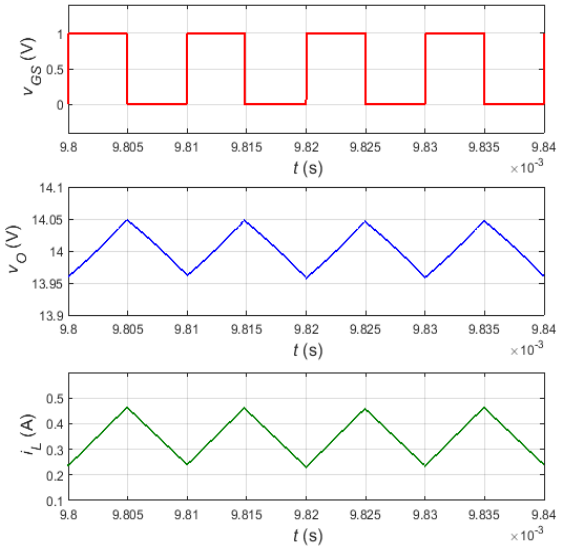


Figure 10. Control pulses, *Vo*, and i_L at steady-state conditions.

4.3. Tracking action and disturbance rejection

The tracking action of the digital control system has been inspected considering the variations in V_I and i_O. Figs. 11 and 12 show the V_O response when the V_I changes abruptly at t = 10ms. If the V_I fluctuations from 28V to 23V as shown in Fig. 11, the peak undershoot (PU) is 120 mV and the settling time (ts) is 600 µs. However, when the V_I rises step by step from 28 V to 34 V, as given in Fig. 12, the peak-overshoot (PO) is about 120 mV and ts is 600µs. Additionally, the figures show the tracking performance of the DVMC system during an abrupt change in load current at t = 10 ms.

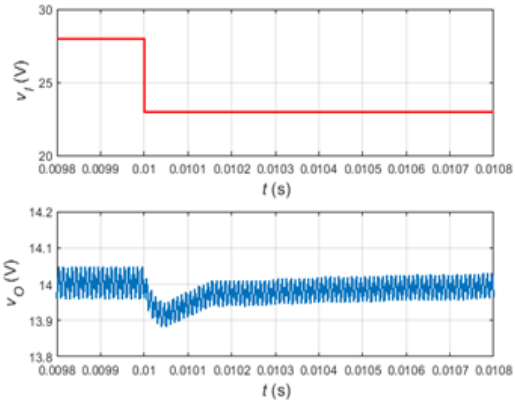


Figure 11. BC response due to a sudden decrease in V

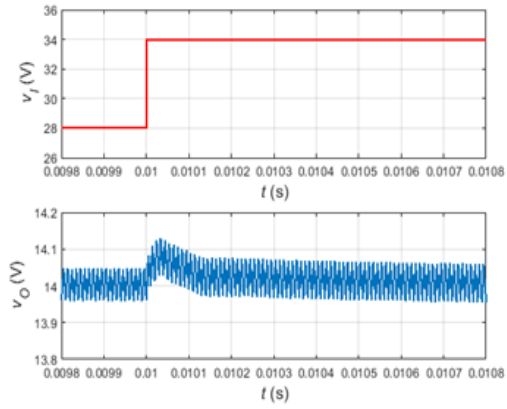


Figure 12. BC response due to a sudden increase in V_I

As depicted in Fig. 13, if the i_O decreases from 0.350 A to 0.175 A, PO and ts are about 100 mV and 100 µs, respectively. In Fig. 14, however, the i_O changes from 0.350 A to 0.70 resulting in PU and ts of 150 mV and 100 µs, respectively. Notably, the digital compensator rejects the line and load instabilities and maintains excellent temporary response. Furthermore, the V_O is well-regulated in the presence of the line and load disturbances. It is evident that the digital compensator eliminates the steady-state error and increases the stability margins. The bandwidth of the closed-loop system is improved, which results in a fast system response.

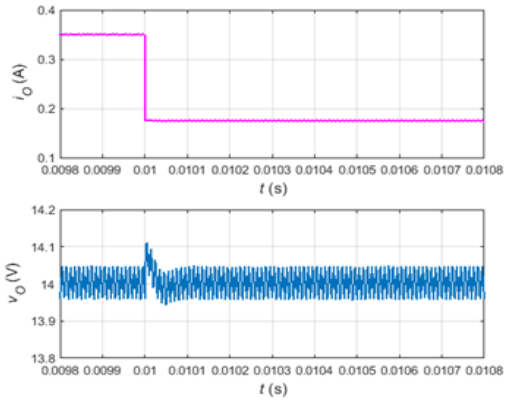


Figure 13. BC response due to sudden decrease in i_O

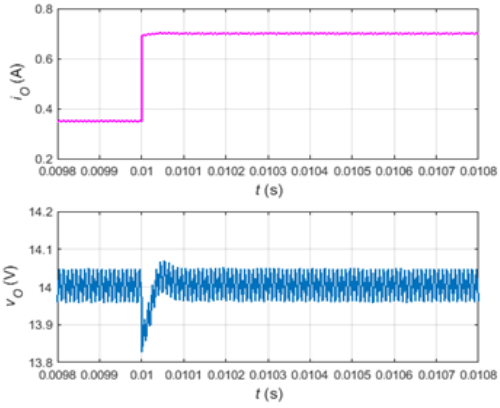


Figure 14. BC response due to sudden increase in i_O.

Table 2 shows a brief comparison between the digital control proposed in this study and what was presented in previous studies.

Table 2. Comparison digital control scheme proposed in this work with previous studies

Reference No.	[13]	[14]	[15]	[22]	This work
Control type	digital average CMC	parallel digital CMC	Digital average VMC and CMC	sliding mode control	digital VMC
Type of converter	buck converter	buck converter	buck converter	buck converter	buck converter
Input voltage	12 V	5 V	5 V	300-400 V	(34 -23) V
Output voltage	1.5 V	2.5 V	1.5 V	150-350 V	14 V
Switching frequency	1.25 MHz	400 kHz	50 kHz	10 kHz	100 kHz
settling time (step change in load)	15 µs Decrease load	105 µs decrease load	700 µs decrease load	-	100 µs decrease load
	14 µs Increase load	100 µs Increase load	600 µs Increase load	0.89 ms Increase load	100 µs Increase load
Voltage overshoot and undershoot (step change in load)	40 mV undershoot	110 mV undershoot	101 mv undershoot	-	150 mV undershoot
	40 mV overshoot	120 mV overshoot	83 mv overshoot	340 mV overshoot	100 mV overshoot
settling time (step change in input voltage)	-	-	-	1.3 ms decrease input	600 µs decrease input
	-	-	-	-	600µs increase input
Voltage overshoot and undershoot (step change in input voltage)	-	-	-	135 mV undershoot	120 mV undershoot
	-	-	-	—	120 mV overshoot

5. Conclusions

A controller of a DC-DC buck converter by DVMC has been designed, analyzed, and simulated by MATLAB-SIMULINK. The proposed compensator has been designed in the s-domain using Bode plots and

transformed to the z-domain using bilinear transformation with the pre-warping method. The characteristics of the discretized compensator can be maintained close to those of the corresponding analog compensator as long as a proper sampling time is selected. The results validated the proposed digital control approach. Furthermore, the digital control system has been applied to a nonlinear model buck converter and tested with line and load disturbances. It is apparent that the digital compensator eliminates the DC error, maintains a fast transient response, and achieves the desired stability margins. The proposed digital control technique is simple and applicable to other types of DC-DC converters.

Authors' contribution

All authors contributed equally to the preparation of this article.

Declaration of competing interest

The authors declare no conflicts of interest.

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This study didn't receive any specific funds.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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