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Technical Research

DESIGN AND SIMULATION OF HIGH GAIN SEPIC DC–DC CONVERTER

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Abstract: This paper proposes a new model of converter, single-ended primary-inductor converter (SEPIC) type with a high gain voltage for clean energy sources. The suggested model is established by combining the traditional SEPIC DC-DC converter with two different circuits. The first circuit is a split- inductor circuit which is made of three diodes and two inductors, while the second circuit consists of two capacitors and two diodes. The suggested SEPIC DC-DC converter achieves a high voltage gain of 7.5 times the supply voltage when the duty cycle value is kept at 0.5 with only a unique controlled switch. The gain of the proposed converter is greatly increased while the ripple of output voltage and the input current is decreased for higher values of the duty cycle. In addition, the decreased value of input current ripple results in limited switching stress. The suggested converter is analyzed in detail for continuous conduction mode (CCM). A MATLAB/ Simulink program is used to confirm the analysis of the suggested converter.

Keywords: *SEPIC; high static gain; voltage stress; ripples; DC-DC converter*

1. Introduction

In the last decade, the use of existing fossil fuels has increased dramatically, contributing to air pollution and rising the expense of the equipment [1]. As a consequence of these issues, the researchers turned their attention to other alternatives such as photovoltaic (PV), fuel cells, wind turbines, and other Renewable Energy Resources (RES). These resources have a range of benefits, as they are environmentally friendly and being readily available. They gained more attraction and became noticeable. The voltage produced by the RES modules, however, is relatively low and depends on the environmental conditions [2]. Therefore, series and parallel system of the PV module may be a way to satisfy the load requirements in order to increase the PV voltage, resulting in lower performance, high cost, and large device size [3], [4]. To achieve a high voltage gain while maintaining decent performance, certain non-coupled SEPIC converters were developed. They can all be used at maximum duty ratio for high voltage applications, but this reduces efficiency and impacts the converter functionality [5], [6]. Various methods for voltage boosting, such as coupled inductor [7]–[9] have been implemented with a non-isolated converter, to obtain high levels of output dc voltage. The output is regulated in the coupled inductor-based converter by changing the inductor coil turn ratio. The coupled inductor leakage inductance has negative effects, where it generates a switch current spike, and thus requires a clamping system to prevent the current from spiking [10]. Therefore, to get a high voltage gain, the isolated converter is used [11]–[16]. However, due to high-frequency transformer losses, the converter efficiency decreases. Weight and size, on other

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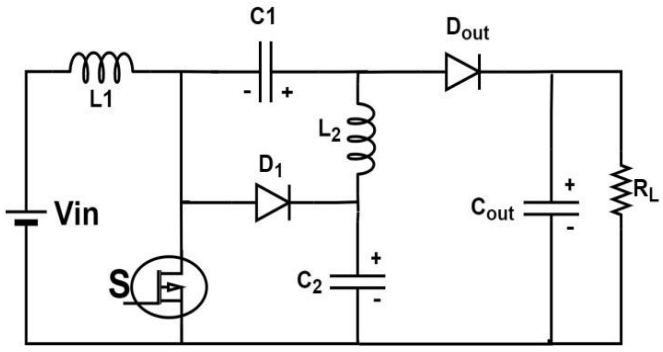
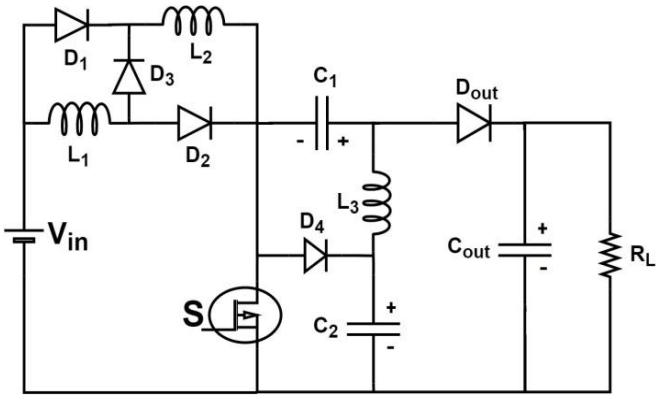
hand, are other main concerns with isolated DC-DC converter. To get a high gain and also overcome the constraints of the conventional SEPIC converter, a new model of SEPIC topology converter is suggested [17]. The proposed topology shows a high switching loss, low level of static gain, and high supply current ripples. An updated SEPIC converter based on a hybrid spilt-inductor in order to get a high gain is presented in [18]. The presented converter shows good regulation. The gain value of this converter never exceeds more than four times at a mid-value of the duty ratio in spite of many components are used. The reference [19] presents an isolated single ended primary inductor converter, and [20] shows inductors coupled converters based on SEPIC converters, the majority of which suffer from voltage stress on control switch due to the leakage inductance problem. Hence, there is a need to develop a step-up DC-DC power conversion system to get a high gain value of output voltage and meet the requirement of an emerging power supply system, so the aim of this paper is to design a new converter structure that combines two different boost circuits. The first part is **a** split-inductor, and the second part is switched capacitor. The new method of SEPIC converter achieves high gain 7.5 times higher than input voltage at mid-value of duty ratio along with preserving low ripples of input current and reducing switching losses. Additionally, due to low switching losses and low supply current ripples, the stress on switch S and output voltage ripples are greatly reduced. As a consequence, the proposed SEPIC DC-DC converter can efficiently be utilized for applications of renewable energy sources.

2. The Proposed SEPIC Converter

In this paper, a non-isolated converter SEPIC type with a single switch is implemented for high voltage applications. The proposed converter is derived by adding, to modified SEPIC converter shown in fig. 1(a), two separate boosting circuits as shown in fig. 1(c). These circuits are a split-inductor circuit which is made of three diodes and two inductors, and a switched capacitor circuit which is made of two diodes and two capacitors. The main characteristics of the suggested converter are; 1) working with a single switch which decreases the control circuitry's complexity, 2) high voltage gain, 3) continuous input current, and 4) overall input source utilization.



(a)



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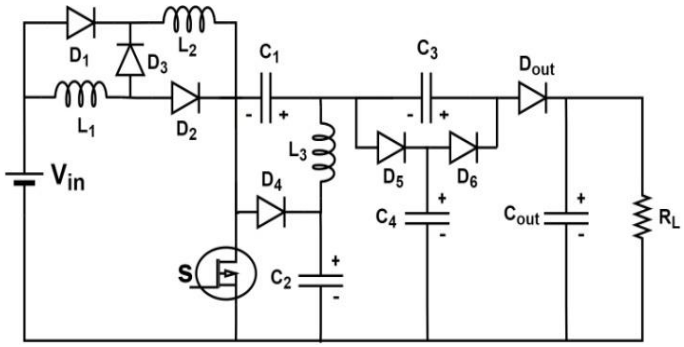


(c)

Figure 1. (a) Modified SEPIC converter [6], (b) Modified SEPIC converter [18] and (c) The proposed SEPIC converter

The operating principle in continuous conduction mode of the suggested converter is presented as follows:

2.1. Continuous Conduction Mode Analysis

Some assumptions are to be considered in order to describe the steady-state operation as capacitors must be large enough to sustain a constant voltage and all components should be ideal. The suggested converter is operated with a single switch S, so the converter operates in two separate modes, mode-I and mode-II as shown in fig. 2(a) and (b), respectively.

Mode-1:

When the switch S is switched ON, the inductors, L_1 and L_2 are connected by forward-biased diodes D_1 and D_2 to the source voltage in parallel. At the same time, C_2 and C_4 capacitors are discharged, while C_1 is charged by inductor L_3 and C_3 is charged by capacitor C_4. The load is powered by the output capacitor (C_{out}) and diodes D_3, D_4, D_5 and D_O are reverse biased as presented in fig. 2(a).

During the switch in ON state, the voltage across L_1, L_2, and L_3 are represented as

$$V_{L1} = V_{L2} = V_L = V_{in} \quad (1)$$

$$V_{L3} = V_{C2} - V_{C1} \quad (2)$$

$$V_{L3} = V_{C2} + V_{C3} - V_{C4} \quad (3)$$

Where V_{in} is the input voltage, V_{L1}, V_{L2}, and V_{L3} are the voltages across L_1, L_2, and L_3, respectively. V_{C1}, V_{C2}, V_{C3}, and V_{C4} are the voltages across C_1, C_2, C_3, and C_4, respectively.

Mode-II:

When the switch is switched OFF, in this case, both inductors L_1 and L_2 are connected in series by forward-biased diode D_3 as shown in fig. 2(b). In this mode, the inductors L_1, L_2, and L_3 are discharging linearity, also capacitors C_1 and C_3, are discharging the energy to the C_{out} and load. Diodes D_1, D_2, and D_6 are reverse biased.

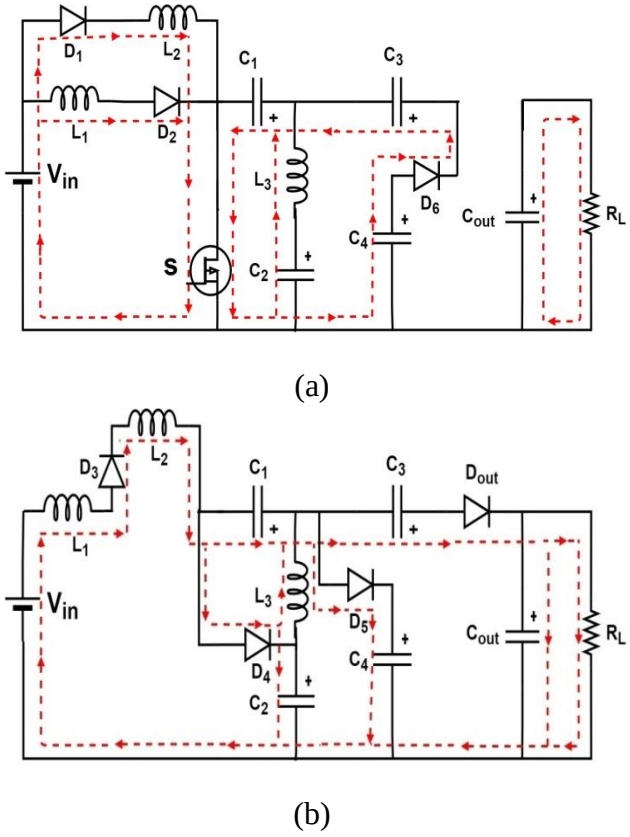


Figure 2. Circuit diagram of the proposed converter when (a) Switch S is turned ON and (b) Switch S is turned OFF

Table 1. Diodes status of the proposed SEPIC converter

Diodes	Switch ON	Switch OFF
D_1	ON	OFF
D_2	ON	OFF
D_3	OFF	ON
D_4	OFF	ON
D_5	OFF	ON
D_6	ON	OFF
D_{OUT}	OFF	ON

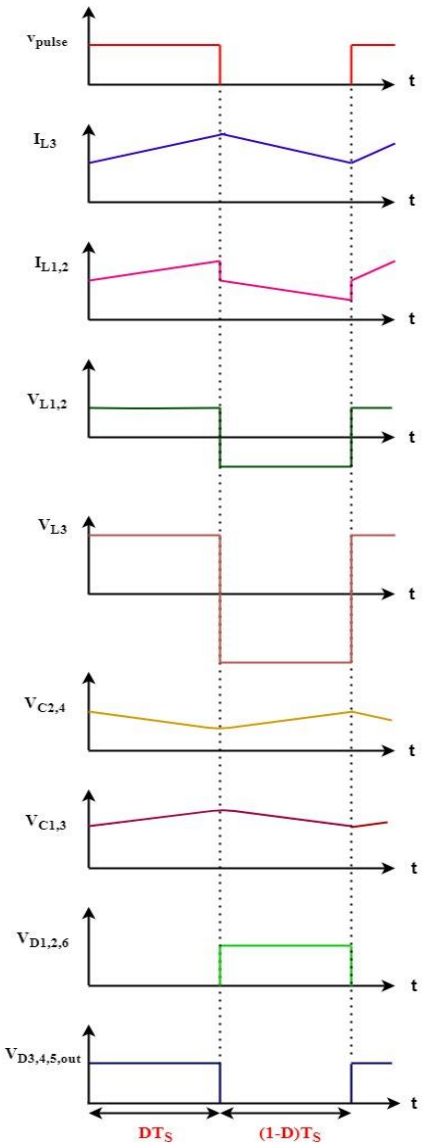


Figure 3. Theoretical waveforms of the proposed converter

During the switch in OFF state, the voltage across L_1, L_2, and L_3 are represented as

$$V_{L1} = V_{L2} = V_L = \frac{1}{2}(V_{in} - V_{C2}) \quad (4)$$

$$V_{L3} = -V_{C1} \quad (5)$$

$$V_{L3} = V_{C2} - V_{C4} \quad (6)$$

The voltage gain of the proposed converter and capacitors voltage can be determined using the Inductor Volt Second Balance (IVSB) theory for L_1, L_2, and L_3 inductors,

$$DV_{L(ON)} + (1-D)V_{L(OFF)} = 0 \quad (7)$$

Where D is the duty ratio and define as

$$D = \frac{T_{on}}{T} \quad (8)$$

$$V_{C1} = \frac{(1+D)D}{(1-D)}V_{in} \quad (9)$$

$$V_{C2} = V_S = \frac{(1+D)}{(1-D)}V_{in} \quad (10)$$

$$V_{C3} = \frac{(1+D)}{(1-D)}V_{in} \quad (11)$$

$$V_{C4} = \frac{(1+D)^2}{(1-D)}V_{in} \quad (12)$$

When the switch S in OFF state

$$V_O = V_{C3} + V_{C4} \quad (13)$$

$$\frac{V_O}{V_{in}} = \frac{(2+D)(1+D)}{(1-D)} = \frac{I_{in}}{I_O} \quad (14)$$

Equation (14) represents the voltage gain of the suggested SEPIC converter in continuous conduction mode.

Fig. 4 shows the comparison between the proposed converter's voltage-transfer gains with the modified SEPIC converter shown in fig. 1(a) and the converter shown in fig. 1(b). The figure indicates that the proposed converter's voltage transfer gain is greater than others converters. And it is shown that the gain of the modified converter is the lowest one in the range of duty cycle between 0.1 and 0.9.

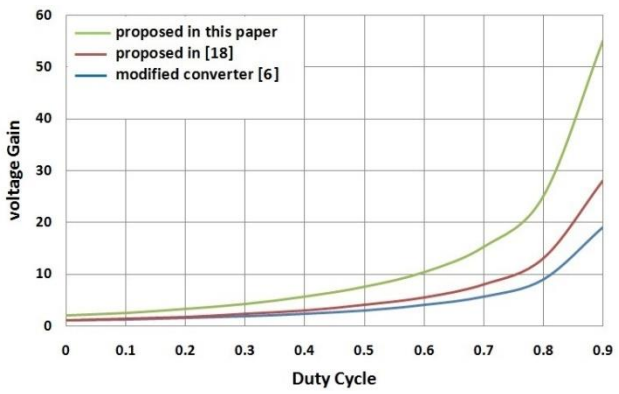


Figure 4. Variation of voltage gain with duty cycle

Table 2. Comparison between the suggested converter and other converters according to voltage gain

Topologies	voltage gain	duty cycle	gain times
Classical SEPIC converter	$\frac{D}{1-D}$	0.5	1
[5]	$\frac{3D}{1-D}$	0.5	3
[6]	$\frac{1+D}{1-D}$	0.5	3
[9]	$\frac{3-D}{1-D}$	0.5	5
[18]	$\frac{1+2D}{1-D}$	0.5	4
Proposed SEPIC converter	$\frac{(2+D)(1+D)}{(1-D)}$	0.5	7.5

2.2. Voltage Stress of the Switch S

From fig. 1(c), the voltage stress on switch is equal to the voltage across C_2 as derived in equation (10). Comparison according to stress on the switch S between the suggested SEPIC converter and the converter proposed in [5], modified SEPIC converter proposed in [6], converter proposed in [18], and classical SEPIC converter is shown in table 3. According to table 3, the voltage stress on the switch S for the implemented converter is the lowest. Despite the fact that the suggested converter has a greater number of components than other converters, it has advantages over other converters, such as low switch voltage stress, high voltage gain, and the use of a single switch.

Table 3. Comparison according to voltage stress on the switch between the suggested converter and other converters

Case	Proposed	[5]	[6]	[18]	SEPIC
Switches number	1	1	1	1	1
Diodes number	7	3	2	5	1
Inductors number	3	4	2	3	2
Capacitors number	5	6	3	3	2
Switch stress	$\frac{V_O}{2+D}$	$\frac{V_O}{3D}$	$\frac{V_O}{1+D}$	$\frac{(1+D)V_O}{1+2D}$	$\frac{V_O}{D}$

2.3 Design Consideration of Inductors

Inductor selection depends on duty cycle value, resistive load, and switching frequency [4]. The ripples current, maximum and minimum currents across L_1, L_2, and L_3, and the critical values of inductors to operate the suggested converter in the CCM are derived as follows:

$$V_{(L1)ON} = L_1 \frac{\Delta I_{L1}}{dt} = V_{in} \quad (15)$$

$$V_{(L2)ON} = L_2 \frac{\Delta I_{L2}}{dt} = V_{in} \quad (16)$$

Where I_{L1} and I_{L2} are currents flowing through L_1 and L_2, respectively. The character dt is a change in the time. Rearranging equation (15) and (16)

$$\Delta I_{L1} = \Delta I_{L2} = \frac{V_{in} D}{L f_S} \quad (17)$$

Where f_S is the switching frequency.

$$V_{(L3)ON} = L_3 \frac{\Delta I_{L3}}{dt}$$

I_{L3} refers to the current flowing through L_3

$$L_3 \frac{\Delta I_{L3}}{dt} = V_{C2} + V_{C3} - V_{C4} \quad (18)$$

Substituting equations (10), (11), and (12) in equation (18) yields

$$\Delta I_{L3} = \frac{(1+D)D}{L_3 f_S} V_{in} \quad (19)$$

To find maximum and minimum current through L_1 and L_2, the equation (20) is derived from fig. 5 as shown below:

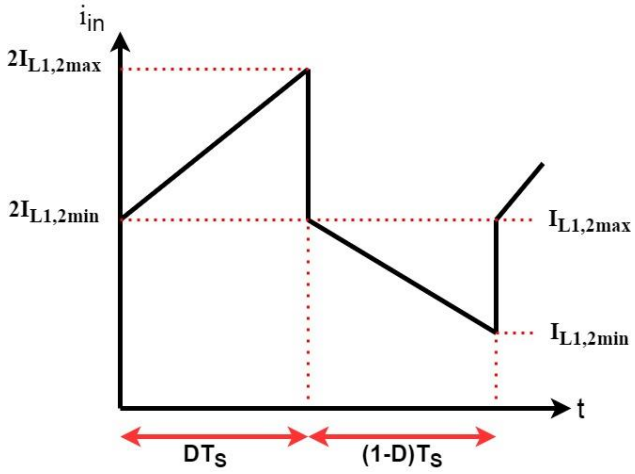


Figure 5. Current waveform through L_1 and L_2 during continuous conduction mode

$$i_{in} = \frac{1}{2}(1+D)\left(I_{L1,2max}+I_{L1,2min}\right) \quad (20)$$

Where i_{in} refer to the average input current, $I_{L1,2max}$ and $I_{L1,2min}$ are the maximum and minimum current through L_1 and L_2

$$I_{L1,2max} = \frac{V_{in}D}{Lf_S} + I_{L1,2min} \quad (21)$$

Substituting equation (21) in (20) and rearranging

$$I_{L1,2max} = \frac{i_{in}}{(1+D)} + \frac{DV_{in}}{2Lf_S} \quad (22)$$

$$I_{L1,2min} = \frac{i_{in}}{(1+D)} - \frac{DV_{in}}{2Lf_S} \quad (23)$$

Also, the maximum and minimum current through L_3 can be determined by considering $I_{L3} = I_O$ at switching turned ON

$$I_{L3} = \frac{V_O}{R} = \frac{(2+D)(1+D)V_{in}}{(1-D)R} \quad (24)$$

Where R is the load resistance

$$I_{L3max} = I_{L3} + \frac{\Delta I_{L3}}{2} \quad (25)$$

$$I_{L3min} = I_{L3} - \frac{\Delta I_{L3}}{2} \quad (26)$$

Where I_{L3max} and I_{L3min} are the maximum and minimum currents through L_3

Substituting equations (19) and (24) in both equations (25) and (26) and rearranging the equations then

$$I_{L3min} = \frac{(2+D)(1+D)V_{in}}{(1-D)R} - \frac{(1+D)DV_{in}}{2L_3f_S} \quad (27)$$

$$I_{L3max} = \frac{(2+D)(1+D)V_{in}}{(1-D)R} + \frac{(1+D)DV_{in}}{2L_3f_S} \quad (28)$$

To find and calculate the boundary value of L_1 and L_2, the equation (29) is derived from fig. 6 as shown below:

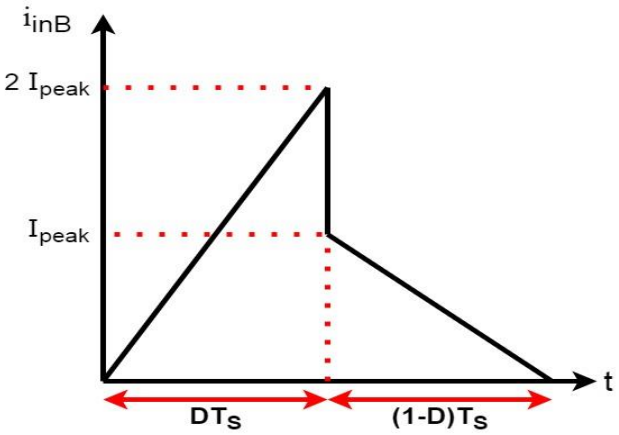


Figure 6. Current waveform across of L_1 and L_2 during boundary conduction mode

$$i_{inB} = \frac{2I_{peak}D}{2} + \frac{I_{peak}(1-D)}{2} \quad (29)$$

Where i_{inB} is the average of the input boundary current and I_{peak} is the peak current of L_1 and L_2, respectively.

$$i_{inB} = \frac{I_{peak}\,(1+D)}{2} \quad (30)$$

$$I_{peak} = \frac{V_{in}D}{L_Bf_S} \quad (31)$$

Where L_B is the boundary value for L_1 and L_2. Substituting equation (31) in equation (30) gives

$$i_{inB} = \frac{(1+D)DV_{in}}{2L_B f_S} \quad (32)$$

Then substituting equation (32) in equation (14) and rearranging

$$L_B = \frac{D(1-D)^2 V_O}{2I_O f_S (2+D)^2 (1+D)} \quad (33)$$

$$L_B = (L_1)_B = (L_2)_B \quad (34)$$

Equation (33) gives the boundary value of L_1 and L_2. Below which (L_1, L_2 < L_B), the suggested converter works in the DCM while it works in the CCM if (L_1, L_2 > L_B).

Also, the boundary value of L_3 can be derived by equating I_{L3min} to zero in equation (27) and rearranging it as

$$(L_3)_B = \frac{(1-D)D\,V_O}{2f_s(2+D)I_O} \quad (35)$$

Equation (35) gives the boundary value of L_3, below which (L_3 < L_B), the suggested converter works in the DCM while it works in the CCM if (L_3 > L_B).

3. Design of the Proposed SEPIC Converter

To prove the theoretical studies during steady-state in CCM of operation, the following specifications are presented in the design example:

V_{in} = 30 V

V_o = 225 V

P_o = 100 W

f_S = 50 kHz.

(a) Selecting the value of duty cycle: Value of duty cycle of the proposed converter is calculated from equation (14)
$D = 0.5$

(b) Inductance selection L_1, L_2 and L_3: L_1, L_2, and L_3 are assumed to be the same value. Each ripple current of the L_1, L_2, and L_3 is obtained from equation (17) by taking into account a maximum current ripple equal to 10 percent of the input current.

$$L_1 = L_2 = L_3 = \frac{V_{in}D}{\Delta I_L f_S} = \frac{30 * 0.5}{0.333 * 50000} = 900\ \mu\text{H} \quad (36)$$

Where I_{in} is calculated from equation (14) as follows:

$$I_{in} = \frac{(2+D)(1+D)}{(1-D)} I_O = \frac{2.5 * 1.5 * 0.44}{0.5} = 3.33 \quad (37)$$

and

$$I_O = \frac{P_O}{V_O} = \frac{100}{225} = 0.44\ \text{A} \quad (38)$$

(c) Calculate the load resistance:

$$R = \frac{{V_O}^2}{P_O} = \frac{225^2}{100} = 506\ \Omega \quad (39)$$

(d) Capacitance selection C_1, C_2, C_3, C_4, and C_{out}: The values of the capacitors are calculated by considering voltage ripple of each capacitor equal to 0.1 volt as follow:

$$C_1 = C_2 = C_3 = C_4 = \frac{P_O}{\Delta V_C V_O f_S} = \frac{100}{0.1 * 225 * 50000} = 88\ \mu\text{F} \quad (40)$$

$$C_O = \frac{P_O D}{\Delta V_C V_O f_S} = \frac{100 * 0.5}{0.1 * 225 * 50000} = 44\ \mu\text{F} \quad (41)$$

The proposed SEPIC converter is designed and simulated using the MATLAB program and the parameters used for simulation are given in the table below.

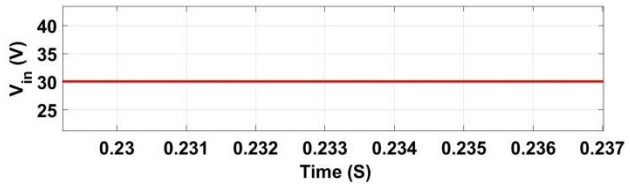
Table 4. Design parameters of the suggested converter

Parameter	value	unit
Input voltage	30	V
Output voltage	225	V

Output power	100	W
Switching frequency	50	kHz
Duty cycle	0.5	-
Load resistance	506	Ω
Inductors (L_1, L_2, L_3)	900	µH
Capacitors (C_1, C_2, C_3, C_4)	88	µF
Output Capacitor (C_O)	44	µF

4. Simulation Results of Proposed Converter

To confirm the theoretical analysis as described in this paper, the proposed converter has been implemented in the MATLAB program. Simulation outcomes are provided in the CCM operation to confirm the theoretical analysis. The simulation results are shown in steady-state situation for better disclosure. The simulation results of output voltage, input voltage, switch voltage and voltages across C_1, C_2, C_3, C_4, L_1, L_2, and L_3 in the CCM operation are shown in fig. (7). Fig. 7(a) and (b), indicates a high output voltage is obtained from 30 V supply voltage. The voltage gain is around 7.5 for a duty cycle of 0.5 and the output voltage is around 225 V. As depicted in fig. 7(e), the voltage stress on switch is equal to the voltage across C_2 as derived in equation (10) and the voltage values of capacitors (C_1=45, C_2=C_3=90, and C_4=135) which is similar to the values calculated using equations (9), (10), (11), and (12) at duty cycle of 0.5. Fig. (8) presents results of the waveforms for input current, output current, switch current, and the current of inductors $L_1, L_2,$ and L_3 with 2.6 A and 0.44 A average currents respectively. As shown in fig. 8(a), the proposed converter has continuous input current. The value of output current in fig. 8(b) equal 0.44 A as derived in equation (38). Fig. 8(d) shows that through mode-I, current across all inductors increases with a positive slop and in mode-II it begins to decreases with a negative slope as predicted. Fig. (9) shows simulation waveforms of current in diodes D_1, D_2, D_3, D_4, D_5, D_6, and D_{out} with current peak values at ON and OFF states of switch S.



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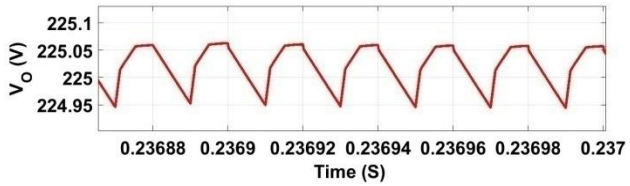

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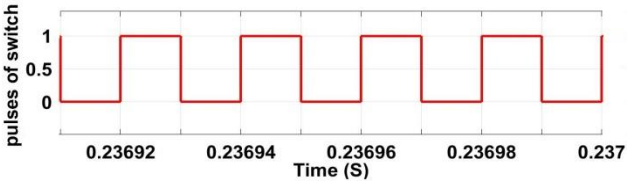

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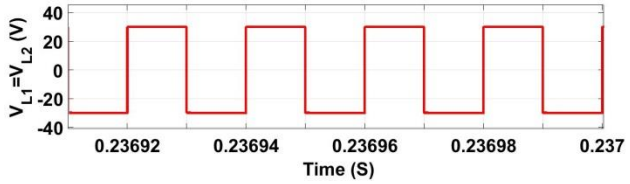

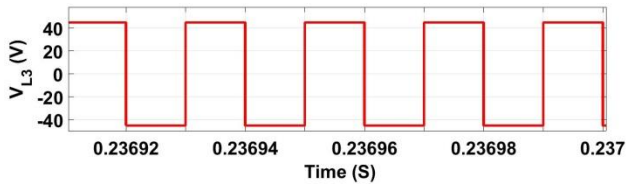

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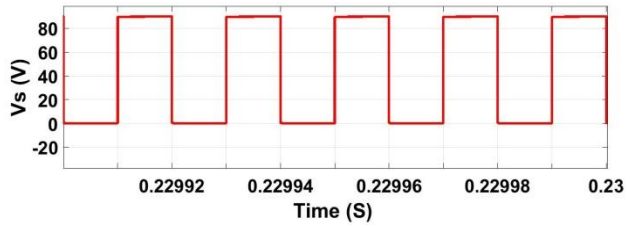
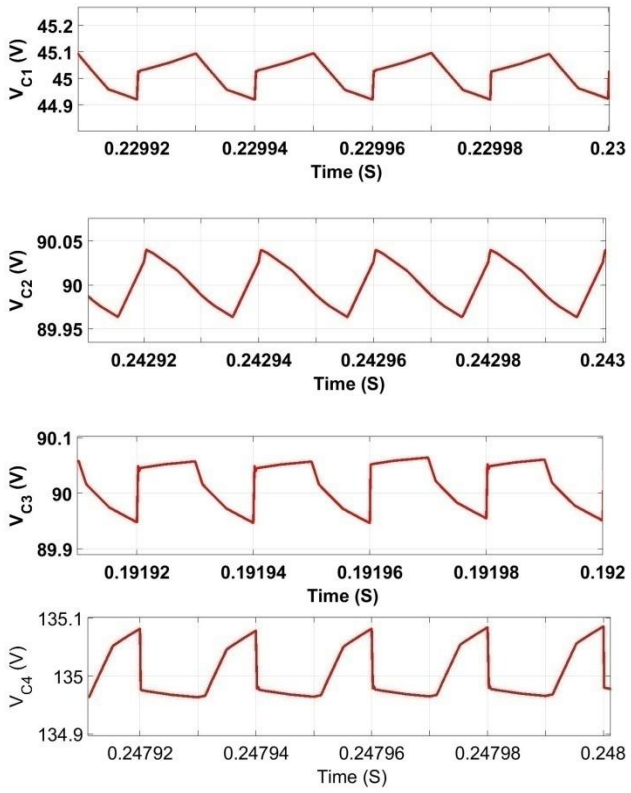
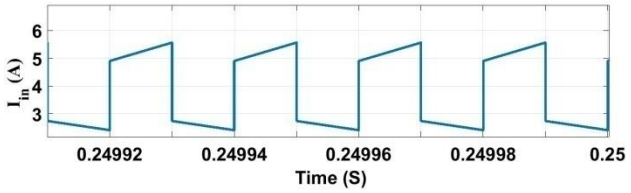




(e)

Figure 7. Simulated waveforms voltage (a) Input voltage, (b) Output voltage, (c) Pulses of switch, (d) Voltage across L_1, L_2, and L_3, (e) Voltage across switch, C_1, C_2, C_3, and C_4



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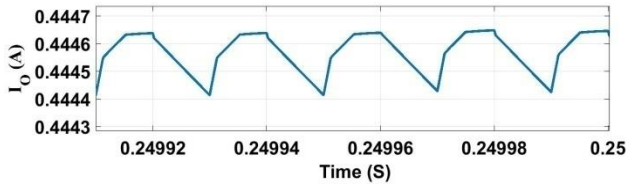
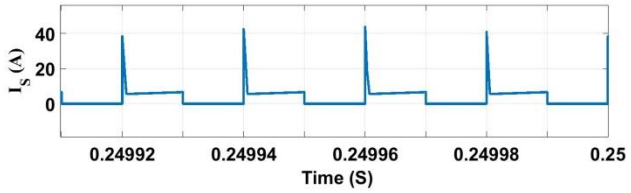
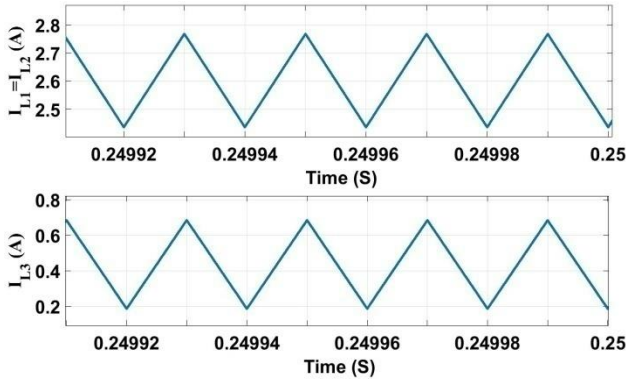


(b)



(c)



(d)

Figure 8. Simulated waveforms current (a) Input current, (b) Output current, (c) Switch current, (d) Current across L_1, L_2, and L_3

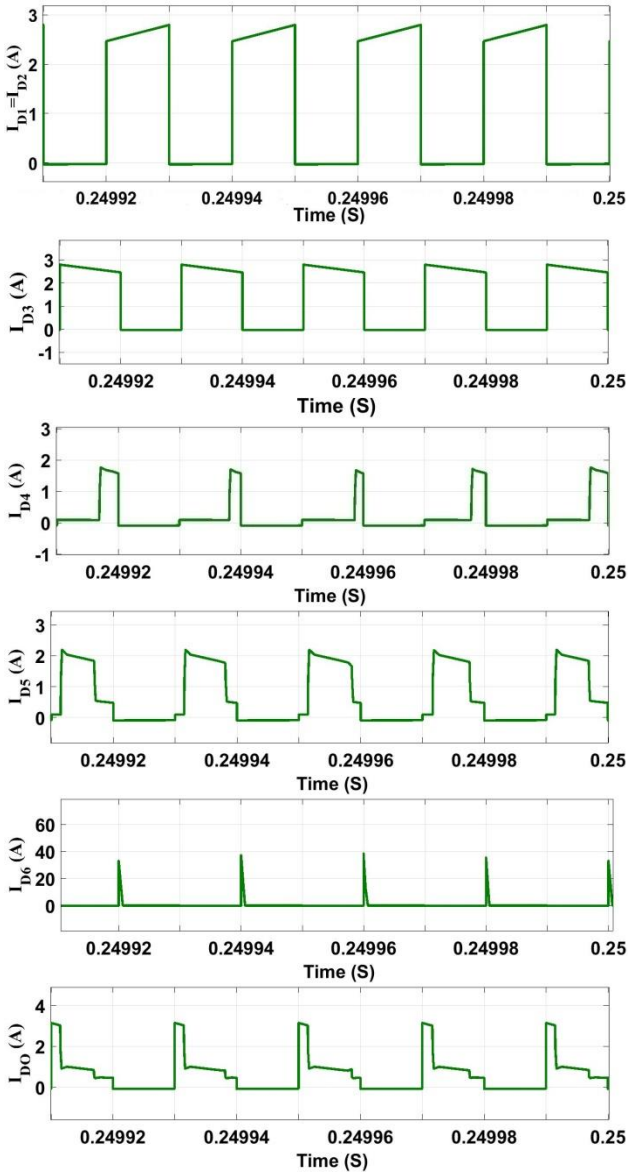


Figure 9. Simulated waveforms current in D_1, D_2, D_3, D_4,

D_5, D_6, and D_{out}

5. Conclusions

In this paper, a new design of DC-DC converter SEPIC type depending on a split-inductor and switching capacitor arrangement was produced. The suggested converter provides high gain comparing with the modified converter presented in [6] and proposed converters presented in [5] and [18]. In addition, comparing with the modified SEPIC converter, it is capable of reducing the output voltage ripple. With the help of switched capacitor and split-inductor, the stress on the switch S is greatly reduced, so the performance of the suggested converter is greatly enhanced. The theoretical studies of the proposed SEPIC DC-DC converter are presented in the continuous conduction mode. Also, the voltage transfer gain is derived in this mode. A MATLAB/Simulink program is used to test and confirm the theoretical analysis of the proposed converter. This converter has the following benefits, according to simulation results: high voltage gain can be achieved with a low duty cycle, continuous input current, low acceptable output voltage ripple, and non-inverting output voltage. For the suggested SEPIC converter, the voltage stress of the switch S is equal to the voltage of capacitor C2 and equal to 90 V which is less than voltage stress of switch comparing with the modified converter presented in [6] and proposed converters presented in [5] and [18]. The proposed SEPIC DC-DC converter achieves a voltage gain of 7.5 times of the supply voltage.

Conflict of interest

The authors announce that there is no conflict of interest in the publishing of this article.

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