Journal of Engineering and Sustainable Development
www.jeasd.org
Vol. 22, No.03, May 2018
ISSN 2520-0917

MITIGATION OF HARMONIC DISTORTION USING OPTIMUM PHASE-SHIFT MULTIPLE PARALLEL INVERTERS

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Abstract: It is clear that the harmonics in power systems have many negative impacts and therefore it is inevitable to reduce their amount to the accepted level and one of the interesting approach to reduce the harmonic distortion is to synchronize phase-shifted inverters operating in parallel. In this paper, a relatively modern technique for harmonic reduction employing synchronized phase-shifted three parallel PWM inverters with current-sharing reactors is analyzed. By using this method, the total harmonic distortion (THD) has been reduced significantly and the amount of reduction is directly proportional to the number of parallel phase-shifted inverters.

Keywords: *Parallel Inverters, Pulse Width Modulation, Harmonic Distortion, THD*

تخفيف التشوه التوافقي بأستخدام إزاحة ألطورالامثل للعاكسآت المتعددة المتوازية

الخلاصة: من الواضح أن التوافقيات في نظم الطاقة لديها العديد من الآثار السلبية، وبالتالي فإنه لا بد من تخفيض قيمتها إلى المستوى المقبول. إحدى ألطرق ألمثيرة للإهتمام للحد من التشويه التوافقي هو مزامنة عاكسآت متعددة متوازية. في هذا البحث، تم تضمين تقنية حديثة نسبيا للتقليل من التوافقيات وهي مزامنة ثلاثة عاكسات متوازية تعمل وفق نظام تضمين عرض ألنبضة مع استخدام مفاعلات مقسمة ألتيار. باستخدام هذه الطريقة، تم تخفيض التشوه التوافقي الكلي بشكل كبير ومقدار التخفيض يتناسب طرديا مع عدد العاكسات ألمتوازية.

1. Introduction

The idea of parallel operation of both kinds of inverters, voltage source inverter (VSI) and current source inverter (CSI) has attracted the attention and interest of many researchers especially as alternative energy sources are being connected to electric utility grid systems. Operation of multiple inverters in parallel is possible where DC sources are available especially from a renewable energy sources or other sources combined with a DC link. Parallel operation of multiple inverters contributes to reduce harmonic distortion of the entire system drastically [1]. Many approaches introduced a current reactor as interface between the output of VSI and the load to provide current waveform control.

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For economic and cost effective consideration, many methods have been employed to minimize such reactors[2].

Another group of researchers employ alternative approach, which is adjusting each inverter in parallel scheme automatically with random component and this lead to better harmonics cancellation and finally improvement of power quality [3].Introducing of parallel operation of multiple inverters in renewable energy systems and others is useful for a number of reasons such as reduction of maintenance costs through operation of many identical elements, cost effective and simpler design, increased reliability through redundancy, etc, without over sizing the single inverter. The drawback of this operation is that it introduces a relatively large inter-tie reactors between the inverter and the common-coupling point [4,5,6], and the issue of the possible circulating currents between inverters. In addition to all previously mentioned the possible need for communication between the inverter control systems is considered as not desirable issue [3]. In this paper we analysis the impact of the phase-shift delay between the parallel inverters on the total harmonic distortion THD of the entire system through using PSpice and Simulink/Matlab software as well as the experimental results for a single inverter, two synchronized phase-shifted parallel inverters with an optimum phase delay of Tc/2, and three synchronized shifted parallel inverters with an optimum phase delay of Tc/3 is presented, where Tc is the carrier period.

Fig.1 depicts a single-phase H-bridge inverter. In this configuration, each inverter in the system is introducing a fixed-frequency naturally sampled pulse width modulation (NSPWM) methodology, in this method the triangular or saw tooth carrier waveform is compared with the reference sine waveform. With this type of high frequency carrier waveform, both phase-legs of the H-bridge are modulated and this significantly reduces the adverse impacts of the harmonics of the pulse train [7]. In this work we select the carrier frequency (fc) to sine reference sinewave frequency (fs) ratio, fc/fs, to be 20 and we set the modulation index MI to be 0.6 with two and three parallel inverters using 3-level NSPWM which has a better harmonic profile than bi-level NSPWM [8]. Fig. 2 illustrates this method to generate three-level NSPWM unfiltered voltage pulses. It is clear as fc/fs increases, the number of pulses generated per cycle will increases and the output will be closer to required sine wave. In other words as fc/fs increase, better harmonic profile obtained and consequently THD will be reduced.

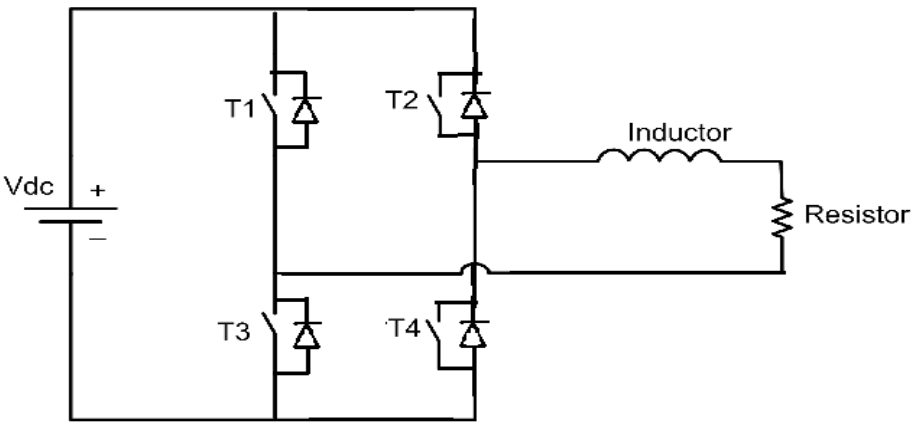

Figure 1. Single-phase H-bridge inverter.

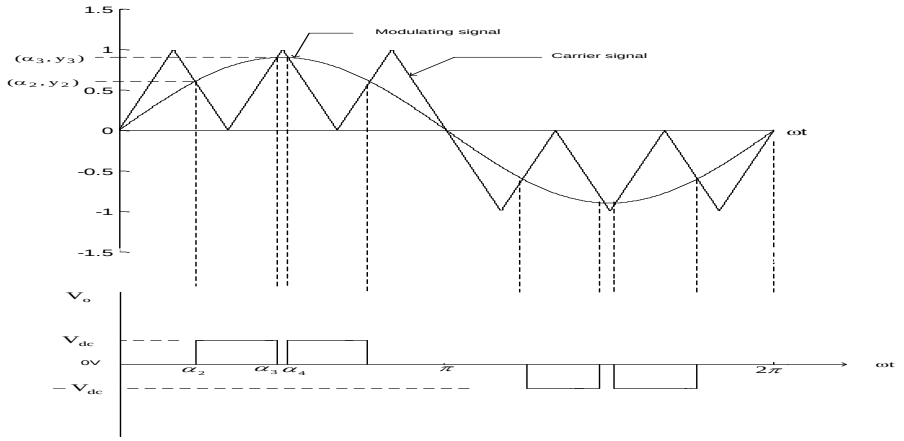

Figure. 2 Three-level NSPWM technique with fc/fs =3

one of the main factors that affect the total harmonic distortion (THD) is the modulation index (MI) which is the ratio of the peak value of the sine wave(referred in the Figure as a modulating signal) to the peak value of the carrier signal (it is 1 per unit) and normally has a value of $0 < \mathrm{MI} \leq 1$ but it is not recommended to be greater than 1 because of possible generation of sub-harmonics that results in increasing THD.

From the definition of THD which is the ratio of square root of the sum of squares of the peak values of all voltage or current harmonics except the fundamental to the peak of the fundamental which is exactly equal MI, we can find the relation between THD and MI as following:

$$\mathrm{THD} = \frac{\sqrt{V_2^2+V_3^2+V_4^2+V_5^2\ldots\ldots\ldots\ldots}}{V_1} \quad (1)$$

$$\mathrm{THD} = \frac{\sqrt{V_2^2+V_3^2+V_4^2+V_5^2\ldots\ldots\ldots\ldots}}{\mathrm{MI}} \quad (2)$$

$$\mathrm{THD} = \frac{Constant}{\mathrm{MI}} \quad (3)$$

Therefore THD has a reverse proportional relation to MI, i.e. as MI increases, the THD decreases and this results in a better harmonic profile and consequently the best quality of energy delivered.

2. Analysis of Optimum Inverters Phase Delay

Fig.3 illustrates the proposed technique of parallel operation of three full-bridge inverters and the number of parallel inverters can be extended. From the Figure, it is obvious that the DC sources are isolated from the system and output reactors are employed as a current controller. The inverter reactors combined with the connected grid inductance contribute to sum-up all current outputs of the multiple inverters.

The second and third inverters in this system phase-shift delays (with respect to first inverter) are varied from 0 and Tc in a three parallel inverters configuration. The optimum phase shift that results in the lowest total harmonic distortion in this case is

found to be Tc/3 (ie, the second inverter lags first one by Tc/3, and third inverter lags first by 2 (Tc/3)). Note that the optimum THD for three-parallel inverters is around 1.4% and this demonstrates the superiority of this technique to reduce THD and

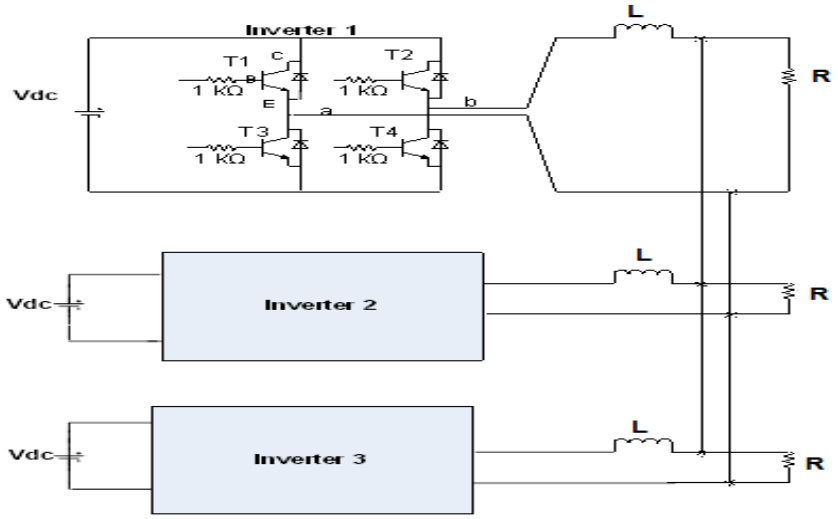

Figure 3. Schematic diagram of three parallel H-bridges PWM invertors.

consequently better quality of the delivered power. From above Figures, we conclude that the optimum phase shift between N numbers of parallel synchronized inverters to obtain minimum THD is Tc/N.

In this paper we explore the optimum phase shift between the parallel inverters with 3-level PWM that results in a minimum total harmonic distortion (THD). Fig. 4 illustrates the THD obtained versus phase-shift delay between two parallel with MI=0.6 and fc/fs=20. The optimum phase-shift delay that results in the lowest total harmonic distortion THD is found to be near Tc/2 where Tc is the carrier period, but exactly is 0.506 Tc. From the figure, it is clear that the THD is 11.35% when no phase-shift delay between two inverters and optimum THD is 2.95%.with the parameters selected as shown in Table 1.

Fig.5 shows the THD of the system in which the second and third inverters phase-shift delays (with respect to first inverter) are varied from 0 and Tc in a three parallel inverters configuration. The optimum phase shift that results in the lowest total harmonic distortion in this case is found to be Tc/3 (ie, the second inverter lags first one by Tc/3, and third inverter lags first by 2 (Tc/3)).

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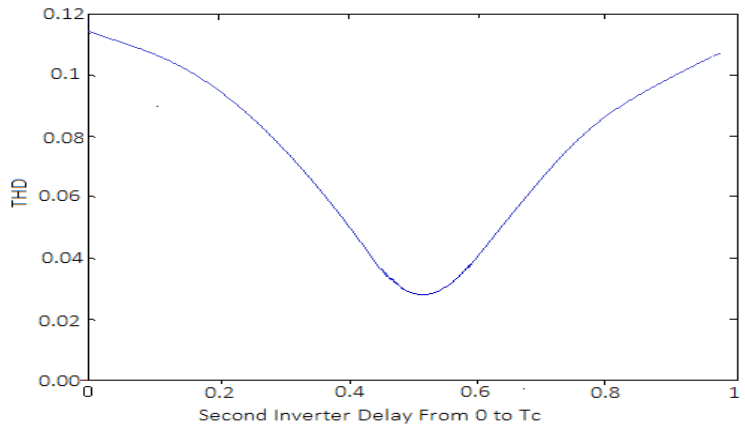


Figure 4. THD versus phase-shift delay for 2 parallel inverters with MI=0.6 and fs/fc=20

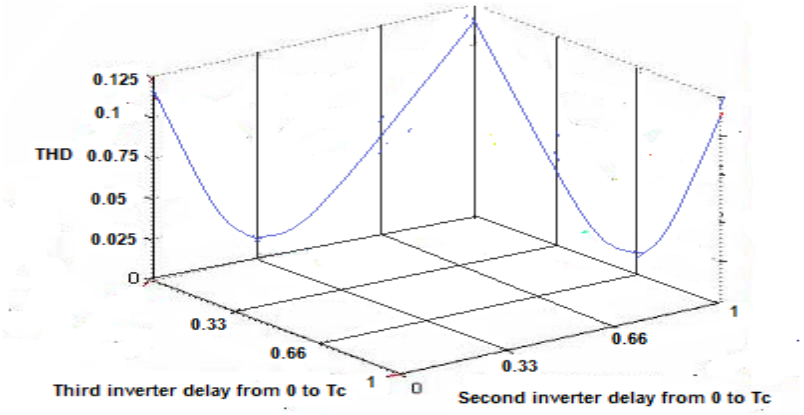


Figure 5. THD versus phase-shift delay for 3-parallel inverters with MI=0.6 and fs/fc=20

3. Simulation Results

To comprehend the analysis of phase shifting of multi-parallel synchronized inverters it is important as a first step to consider the switching strategy for two synchronized phase-shifted inverters as depicted in Fig. 6. In Fig. 6 (a and b), the output pulses of each NSPWM 3-level inverter is demonstrated. The second inverter is driven as the first inverter but delayed by Tc/2. Introducing current sharing inductors, the unfiltered resultant Vn at the common point of the two parallel inverters, can be derived for N numbers of parallel inverters as:

$$Vn = [V_{out(1)} + V_{out(2)} + V_{out(3)} + \ + V_{out(N)}] / N \qquad (4)$$

Where $V_{out(k)}$ is the output pulses of the Kth inverter. Fig. 6 (c) demonstrates the output resultant voltage waveform for the case N=2 (i.e., two parallel inverters). It is clear that the number of voltage levels in this voltage waveform per each cycle period is five levels (0V, 1/2 Vdc, Vdc, -1/2 Vdc, - Vdc) compared to the three levels in the case of one inverter and this number ascends to seven levels per cycle in the case of three-parallel inverters (0V, 1/3 Vdc, 2/3 Vdc, Vdc, –1/3 Vdc, –2/3 Vdc, – Vdc) as shown in Fig. 7. Thus in general the number of unfiltered output voltage waveform levels is equal

to 2N+1 where N= number of parallel inverters and as N increases, the resultant output voltage waveform becomes more sinusoidal-like with an effectively higher carrier frequency N x fc

Fig. 8 depicts the output voltage waveforms for the previous cases and Table 2 shows the corresponding THD which decreases as N increases.

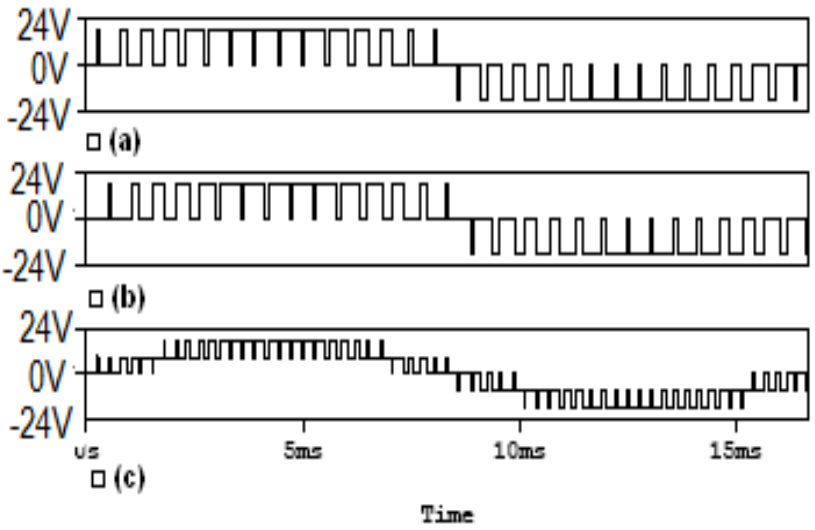


Figure 6. (a) Two parallel inverters with voltage pulses at the output of the first inverter
(b) Two parallel inverters with voltage pulses at the output of the second inverter
(c) The resultant output voltage pulse for two parallel inverters

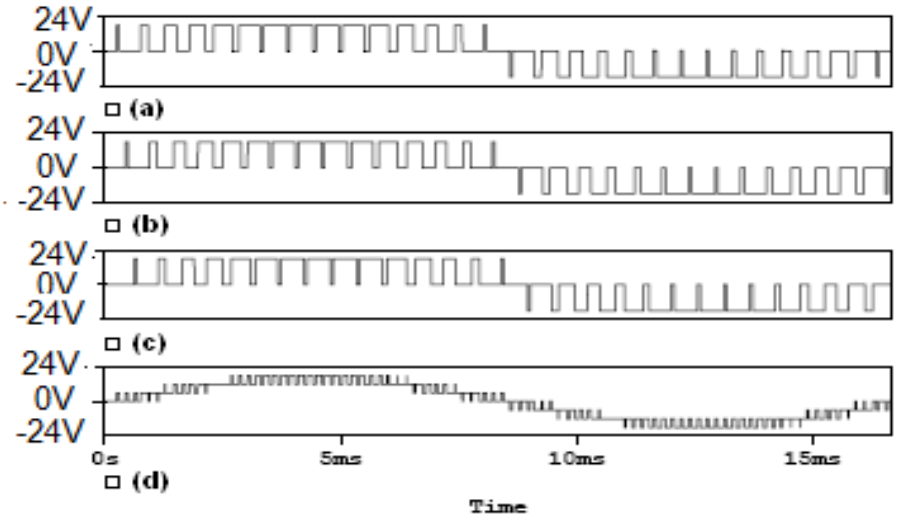


Figure 7. (a) Three parallel inverters with voltage pulses at the output of the first Inverter.
(b) Three parallel inverters with voltage pulses at the output of the second inverter.
(c) Three parallel inverters with voltage pulses at the output of the third inverter.
(d) The resultant output voltage pulses for three parallel inverters.

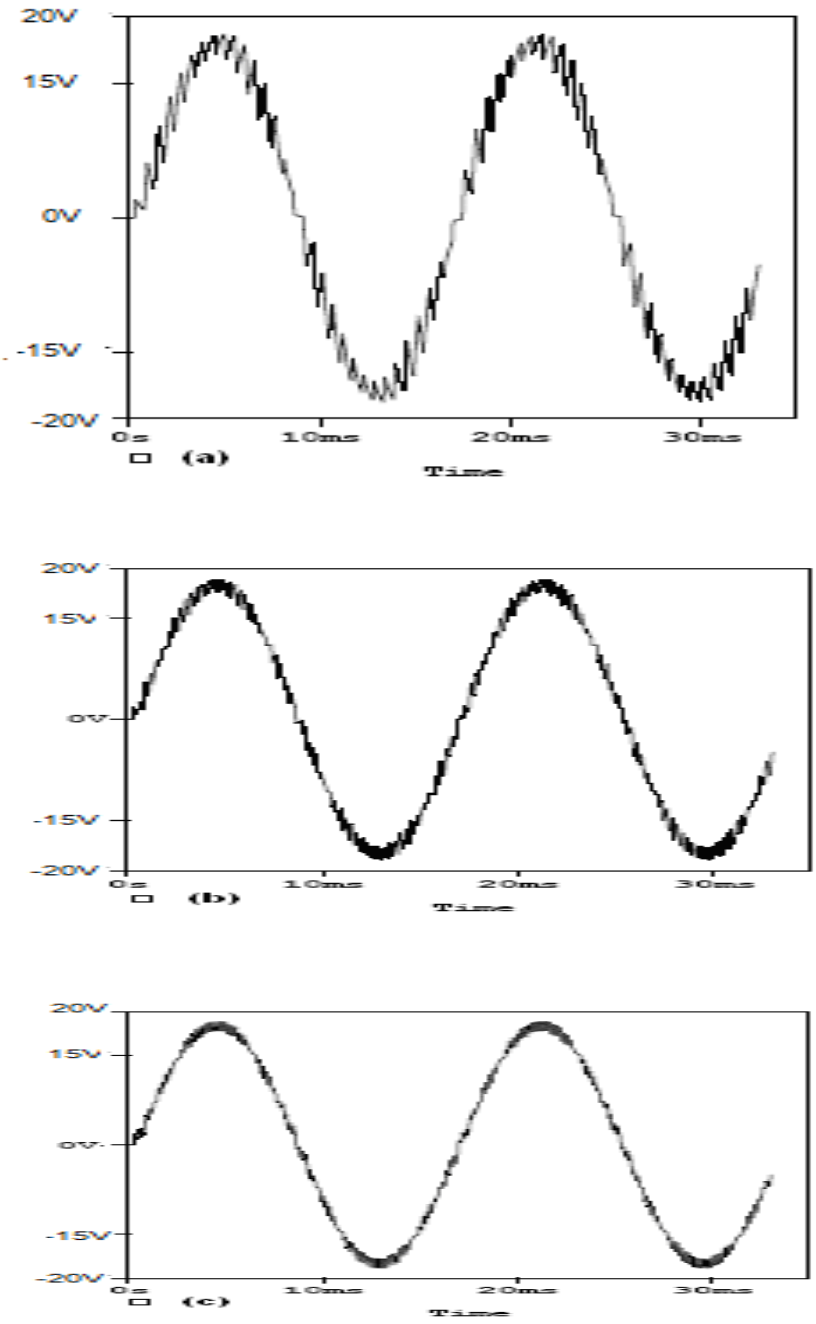


Figure 8. (a) Simulation output voltage waveform for single inverter
(b) Simulation output voltage waveform for two parallel inverters
(c) Simulation output voltage waveform for three parallel inverters

4. Experimental Results

The components used in experimental work are shown in Fig.9 which identifies the block diagram of the implemented proposal. The components used include PIC 16F877 micro-controllers to generate the PWM gating pulses to drive the semi-conductor switches of the inverters, the synchronization unit that consists of an external clock source to drive the OSC1/CLKIN pin, and a master reset connected to the MCLR pin.

Fig.10 depicts the experimental wave forms for single, two parallel, and three parallel inverters and it is clear from the output voltage waveforms that the waveform is

getting closer to ideal sine wave form as the number of parallel inverters increases. Table 2 demonstrates the corresponding THD results obtained which verifies the simulation results.

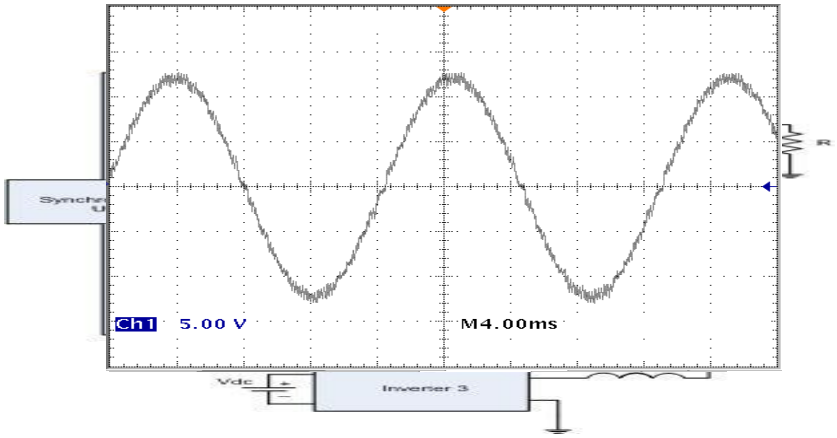
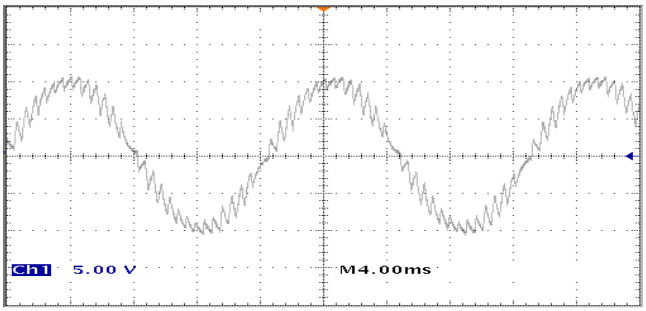


Figure 9. Experimental block diagram for the proposed methodology

Table 1. Parameters used in simulation and Experimental works

Parameter	Value
fc/fs	20
MI	0.6
Vdc	15 V
L	200 mH
R	100Ω

(a)



(b)

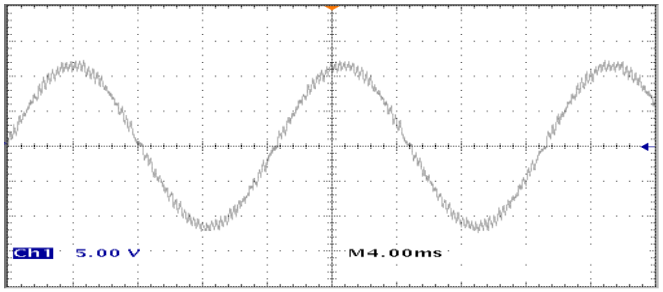
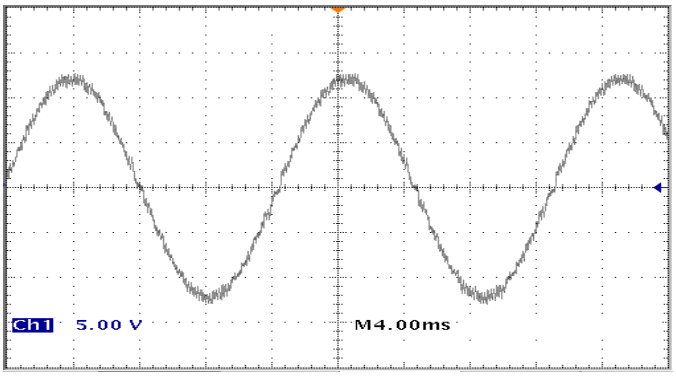


Figure 10. Experimental output voltage waveforms (oscilloscope).
(a) For one inverter
(b) For two parallel synchronized inverters
(c) For three parallel synchronized inverters



(c)

Figure 10. Continued

Table 2 Simulation and experimental results.

	One Inverter	Two Inverters	Three Inverters
MATLAB Results	11.35 %	2.95 %	1.40 %
PSpice Results	11.37 %	3.01%	1.42 %
Experimental Results	11.82 %	3.37%	1.47 %

5. Conclusions

In this paper, the technique of optimum phase-shift in synchronized phase shifted parallel PWM inverters with current-sharing reactors is proposed. The output voltage waveforms and the numerical result obtained demonstrate the significant reduction in THD of the entire system. Experimental results verified and validated our simulation results. Therefore, the proposed technique is a promised methodology for the harmonics reduction of the renewable energy systems.

6. References

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