A CHEAP ZILOG MP APPLIED TO SPREAD SPECTRUM SYSTEMS DESIGN

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Abstract: : The Z2000 Evaluation Board performing direct sequence spread spectrum processing, a 900 MHz radio receiver and a transmitter module , was applied to build a Direct sequence spread spectrum transceiver , RF board was designed & implemented for the purpose by al - Ezz company in Iraq **.**

Key words: *Spread Spectrum , Direct Sequence , Pseudo Noise , Non-Coherent Systems , CDMA*

تصميم منظومة طيف منتشر باستخدام معالج رخيص نوع زايلوك

الخلاصة: يقدم هذا البحث لوح الكتروني للمعالج Z2000 الطيف منتشر السلسلة المباشرة. استخدم نموذج استلام وارسال راديوي بتردد 900MH لبناء سلسلة مباشرة للطيف ارسال واستلام. وتم تصميم وتنفيذ لوح الترددات الراديوية وفقا لأغراض شركة العز العامة في العراق.

1. Introduction

1.1 Spread Spectrum Methods

Spread spectrum systems are classified by the ways that the original data is modulated by the PN code [1]. The most commonly employed spread spectrum techniques are the following:

- Direct Sequence Spread Spectrum (DSSS)
- Frequency Hopping Spread Spectrum (FHSS)
- Hybrid Direct-Sequence and Frequency-Hopping Spread Spectrum
- Time Hopping Spread Spectrum
- Chirp Spread Spectrum

So there is a variety of methods for spreading a signal for transmission [1]. The general strategy for spread spectrum communication is to subdivide a communications channel into K sub bands. Ks < K of these sub bands are selected in each time slot (chip) and the available energy is split among them, leaving the remaining ones unused [2]. It can be shown that the effective jamming energy, Eoj, is

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Eoj = EjKs / K

Where EJ is the actual energy transmitted by the jammer [1]. Thus, with jam energy as a metric, Ks = 1 is an optimal strategy. Under other metrics, such as error rates, other choices for Ks may be desirable, however [3].

The two main classes of spread spectrum communications systems are frequency hopping (FH) and direct-sequence (DS) systems [1]. In an FH spread spectrum system, the spreading is accomplished by modulating a carrier frequency that is changed (or hopped) in each time slot. In each chip time, k bits from a binary pseudo-random noise (PN) sequence are used to select one of 2^k carrier frequencies distributed over the available bandwidth.

The receiver then uses an estimate of the PN sequence to determine which carrier frequency to use for demodulation during each chip. DS SS systems forego the use of a spreading carrier frequency, instead directly

Modulating the data signal by a higher-rate PN sequence [1]. This electively spreads the bandwidth by the ratio of the PN bit rate to the data bit rate. Demodulation is performed at the receiver by generating an estimate of the PN sequence and using this to demodulate each chip. Both classes of systems can be classed as coherent or non-coherent, depending on whether or not they spherically recover the clock used at the transmitter. In a coherent system, the receiver attempts to synchronize itself to the chip clock [3].

Non-coherent systems perform the demodulation without explicitly generating a local synchronized chip clock. FH systems are typically popular for military applications because interference between adjacent channels within a band is only observed when they randomly occupy the same frequency channel . In commercial situations, such as cell phone networks, DS systems are far more popular. This owes to better spatial bandwidth sharing (i.e., bandwidth pollution from one cell to its neighbors is lower than in FH systems) and simpler receiver designs.

1.2 Direct Sequence Spread Spectrum Technique

The DSSS physical layer uses an 11-bit Barker Sequence to spread the data before it is transmitted. Each bit transmitted is modulated by the 11bit sequence. This process spreads the RF energy across a wider bandwidth than would be required to transmit the raw data. The processing gain of the system is defined as 10x the log of the ratio of spreading rate (also known as the chip rate) to the data. The receiver despreads the RF input to recover the original data. The advantage of this technique is that it reduces the effect of narrowband sources of interference. This sequence provides 10dB of processing gain that meets the minimum requirements for the rules set forth by the FCC. The spreading architecture used in the direct sequence physical layer is not to be confused with CDMA. All 802.11 compliant products utilize the same PN code and therefore do not have a set of codes available as is required for CDMA operation.

The processing gain Gp is defined by: Processing gain =
Gp = transmitted signal bandwidth / information bandwidth   (1)
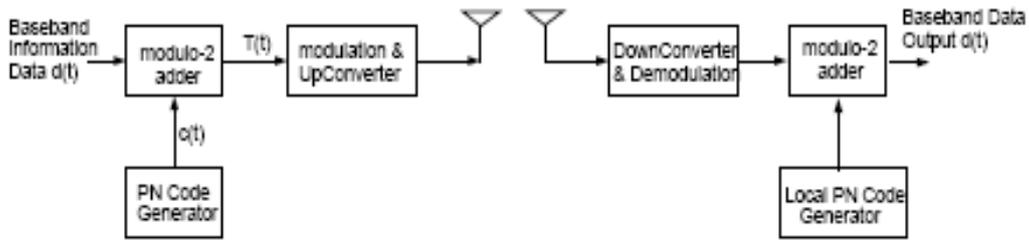
Fig (1): A Typical Direct Sequence Spread Spectrum Transmitter & Receiver.

2. The Z2000 Chip operation

The main stages of the Z2000-Mp are containing:

2.2 Encoder

In the deferential encoder, the polarity of the data is presented in the phase change between consecutive bits. The deferential decoder can correctly recover the original data as long as the phase deference between successive symbols is maintained after the transmission. The absolute phase of each symbol is not required for correct decoding. Hence, the deferential modulation allows a phase ambiguity that may be introduced by some carrier recovery circuits.

For binary phase shift keying (BPSK) operation, the deferential encoder compares the input bit in(k)with the previous output bit out (k − 1) by a logical exclusive-OR operation:

$$out(k) = in(k) \oplus out(k-1) = \overline{in(k)} \cdot out(k-1) + in(k) \cdot \overline{out(k-1)}$$

(2)

where $\oplus$ represent the exclusive-OR operation or modulo-2 addition.. An arbitrary reference binary digit is assumed for the initial bit of the output sequence.

For quadrature phase shift keying (QPSK) operation, the differential encoder is more complicated. There are four possible states in each of the inputs and outputs of the differential encoder.
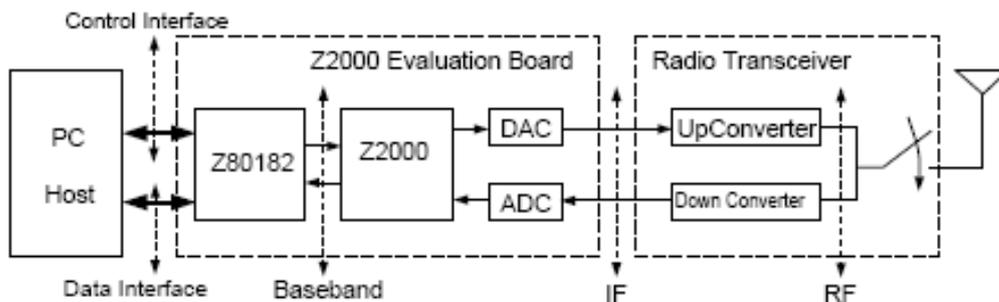

Fig (2): The Overall Transceiver System

2.3 PN Spreader

The Z2000 uses symbol-synchronous PN modulation in data transmission and reception. This means that every data symbol (I and Q symbols in QPSK mode) coming out of the differential encoder is XOR-ed with one complete PN code sequence.

Thus, we see that the data rate is increased by the length of PN code and the spectrum is spread after PN modulation by the same number. The Z2000 allows two independent PN codes to be employed: one for preamble and another for information data. Moreover, the lengths of these two PN codes may be deferent. However, the length of both have an upper bound of 64 chips due to hardware limits and a lower limit of 10 chips because of the FCC Part 15 requirement of 10 dB minimum processing gain.

It is suggested that a longer PN code be used for the preamble. This takes advantage of the higher processing gain and it will improve burst acquisition performance. The lengths and their coefficients of both PN codes are programmed by Z80182 control registers.
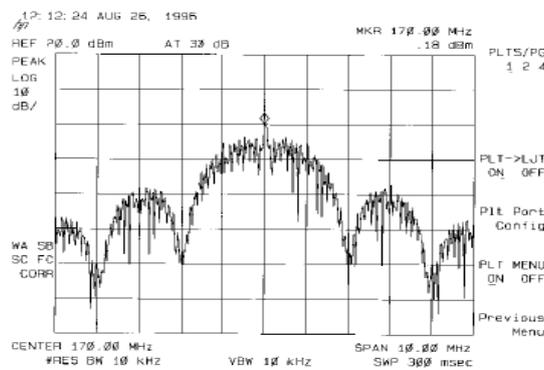

Fig (3): Transmitter output spectrum.

3. Receiver

The sampled and digitized received IF signal is first down-converted to base band and the PN-despread with a PN matched filter. A symbol tracking processor incorporates a threshold detector to detect a correlation peak once per symbol and a \flywheel circuit" to track the symbol.
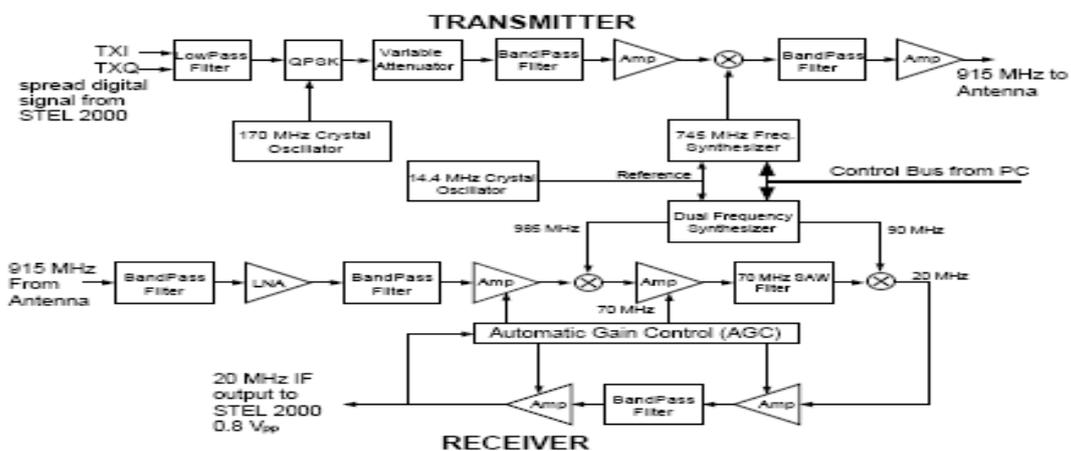

Fig (4): RF Module Architecture.

3.1 PN Matched Filter

The PN matched filter is designed to operate with two signal samples per chip to allow the system to sample the incoming signal asynchronously with respect to the PN spread rate. This requires that the integrate and dump filter output rate must be twice the PN chip rate. Also, to avoid spectrum aliasing, the output rate of the integrate and dump _filter must be less than or equal to one half the frequency of RXIFCLK. The number of samples summed by the integrate and dump filter is the number of RXIFCLK samples over half a PN chip duration. A front-end processor operating at the front of the matched filter averages the data stream from the integrate and dump filter over each chip period by adding each incoming sample to the previous one.

The PN matched filter calculates the cross-correlation between the incoming signal and the locally stored PN code coefficients twice per chip.

The matched filter output is

$$output = \sum_{n=0}^{63} Data(n \cdot 2T) * c(n \cdot 2T)$$

(3)

Note that 1/T is the base band sampling rate, which is twice the chip rate. In other words, T is half the chip duration. For the proper operation of the PN matched filter, a delay time of 2T (one chip duration) is required for each of the 64 delay lines.

4. The Emulation Program

1. Program Start
2. Select MIMIC or ESCC-B
3. Reset STEL 2000
4. Reset its register copy
5. Reset ESCC channel
6. Initialize ESCC to SDLC
7. Enable ESCC
8. Configure STEL 2000
9. Allocate Buffer Space
10. Set Tx Buffer Content
11. Reset Rx Buffer to Zero
12. Print out the Control Menu
13. Waiting for User Response
15. User Response?
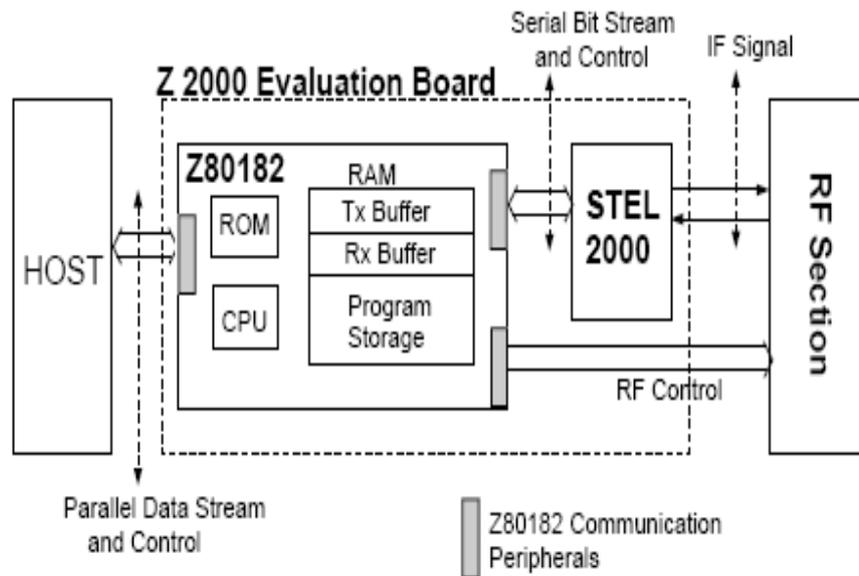16. User Command Processing
17. End

Fig (6): Overall Software Environment

6. Results

The results are obtained when 63-bit M-sequence code is used as the PN spread code and the signal is BPSK modulated. An on-board 16 MHz crystal oscillator provides the receiver IF clock signal (RXIFCLK). The register at address 41H defining the number of TXIFCLK cycles per chip is set to 7. Thus, from the Z2000 User's Manual, the PN chip rate is given by:

$$16 \text{ MHz} / (7 + 1) = 2\text{MHz} \tag{4}$$

It is a polar base band signal spectrum with the 1st side lobe 13 dB lower than the main lobe. The low-pass filter is a three-element Butterworth filter with a cutoff frequency at 2 MHz. The 1st side lobe is attenuated about 7 dB , we show the spectrum of the output from the Colpitts crystal oscillator. This signal is amplified after a MAV-11 amplifier and low-pass filtered by a three-element Butterworth filter. This filter is designed to cutoff at near 170 MHz The graph shows that the 170 MHz frequency output is fairly clean and the second harmonic is more than 25 dB below the desired 170 MHz.

The output signal level is adjustable through the current controlled attenuator. If a helical band pass filter with center frequency at 170 MHz and a cutoff bandwidth of 4 MHz is available later, it should be operated between two stages of amplification will expect the side lobes be attenuated to a greater degree., we can say that this Tx Exciter works as we designed to perform the BPSK modulation at 170 MHz

The low pass filter (LPF) of Butterworth type was used in the system to ensure the decrease of noise on the signal . also the 2MHz cut off frequency is determined for the low pass filters used in accordance with the experimental reports.
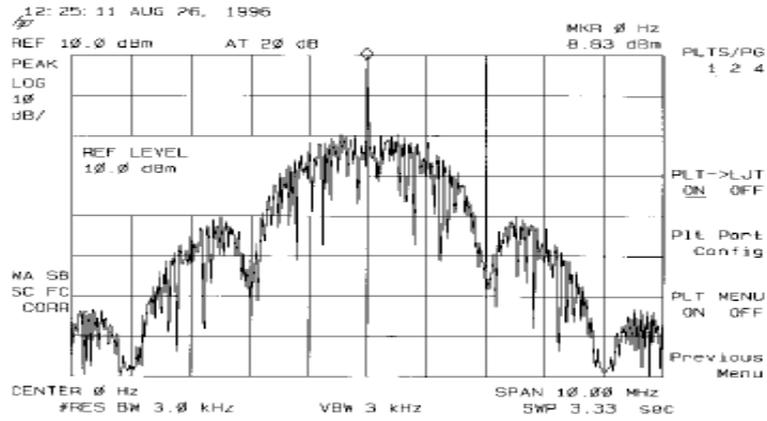
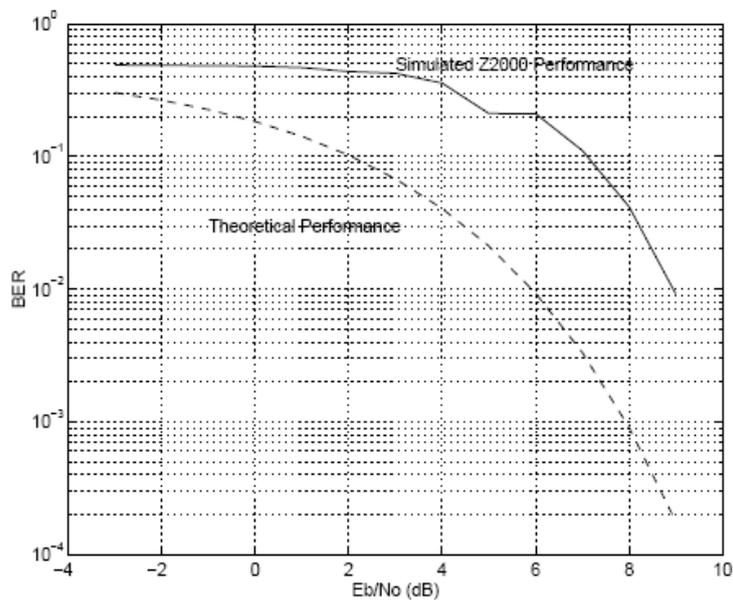Fig (5): Base band Spread Signal Spectrum After Low-pass Filter.

Fig (7): BER Performance with Symbol Tracking (Threshold = 5)

7. Conclusions

A physical layer design for an ISM band direct sequence spread spectrum wireless LAN is presented. This physical layer directly interfaces with the MAC layer and uses the 902-928 MHz ISM band for the RF transmission. The Zilog Z2000 Evaluation Board is implemented for the spread spectrum processing.

A proper hard ware for the RF was designed using (intersil) evaluation board with u/c & attenuation compatible with it.

BER was in accepted limits for such transmission as well.

8. Acknowledgement

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