Improving The Performance of Quadratic Boost Converter By Adding Auxiliary Inductor

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Abstract

This paper suggests a new method to achieve input current ripple (ICR) reduction of the quadratic boost converter (QBC). The planned converter is represented by adding an auxiliary inductor connected in a series with the bootstrapping diode to a QBC. The benefit of this arrangement is to implement the interleaving concept to lessen ICR, while the quadratic concept is to attain the voltage gain within the required level. However, this modification will slightly affect the output voltage; the effect depends on two factors: the duty cycle and the auxiliary inductor value. The performance improvement includes increasing dynamic response speed, reducing reverse recovery and conduction losses in semiconductor devices and less oscillation observed by ICr, leading to better stability than the conventional converter. Therefore, the converter's overall efficiency is improved. A comparison with a typical QBC was presented using the LTspice program to demonstrate the improvement.

Keywords- Quadratic boost converter, Interleaved boost converter, Input current ripple reduction, LTspice.

I. INTRODUCTION

In numerous applications where isolation is not required, boost converters (BC) are extensively employed in step-up DC-DC conversion and power factor correction[1]. It is widely known in the literature that conventional BC is inadequate for high-gain requests due to the parasitic circuit resistance and the limited commuting periods of semiconductor components. These drawbacks can limit the converter gain, where the output voltage value will not exceed twice the input voltage [2], [3]. Furthermore, some applications, such as converters designed for renewable energy and light-emitting diode (LED) drivers, should be supplied with a constant current from the DC source [4]. In addition, the maximum amount of energy from renewable sources can be obtained with a constant continuous ICr [5]. This is because the value of a high root-mean-square (RMS) current caused by a large current ripple would lead to increased losses and heat, which could hasten the deterioration of the life span of LED light [6]. Hence, it is imperative to employ converters with high gain and low ICR. [7].

To lessen the ICR of the traditional BC, a considerable value of the input inductor needs to be added at the front end [8]. Nevertheless, large inductor values not only increase the total size of the converter but further decrease its dynamic response. Several methods are used in this field to minimise the ICR. One of these methods is using an effectively structured input LC filter. This method gives acceptable results in low and medium-power applications, but the volume of the filter makes it unsuitable for use in high-power applications [9].

Various ripple cancellation networks (RCN) have been presented for use in DC-DC converters, Such as in [10], [11], where the converter uses RCN comprising of a modest-sized capacitor and a modest-sized inductor. Based on the conventional BC to achieve a tapped inductor, resulting in a smaller and lighter converter than the traditional LC input filter. This topology suits typical applications such as SMPS, electric vehicles, fuel cells and renewable energy sources.

With the boost or other step-up converter, the BC can be cascaded to obtain high voltage gain [12]–[14], but this approach requires multiple components for each stage, leading to a complex, costly, and inefficient circuit [15]. One typical method to simplify the circuit and minimise the number of components is integrating it into a single-switch converter by employing a main switch shared among many functions [16]. The converters exhibit increased gain due to their quadratic component, enabling them to cancel the ICR and perform buck-boost conversions[17]–[19], and boost conversion [20]–[22]

The coupled inductor used in a non-isolated DC-DC converter allows for a more significant voltage level increase. However, a coupled inductor increases the ICR; adjusting (RCN) specifications without increasing the dimension of the inductor can reduce the current ripple [23]. The study [24] proposed a QBC with a double-coupled inductor and a ripple absorption circuit for a high-gain DC-DC converter. The regulating range of voltage gain can be efficiently extended. The restriction of duty ratio can be eliminated by incorporating a voltage-multiplying unit into the converter, and the magnetic element's volume can also be decreased.

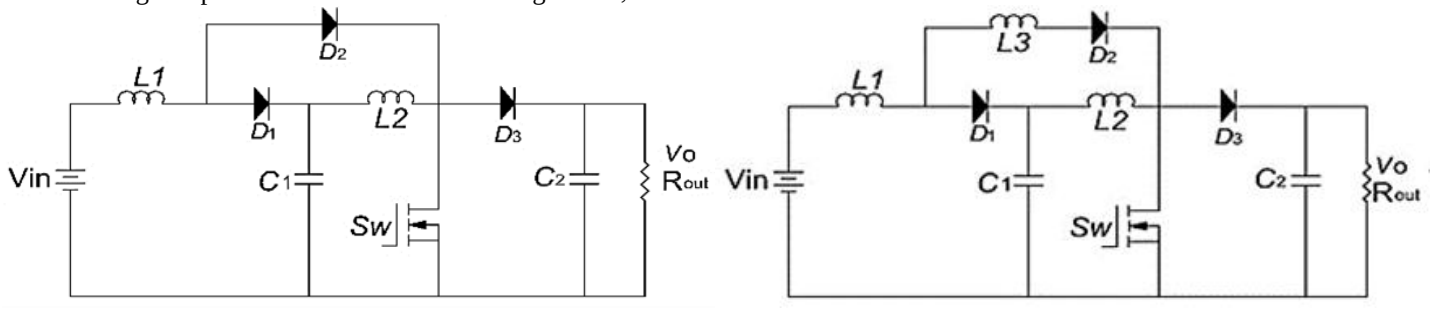
The interleaved BC reduces the ICR and is commonly used in higher power ratings. The parallel configuration of these converters distributes switch current and thermal loads, improving efficiency and reliability [25]. As interleaved cells increase, the ICR decreases. The study [26] introduces a high step-up interleaved cascade converter with several advantages over the conventional cascade BC, Which includes a higher voltage gain, lower ICR, and lowered voltage stress on switches and diodes. It also shares ICr between inductors, allowing the use of lower current-rated inductors, which reduces the converter's size and conduction losses while increasing efficiency. The RCN configuration described in reference [27] comprises a pair of capacitors, a pair of coupled inductors, and a pair of inductors that are directly connected through a shared core. The suggested converter eliminates ICR without causing a significant increase in current stress and power loss. It provides the same benefits as the traditional IBC and can achieve high efficiency at all power ranges. Therefore, the IBC with RCN exhibits promising prospects for application in high-power and high-efficiency DC-DCconversion.

In general, the coupled inductor technique has many problems, such as the increasing current ripple, producing spike voltage across semiconductor devices as the leakage inductance of the coupled inductor, and increasing reverse recovery problems. A clamp or a snubber circuit with other techniques is employed to handle these problems [28], [29].

This paper provides a novel modification idea for reducing the ripple of the ICr. Adding an auxiliary inductor to the bootstrapping diode can achieve an interleaving process for ICr. So, the effect of this technique is enhancing the performance of the converter. A comparison with other topologies to prove the performance of the proposed topology is done by simulating the circuit using the Lt-spice Simulink/program, and the proposed converter is examined in two cases of operating conditions. Finally, an assessment and discussion of simulation results are presented.

II. The Circuit Configuration of The Proposed Converter

The conventional QBC and proposed converter configurations are shown in Figures 1 (a) and (b), respectively. Both consist of two inductors (L_1, L_2), two capacitors (C_1, C_2), three diodes (D_1, D_2, D_3), and one single power switch (Sw). The proposed converter incorporates an auxiliary inductor (L_3) that is connected in series with the bootstrapping diode (D_2) to achieve the interleaving of the ICr. This interleaving process involves directing the ICr through the (D1) branch during a portion of one cycle and through L_3 during the remaining rest period. As a result of this configuration, the converter is able to achieve a low ICR.



(a) (b)

Figure 1a The Conventional QBC [30]. 1b The Proposed Converter.

III. Principles of operation

The proposed converter is derived from the QBC structure by adding an auxiliary inductor (L_3). However, both have the same arrangement and identical components; the operation properties of the proposed converter differ from that of the conventional converter depending on the selection of the auxiliary inductor size.

The topology is studied under the following presumptions: it functions at steady-state, ideal power devices, capacitors are large enough that can maintain a constant voltage across their terminals, two inductors (L_1, L_2) are operating in Continuous conduction mode (CCM), the auxiliary inductor (L_3) is chosen to be small size to operates in discontinuous conduction mode (DCM). The basic steady-state operation of the proposed converter is shown in Figure 2 and can be described as follows:

First: - During the first state, the switch (MOSFET) is turned on, permitting current to pass from the input voltage source through the inductor (L_1), which should be previously charged. This phase consists of two intervals.

Interval 1 (t_o -t_1):- During this period, the current path is demonstrated in Figure 2 (a). The period is represented by D'. The diode D_1 is forward-biased because the effect of L_3 makes the voltage on the cathode side higher than the anode side, leading the inductor (L_1) to continue de-energising. The diode (D2) is forward-biased, and (D_3) is reversed-biased. The capacitor (C_1) and inductors (L_2& L_3) are energised by the input voltage source plus the stored energy in the inductor (L_1). The output capacitor (C_2) is discharging through the load. In this state, Δi_{L1}, Δi_{L2}, and Δi_{L3} are described by formulas (1), (2), and (3), respectively.

$$\Delta i_{L1} = \frac{(V_{in} - V_{C1})D'T}{L_1} \quad \text{Eq (1)}$$

$$\Delta i_{L2} = \frac{(V_{C1})D'T}{L_2} \quad \text{Eq (2)}$$

$$\Delta i_{L3} = \frac{(V_{C1})D'T}{L_3} \quad \text{Eq (3)}$$

$$i_{L1} = i_{C1} + i_{L2} + i_{L3} \quad \text{Eq (4)}$$

The currents of capacitors in this state are expressed as follows:

$$i_{C1} = i_{L1} - i_{L2} - i_{L3} \quad \text{Eq (5)}$$

$$i_{C2} = -I_O \quad \text{Eq (6)}$$

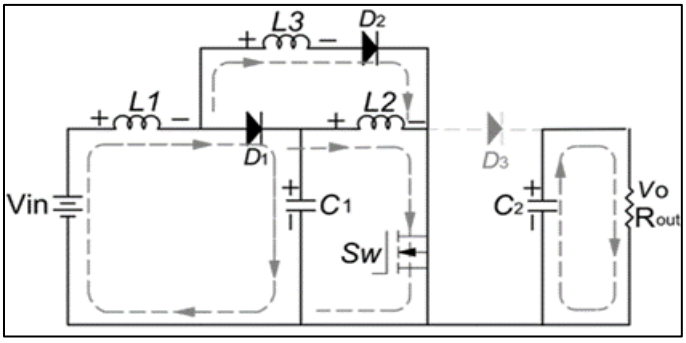


Figure 2a, Illustrates Interval 1.

Interval 2 (t_1 -t_2):- During this period, the current path is demonstrated in Figure 2 (b). The period is represented by D". (D_1) and (D_3) are reverse biased, (D_2) is forward biased, (L_1, L_3) are energising from the input source, while (L_2) is energising from the capacitor (C_1). The capacitor (C_2) continues to discharge through the R load. In this state, Δi_{L1}, Δi_{L2}, and Δi_{L3} are described by formulas (7), (8), and (9).

$$\Delta i_{L1} = \frac{(V_{in})\ D''\ T}{L_1} \quad \text{Eq (7)}$$

$$\Delta i_{L2} = \frac{(V_{C1})\ D''\ T}{L_2} \quad \text{Eq (8)}$$

$$\Delta i_{L3} = \Delta i_{L1} \quad \text{Eq (9)}$$

The currents of capacitors in this state are expressed as follows:

$$i_{C1} = -i_{L2} \quad \text{Eq (10)}$$

$$i_{C2} = -I_O \quad \text{Eq (11)}$$

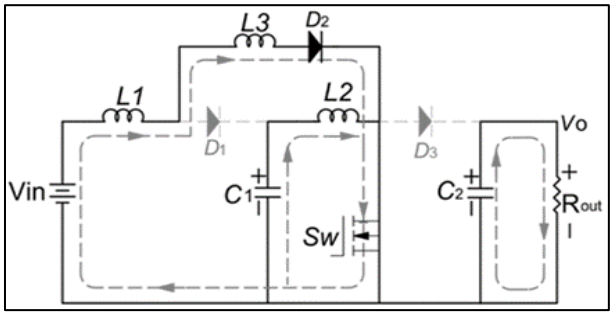


Figure 2b, Illustrates Interval 2.

It is important to note that the inductor (L_1) is only energising during the D" period on interval 2. The duty cycle D can be expressed as the sum of two intervals D' and D". As a result, the ripple current of the inductor (L_1) of the proposed converter is lower compared to the conventional converter due to the fact that D" is less than D.

The currents flowing through all inductors during the On state can be determined by summing two intervals, as described by the following formulas:

$$(\Delta i_{L1})\text{on} = \frac{(V_{in} - V_{C1})D'T}{L_1} + \frac{(V_{in})\ D"\ T}{L_1} \quad \text{Eq (12)}$$

$$(\Delta i_{L2})\text{on} = \frac{(V_{C1})D'T}{L_2} + \frac{(V_{C1})\ D"\ T}{L_2} \quad \text{Eq (13)}$$

$$(\Delta i_{L3})\text{on} = \frac{(V_{C1})D'T}{L_3} + \frac{(V_{in})\ D"\ T}{L_1} \quad \text{Eq (14)}$$

Second:- During the second state, the switch is off, beginning inductors to release their stored energy into capacitors. The voltage across the inductor reverses polarity, causing the diode to conduct and complete the circuit. This phase consists of two intervals.

Interval 3 (t_2 -t_3):- In the present condition, all diodes within the system exhibit forward bias, resulting in the charging of capacitor C_1 through the inductor L_1. L_2 and L_3 are connected in parallel, and both contribute to the charging of capacitor C_2. The functioning of this case is illustrated in Figure 2 (c). In this state, Δi_{L1}, Δi_{L2} and Δi_{L3} are described by formulas (15), (16), and (17).

$$(\Delta i_{L1})\text{off} = \frac{(V_{in} - V_{C1})(1 - D)T}{L_1} \quad \text{Eq (15)}$$

$$(\Delta i_{L2})\text{off} = \frac{(V_{C1} - V_{C2})(1 - D)T}{L_2} \quad \text{Eq (16)}$$

The inductor L_3 operates in DCM, so:

$$(\Delta i_{L3})\text{off} = \frac{(V_{C1} - V_O)\ \Delta D\ T}{L_3} \quad \text{Eq (17)}$$

Where the discharge time duty cycle of L_3 is denoted as ΔD.

The currents of capacitors in this state are expressed as follows:

$$i_{C1} = i_{L1} - i_{L2} - i_{L3} \quad \text{Eq (18)}$$

$$i_{C2} = i_{L2} + i_{L3} \quad \text{Eq (19)}$$

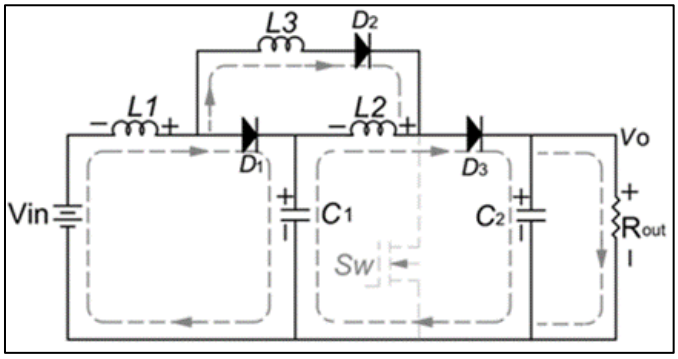


Figure 2c illustrates Interval 3.

Interval 4 (t_3 -t_4):- In the present state, all components exhibit the same performance as in the previous state, with the exception of the inductor (L_3), which has destroyed its stored energy, resulting in the absence of current flow. The functioning of this case is illustrated in Figure 2d.

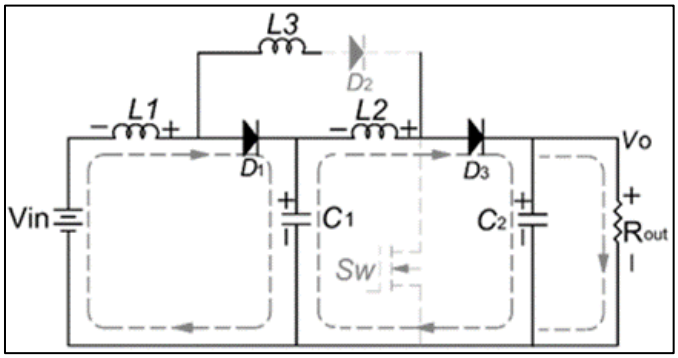


Figure 2d illustrates Interval 4.

In steady-state, the net variation of all inductors across a switching cycle equals zero. It is defined by the formulae (20) below:-

$$(\Delta i_L)\text{on} + (\Delta i_L)\text{off} = 0 \qquad (20)$$

The derivation of the expressions for $V_{C1}$and V_O, as described in formulas (21) and (22), can be obtained by applying an equation (20) for three inductors.

$$V_{C1} = \frac{(V_{in})}{(1 - \text{D"})} \qquad (21)$$

$$V_O = \frac{(V_{C1})}{(1 - \text{D})} \qquad (22)$$

The current waveform of each inductor with gate pulses which represent by (V_{GS}) and the portions of period are illustrated in Figure 3.

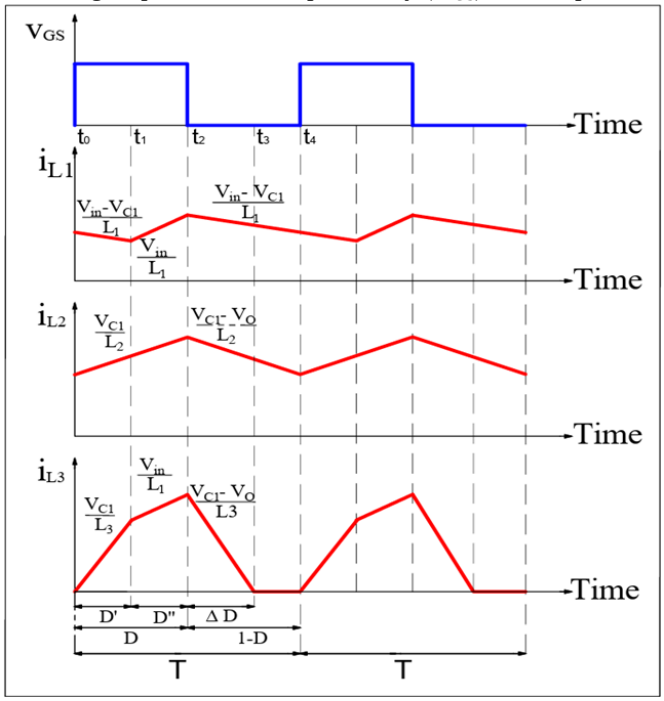


Figure 3 depicts the waveforms of the current in the inductors.

Charge time of (L_1), denoted as D", is primarily influenced by the value of (L_3) and to a lesser degree by the value of (L_1). The factor k represents the ratio of (D" to D). The relationship between the ratio of (L_3 to L_1) and the parameter k can be determined by analysing the simulation results of the proposed converter under a constant duty cycle and a fixed value of L_1, as illustrated in Figure 4.

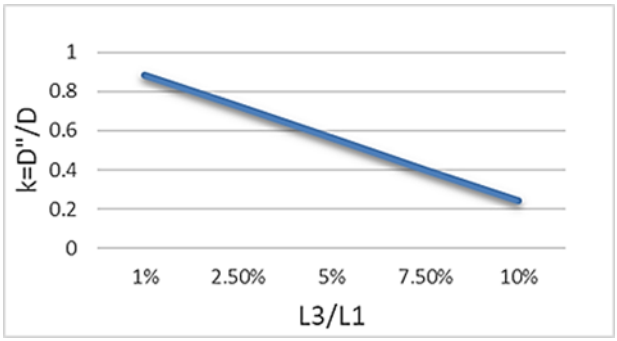


Figure 4, Illustrates the impact of the value of (L_3) on the duration required for the charging process of (L1).

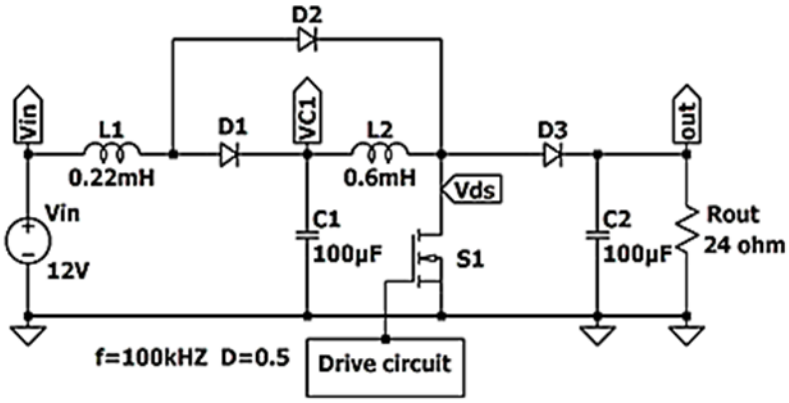
The voltage gain is denoted by the formula (23).

$$\frac{V_o}{V_{in}} = \frac{1}{(1-\mathrm{D''})(1-\mathrm{D})} = \frac{1}{(1-\mathrm{kD})(1-\mathrm{D})} \qquad \text{Eq (23)}$$

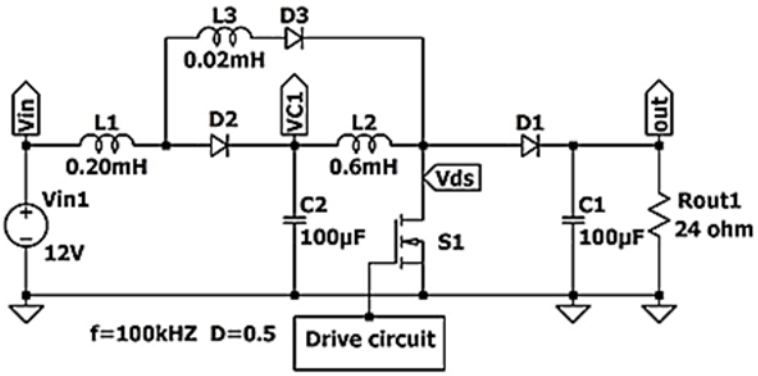
Adding the auxiliary inductor (L_3) with bootstrapping diode (D_2) is the reason behind the different behaviour of the proposed converter. On interval 1, the high voltage on the input side forces the diode (D_1) to be forward-biased; by this arrangement, the interleaving process between two branches (D_1) and (L_3) can be achieved. Therefore, ICR is significantly reduced. Furthermore, the diodes (D_1, D_2) have no reverse recovery current, and D_3 has a lower reverse recovery current than conventional ones.

IV. COMPARISON TO OTHER TOPOLOGIES

A comparative analysis was performed to confirm the performance of the suggested circuit. The evaluation relied on the proposed converter and a high step-up QBC that was studied, designed, and experimentally validated in reference [30]. The configurations of the two topologies with the magnitudes of the components are illustrated in Figure 5. Two converters operate in CCM and fixed duty cycle. The drive circuit controls the power switch. The LTSpice program is utilised to simulate the comparisons.



(a)



(b)

Figure. 5 shows the structure of the two converters using identical parameters (a) The converter in [30]. (b) The proposed converter.

In order to ensure a fair comparison, every individual element of the proposed converter has been specifically chosen to be identical to the corresponding components utilised in the converter described in reference [30]. The auxiliary inductor (L_3) is chosen to have a size that is 10% of the input-side inductor (L_1) in order to achieve an appropriate output voltage, as indicated by equation (23). The objective is to ensure that the combined inductance value of (L_1) and (L_3) in the proposed converter is equivalent to the inductance value of (L_1) in the conventional converter. The characteristics of the proposed converter were assessed through testing under two different cases:

First case: The proposed topology operates at the same duty cycle as the converter [30], which is 0.5.

Second case: The proposed topology operates at the duty cycle 0.743 to attain the same output voltage as the converter [30].

The evaluation of the converters' performance relied on the simulation results of the two cases, including the conventional one, which is illustrated and discussed in Section V.

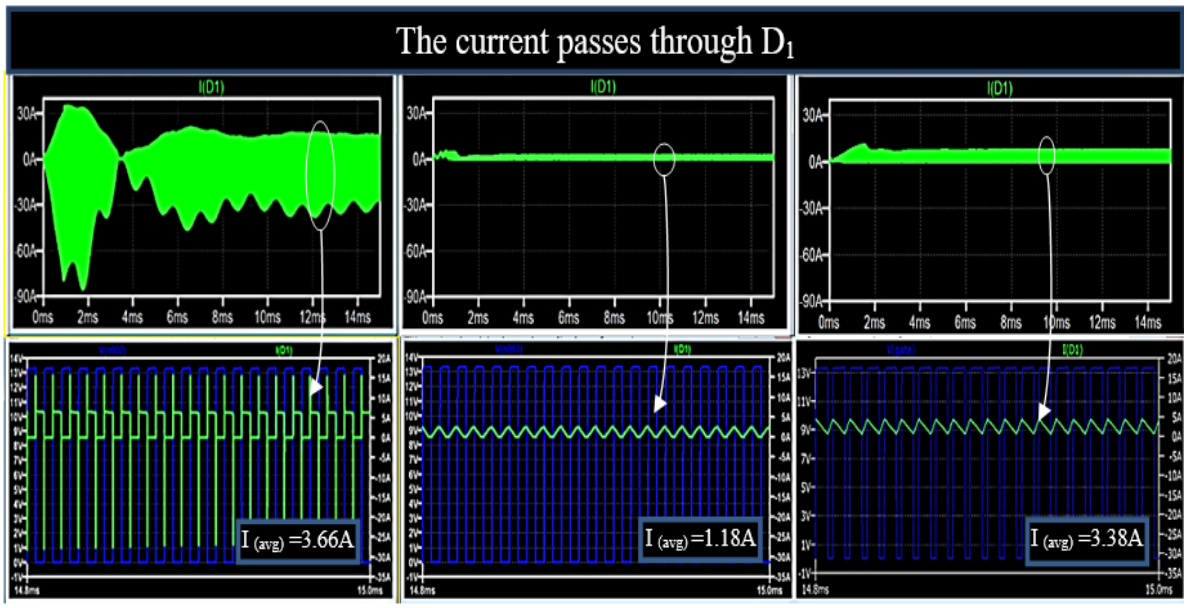
V. SIMULATION RESULT

4.2.1 Comparison results between the proposed topology and conventional converter depending on the duty cycle value.

This Section illustrates the waveforms of the parameters operating at transient and steady-state conditions, each figure accompanied by the steady-state average value of the relevant parameters. The first column represents the parameters' waveform for the conventional QBC. The second and third columns represent the parameters' waveform for the PT when it operates with a duty cycle of 0.5 and 0.743, respectively. The comparison among three cases are represented in Figure 6.

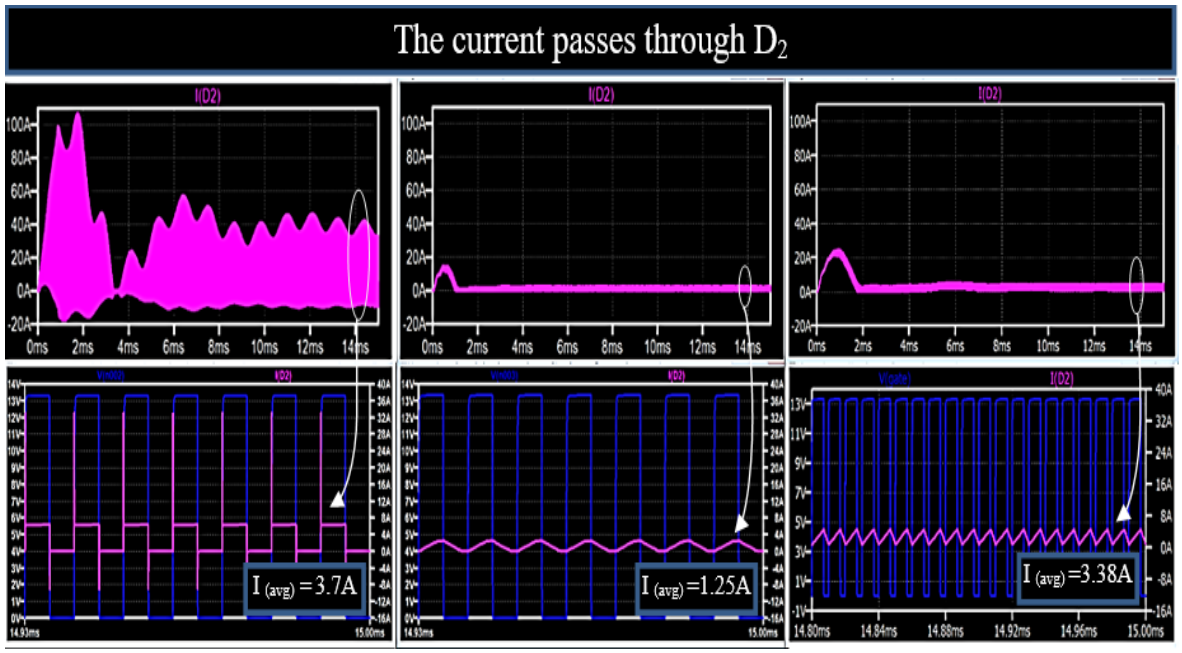
The performance of their parameters can be analysed in the following aspects:-

- The current flow through diode D_1 is depicted in Figure 6.1 (a,b,c), through D2 in Figure 6.2 (a,b,c) and through D3 in Figure 6.3 (a,b,c) respectively. The results indicate that adding an auxiliary inductor significantly reduces the reverse recovery current and magnitude of the currents passing through the diodes, even when operating at a higher duty cycle. Consequently, the rated current of the diodes is reduced, and the conduction loss is also reduced.
- The currents flow through the inductors L_1 is depicted in Figure 6.4 (a,b,c) and through L_2 in Figure 6.5 (a,b,c), respectively. The PT has a significantly lower oscillation ratio of the inductors' current. For instance, when the PT works at D=0.5, the percentage oscillation ratio for I_{L1} is (3.19% at L_3/L_1=10% and 4.33% at L_3/L_1=5%) compared to the conventional converter (69%). Furthermore, the current of the inductor L_2 does not suffer from overshooting as in the conventional one. These features permit the use of inductors with a low specification for the core especially when it works at a low-duty cycle.
- The voltage stress across the power switch (MOSFET) and the current stress in three cases are demonstrated in Figure 6.6 (a,b,c). In the PT, the current stresses on the power switch are significantly lowered. This feature allows the use of a power switch with a lower current-rated and the voltage is slightly lower.
- The output voltage and the capacitor's voltage in three cases are represented in Figure 6.7 (a,b,c). Notably, the PT has a faster response and is more stable than the conventional converter. It has a lower oscillation ratio of output voltage (0.23% at L_3 =10% of L_1 and 0.227% at L_3 =5% of L_1) compared to the conventional converter (4.13%), indicating that the PT is a better solution for applications where a low oscillation ratio of output voltage is critical.



(a) (b) (c)

Figure 6.1 illustrates the simulation results for the current pass-through diode D1of (a) The conventional QBC. (b) The PT operates with (D=0.5) (c) The PT operates with (D=0.743).



(a) (b) (c)

Figure 6.2 illustrates the simulation results for the current pass-through diode D2of (a) The conventional QBC. (b) The PT operates with (D=0.5) (c) The PT operates with (D=0.743).

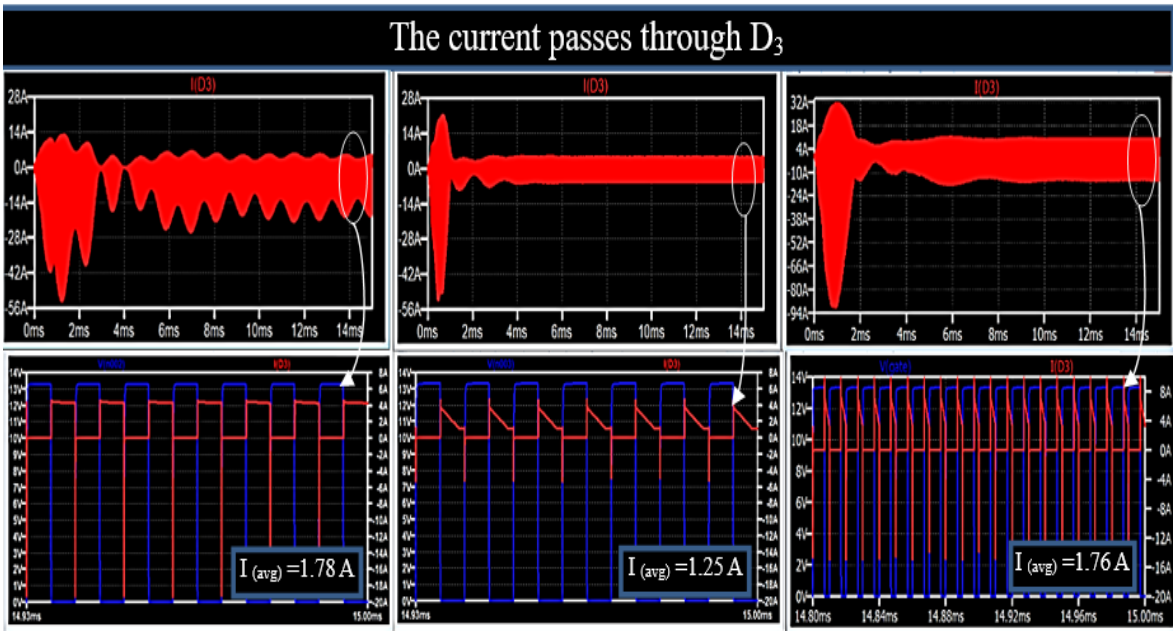


Figure 6.3 illustrates the simulation results for the current pass-through diode D3of (a) The conventional QBC. (b) The PT operates with (D=0.5) (c) The PT operates with (D=0.743).

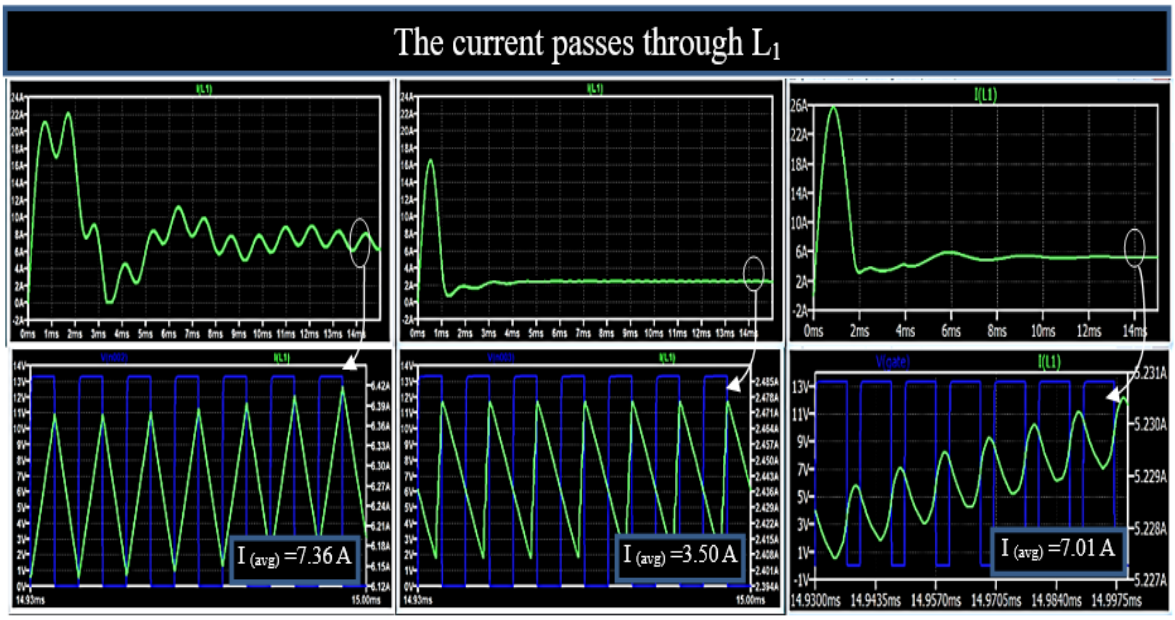


Figure 6.4 illustrates the simulation results for the current pass-through inductor L1 of (a) The conventional QBC. (b) The PT operates with (D=0.5) (c) The PT operates with (D=0.743).

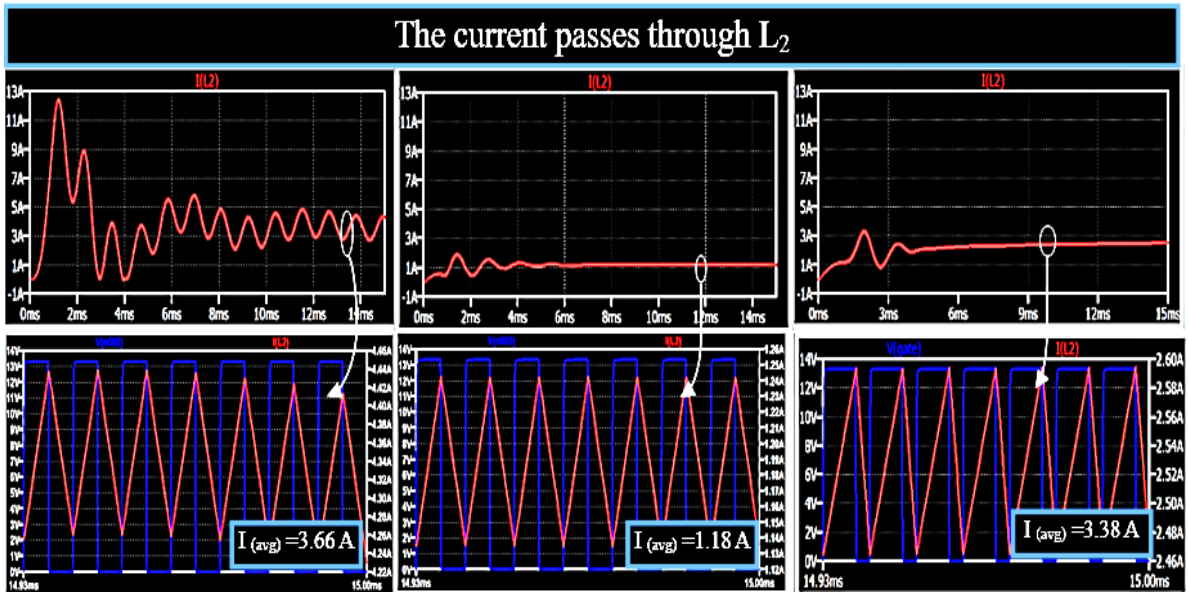


Figure 6.5 illustrates the simulation results for the current pass-through inductor L2 of (a) The conventional QBC. (b) The PT operates with (D=0.5) (c) The PT operates with (D=0.743).

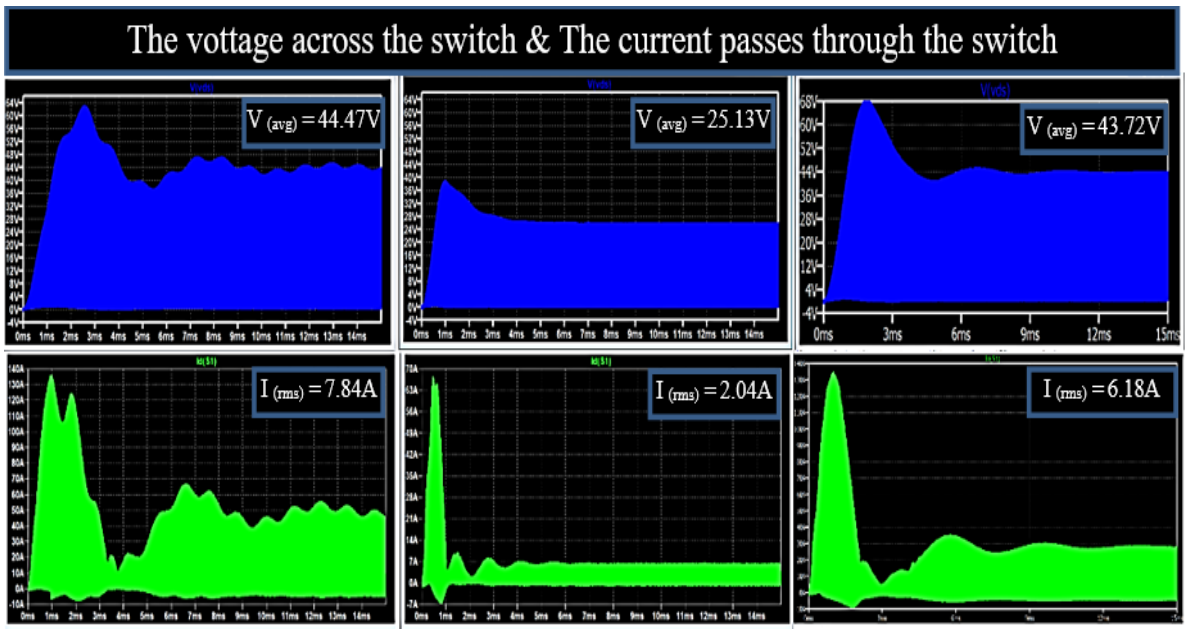


Figure 6.6 illustrates the simulation results for the switch voltage and current of (a) The conventional QBC. (b) The PT operates with (D=0.5) (c) The PT operates with (D=0.743).

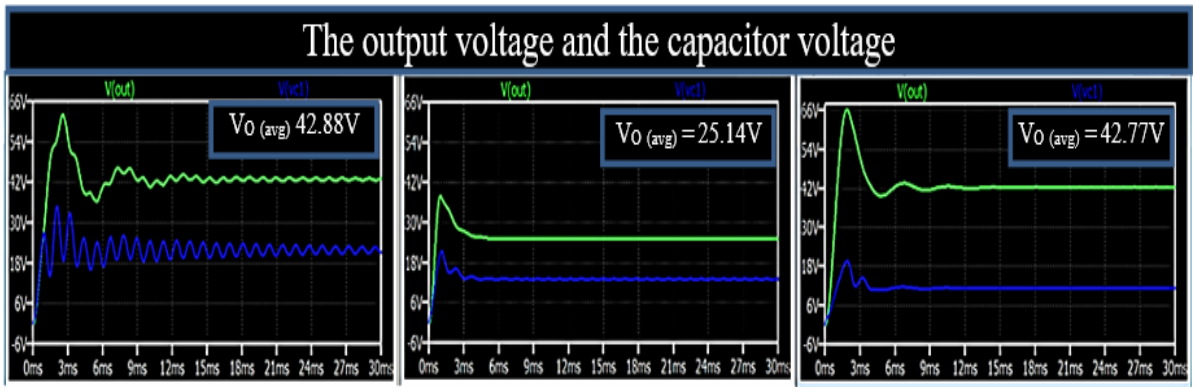


Figure 6.7 illustrates the simulation results for the output and capacitor voltage of (a) The conventional QBC. (b) The PT operates with (D=0.5) (c) The PT operates with (D=0.743).

VI. DISCUSSION OF SIMULATION RESULT

The conclusion from the above results is that the auxiliary inductor can dominate the vital properties of the proposed topology, as shown below:-

- The interleaving technique can reduce the ICR, as demonstrated in Figure 7.

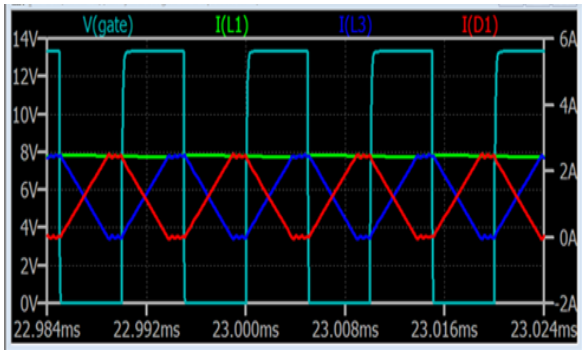


Figure 7 shows the ICR reduction of the proposed topology.

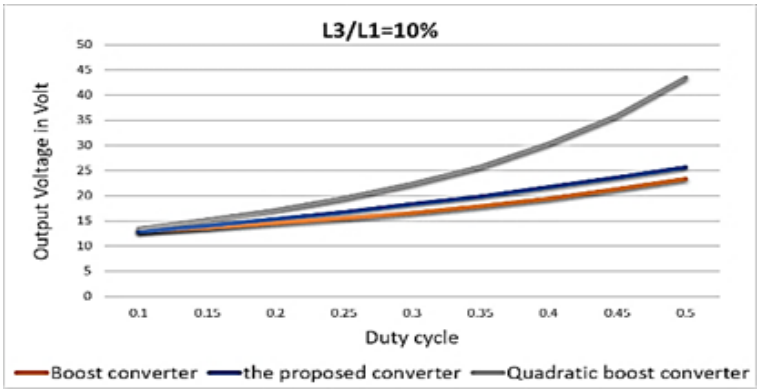
- The auxiliary inductor (L_3) operates in DCM due to its small size, which results in zero current flow through the inductor during one switching cycle. As a result, the bootstrapping diode experiences no reverse recovery current.
- Increasing voltage gain can be achieved by reducing the inductance of the auxiliary inductor to less than 10% of the front-end inductor, but that can increase the ripple of the ICr slightly, even though it still improved and is lesser than the conventional one. For this reason, a compromise between the current ripple and voltage gain is necessary, depending on the requirements of applications.
- Reducing the oscillation in the current and voltage waveforms, which causes due to the switching action of the converter. This oscillation can negatively impact the converter's efficiency, stability, and output voltage accuracy and cause electromagnetic interference that can affect other electronic devices. Furthermore, increasing the stress on components can affect their reliability and longevity.
- Reducing the reverse recovery current of the diodes can have several positive effects on its performance, including reduced power dissipation in the diode, which can improve the efficiency, increase the maximum switching frequency leads to improve the size, cost, and overall performance of the converter, and improve the reliability and lifespan of the diode.
- Reducing the current pass through the main power switch will result in lower conduction losses and lower turn-off losses.

VII. THE RESULTS OF COMPARISON WITH OTHER CONVERTERS

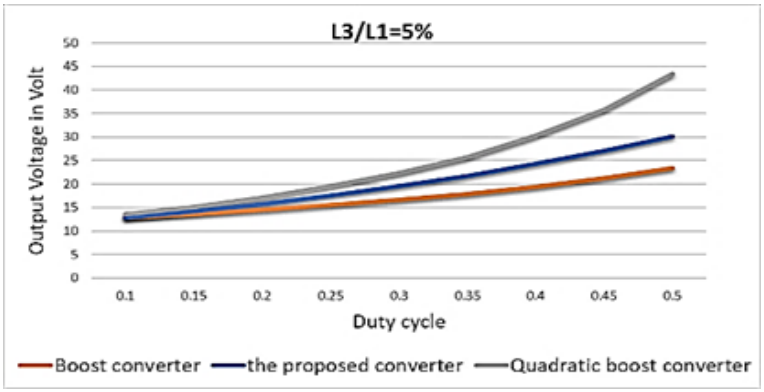
The comparison between three topologies: boost converter, QBC, and the proposed converter is illustrated in Figure 8.

The relationship between the output voltage and duty cycle of these three topologies when the ratio (L_3/L_1) equals 10% and (5%) are illustrated in Figure 8 (a) and (b) respectively.

The relationship between the ICR and duty cycle of these three topologies when the ratio (L_3/L_1) equals 10% and (5%) are illustrated in Figure 9 (a) and (b) respectively.

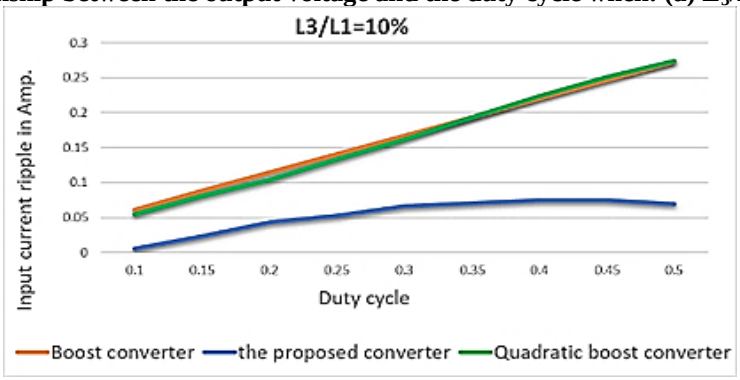


(a)

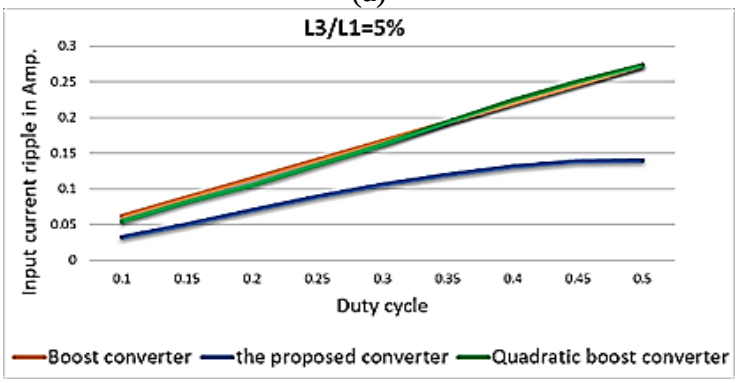


(b)

Figure 8 shows the relationship between the output voltage and the duty cycle when: (a) L_3/L_1 is 10%, (b) L_3/L_1 is 5%.



(a)



(b)

Figure 9 shows the relationship between the the ICR and duty cycle when: (a) L_3/L_1 is 10%, (b) L_3/L_1 is 5%.

In summary, the incorporation of an auxiliary inductor will result in a decrease in both the output voltage and ICR. The level of this reduction is dependent upon two key factors: the duty cycle and the value of the auxiliary inductor.

VIII. CONCLUSION

This paper proposed a modified high-step-up QBC. A series connection of an auxiliary inductor with a bootstrapping diode can achieve an interleaving technique where the ICr has sharing property. The auxiliary inductor plays an essential role in controlling the features of the proposed converter and improving its performance, which includes reducing the reverse recovery problem, having a faster response, and mitigating oscillation in the currents of inductors and voltages of capacitors enhances the stability of the converter in comparison to traditional converters. Since the peak currents passing through all semiconductor components are lowered, the conduction loss has reduced, so the efficiency of the proposed converter is improved. According to the simulation results, the suggested converter reduces current ripples by more than 95%. As a result, the input side of the converter experiences almost no ripple current, which enables it to be used in low-ICR applications such as LED drivers and renewable energy sources.

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