

Design and Implementation of Programmable Multi Stage Decimation Filter For Wireless Communication Receivers

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Abstract

This paper presents, the design of programmable multi stage decimation filter for wireless communication receivers using MATLAB program in the intermediate frequency band up to 150 MHz which will serve the CDMA, WCDM and GSM systems. However, this paper will deal with the designing and investigation of decimation filter in terms of the filter performance in pass band, stop band and adjacent band rejections of the filter. The multi stage decimator produce low computational complexity and error. In addition, relaxation in the specifications of anti aliasing filter in each stage compared to single stage realization. The results obtained shows an important improvements in the filter response compared with conventional design. The proposed decimation filter will enhance the 3G and 4G of communication systems.

Key word- Multi-stage, Decimation Filter, wireless communication, MATLAB, FPGA

تصميم مرشح مختزل متعدد المراحل مبرمج لمستلمة أنظمة الاتصالات اللاسلكية

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الخلاصة :

يقدم هذا البحث تصميم مرشح مختزل متعدد المراحل مبرمج لمستلمة الاتصالات اللاسلكية باستخدام برنامج ماتلاب للحزمة الترددية المتوسطة لغاية 150 ميگاهيرتز للعمل مع منظومات GSM, CDMA, WCDMA لذلك فان هذا البحث سيتناول التصميم والتحقق من اداء الفلتر المختزل في حزمة المرور والتوقف والحد القريب. المختزل متعدد المراحل يمكن ان يقدم تعقيدات حسابية واخطاء قليلة بالاضافة الى تمكن المختزل من العمل بمرومة معهودة في كل مرحلة والتعامل بحرية لمعالجة التموج والتلاسق في الاشارات. النتائج تبين ان المرشح المقترح يحقق تحسن مهم في اداء الفلتر بالمقارنة مع المرشح التقليدي. المرشح المختزل المقترح يمكن ان يعزز أنظمة الاتصالات من الجيل الثالث والرابع.

1. Introduction

Establishment of joint use of a demonstration of digital signals for the transport and storage of the challenges in the field of digital signal processing^[1]. Claims of FIR digital filter, and up / down sampling systems are going on everywhere in the electronic modem harvest. Less complexity of the circuit is at all times the design goal is important because it reduces the cost of industrial^[2]. The ups and downs samples and samples used to modify the sampling rate of the digital signal in multi-rate systems, DSP. Commitment to the conversion rate leads to the manufacture of unwanted signals associated with anti-aliasing and imaging errors. Even some groups candidate should be developed to reduce these errors^[3]Decimation filter is an important part of software defined radio (SDR) or 3G reception on the basis of 4G baseband^[4]. Moreover, the behavior and destruction matched filtering to eliminate adjacent channel and exploitation signal-to-noise ratio (SNR received). Exempts filter is mainly used to convert a string of GSM signal or disappear^[5]. And low-pass filters used usually to reduce the bandwidth of the signal earlier dipping to the sampling rate. The bottom of the samples is essential for the sampling rate adjustment device used to reduce the sampling rate by an integer factor^[6-7]. IF digital technologies can be used to take samples of the IF signal and the implementation of direct and sample rate translation in the digital domain. For the purpose of SDR, because different principles and different segments / bit rates, required an incorrect sample rate conversion to convert a number of samples to an integer multiple of the slide / bit rate for any basic standard Front-end subsystem works in high data rate and the rear end operate at low data rate or the rate of the chip. Front elevation data rate FPGA DSP tasks directed to implement a multi-carrier system. Each channelizer up to digital intermediate frequency, translates into a baseband channel filter and use a multi-stage multi-rate sample rate adjusts to meet Nyquist of selected band. Background processor will operate normally on several slower sample rate streams performing functions such as processing rake and rake adjustment processing, demodulation, turbo decoding, Viterbi decoding^{[8],[9]}.

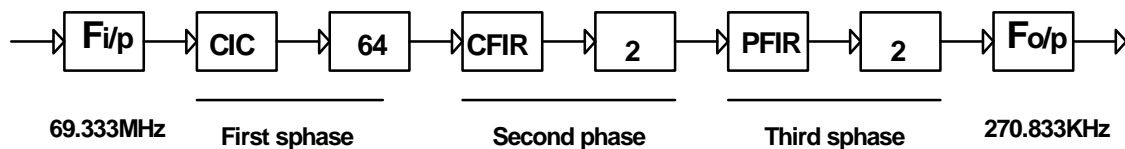
2. Decimation filter model requirements

First, one should make a decision for any class of the structure of the candidate does not have to be used and the band to be on the decimation. For example, in the GSM mode, if required illustrated parts baseband in **Table (1)**^[10].

Table 1: Intermediate frequency range and parts requirement to develop a GSM baseband ^[10]

Input	69.333248MHz
Data	80kHz
Output	270.833kHz
Stop-band frequency	100kHz
Transition band	20kHz
Ripple	-0.03dB
Band refused to neighboring	-25 dB
Stop band essentials	-105 dB

The block diagram shows the practical design decimation filter for the purpose of special drawing rights system in **Figure (1)**. This structure is used to change the IF band GSM mode from 69.333248 MHz to 270.833 kHz in multiple parts. It uses COM (CIC) decimation filter integrated sequentially in the first part to decimate the input signal by a delicate issue. Compensation is limited impulse response (CFIR) filter used in the second part to your family signal via 2 due to high gains founded by CIC filter and provide additional filtering of the incoming signal. Finally, the programmable FIR (PFIR) filter decimated by 2, to form a preferred GSM signal and to provide the necessities of the system.

**Fig. (1): Block diagram process of designing the proposed decimation**

For the provision of the necessities GSM, and the upper structure of the decimation to realize part in conditions of circumstances pass-band/stop-band the response filter to avoid any interference in the channel and reduce the power consumption of the candidate. To achieve the optimal shape for the design of a candidate, has been selected Equiripple linear phase FIR filter to design CFIR and PFIR in the sequence of liquidation because it allows succeed in the response in the form of slash and let the incline in attenuation.

3. The proposed CIC,CFIR, PFIR design filters using M-File.

3.1. The structure of the first phase.

The primary part of the structure of the decimation filter is a CIC decimator filter. Candidate has been selected CIC consists of five stages and the decimation factor of 64 due to high input frequency of the GSM system needs many stages and high decimation factor to the

bottom of the IF frequency conversion towards further processing. To understand and analyze the response recitation CIC, and the M-file and (fvtool) in MATLAB and used to demonstrate the response of this filter. CIC filter response shown in **Figure .(2)** appears in the form $|\text{Sin}x/x|^2$ which gives quick relief with high gain in the preferred range of zero to 80 kHz, which represents baseband signal of GSM. Moreover, not flat frequency response even in the passage of the band.

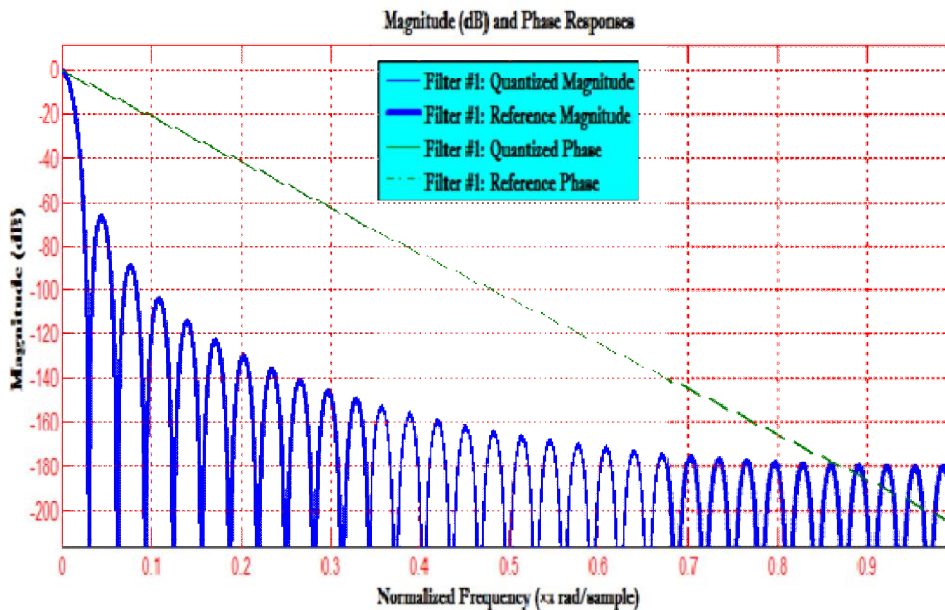


Fig .(2): The five-phase CIC filter response

3.2. The design of the second phase

the designing filters CFIR is in terms of design methods Equiripple with low filter system and error. As a result, the design of linear phase must be aware. To provide this goal, determine the width of the transition for CFIR candidate as short as possible, and therefore can not be the implementation of the system in terms of complexity, and the total width of the transmission decimation filter put on the safe side. As a result, it has been determine the width of the transition to candidate CFIR in the pace normalize in 0.0294π of the rad / sample to improve the design FIR filter. To make sure that the process stays on the safe side, has been selected a bit extreme pass band and stop band ripple of 0.01 dB as public ripple. Has been selected attenuation slope of 60 dB, to give sufficient attenuation of PFIR and thus, avoid spectral replicas as shown in **Figure (4)**.

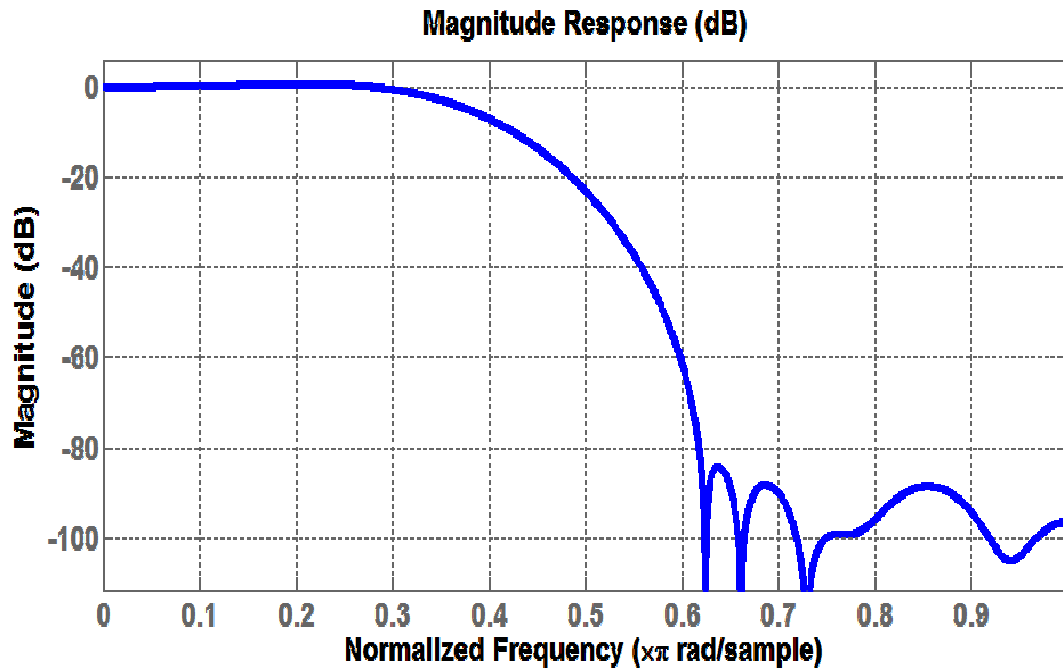


Fig. (4): Second phase CFIR the filter response

To see the first and second phase response in the same graph, Figure 5 clearly shows the response of the filters cascaded pull. The resulting response shows that the candidate CFIR provides maximum attenuation in the band of interest to achieve a flat pass-band, which is opposite to the first phase of the response in order to achieve a balance in sharp relief.

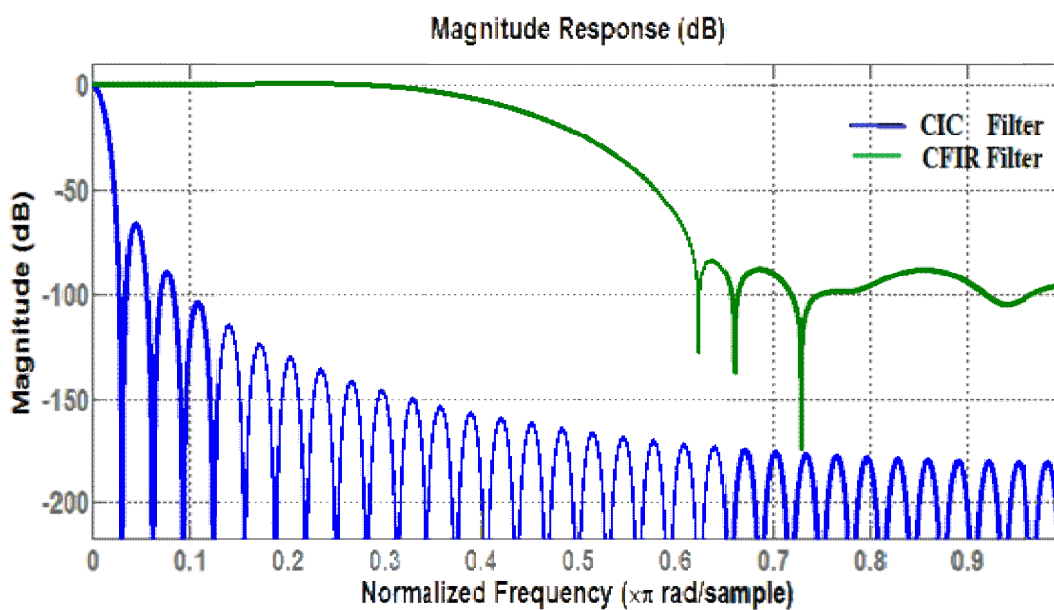


Fig .(5): The response phase CIC and CFIR combined

3.3. The designing of the third phase

To begin with, if one look at the reaction of the first and second stage with a mask GSM frequency as shown in Figure 6, and the resulting response does not provide the exact requirements of the GSM mask in the passage and stop band. However, to meet the requirements of GSM, and the liquidation of the third stage has to provide optimal structure for the third phase (PFIR) candidate.

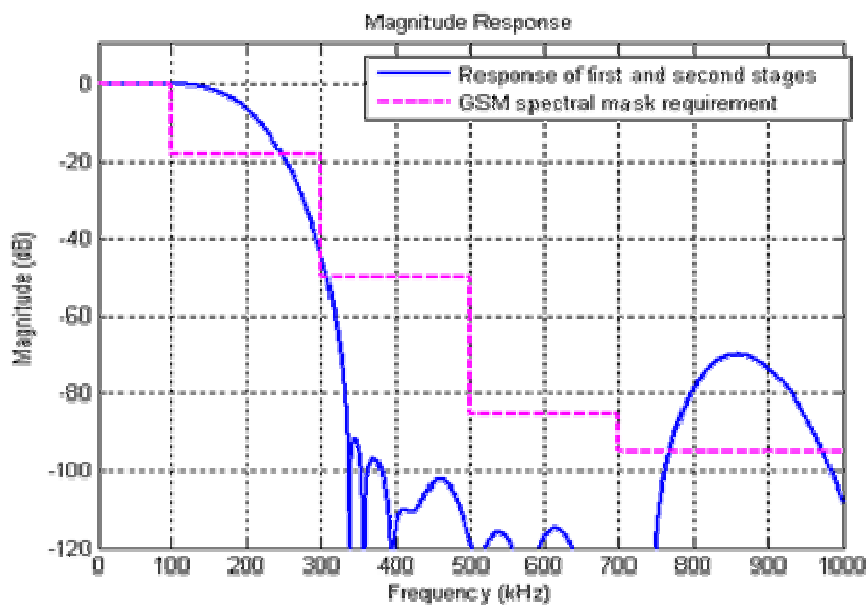


Fig. (6): The first and second phase response with GSM frequency mask.

However, the structure of the third phase of the filter required to provide GSM requirements in terms of frequency and amount of mask error in the pass-band. Thus, it can be optimized mistake by putting a minimum liquidation transactions that reduce the maximum total error is likely. At this time the filter coefficients cooperation plays an important role in reducing error, which is the trade-off between transactions and the error must be achieved to improve the design of the filter. After investigating deeply into the filtering algorithms, the system is to choose a candidate in 65 taps Equiripple the linear phase FIR filter with different weights. Since different weights are included in the structure of the filter, resulting in response appears a PFIR different candidate values stop band attenuation at 100 kHz and 108 kHz. Moreover, weights were identified in the pass band to be greater than the station range of weight by 30 times to improve the adjacent band rejection, as shown in **Figure (7)**.

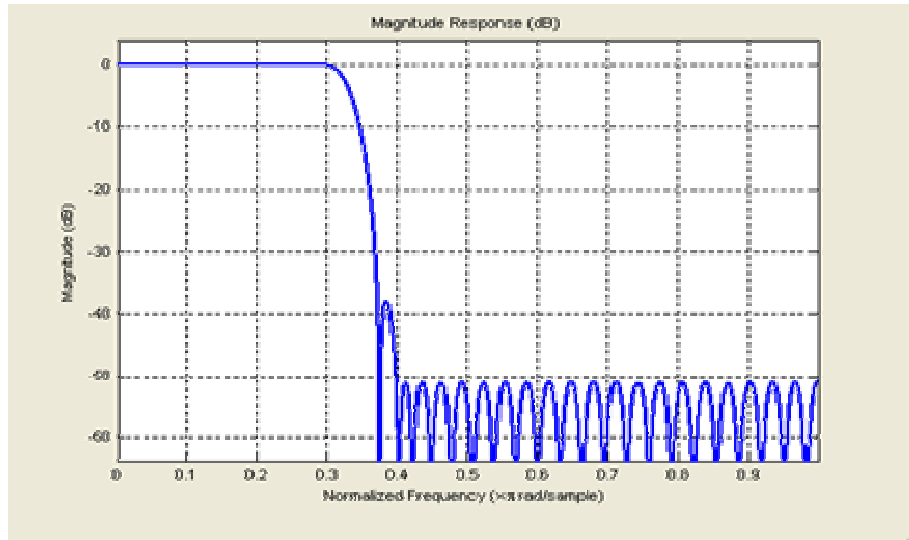


Fig .(7): The different stop-band with third stage response

The three stage response is combined in same graph to show the required specifications is achieved or not as illustrated in **Figure (8)**. One can see three regions of attenuation in a band of interest. In the pass band, and the top of the filter attenuation PFIR equals loss CIC and filter CFIR in part the band stops, and high attenuation of candidate CFIR the lower down CIC attenuation and filter PFIR. In the mind, and high attenuation of the CIC filter pulls down loss CFIR and PFIR filters. Response proposed decimation filter meet the requirements mask GSM, with significant improvements as shown in **Figure (9)**. And illustrated ripple scope of the proposed candidate scrolling in **Figure (10)**. As is clearly shown, not joined a ripple of approximately -0.022 dB. Compared with traditional decimation filter, and the proposed algorithms is to provide about 30% improvement in the ripple which allows to reduce the energy consumption by the implementation of the filter and promotion of 3G and 4G wireless communications system as the objective of this research.

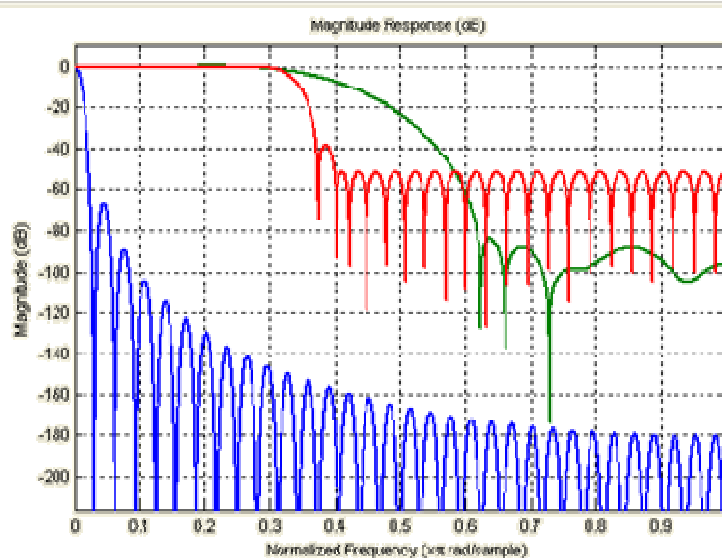


Fig. (8): Three phases combined response.

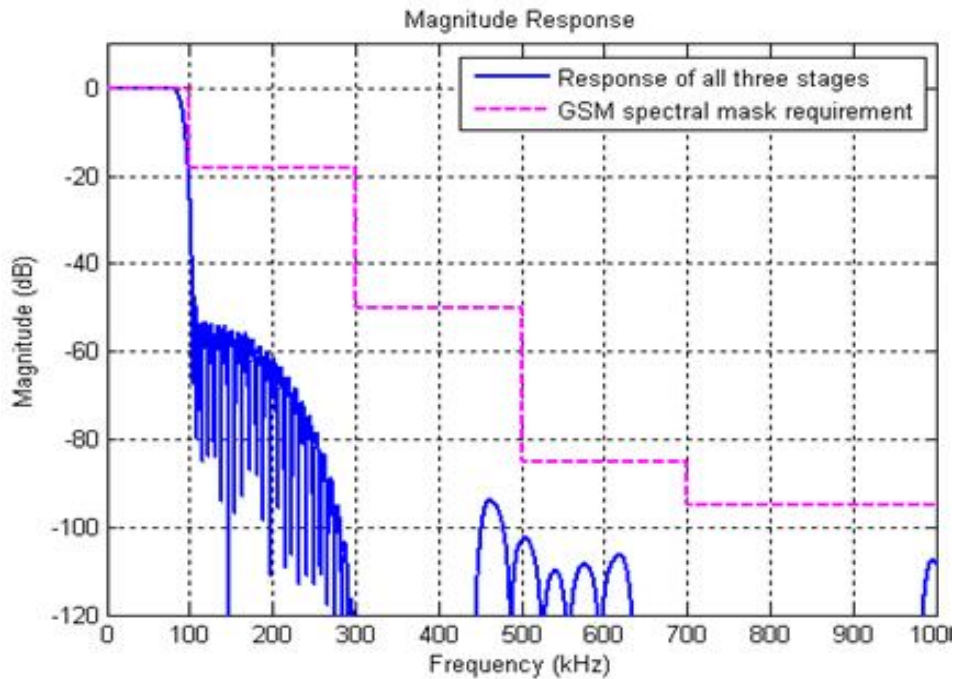


Fig .(9): three phases combined with GSM frequency response mask.

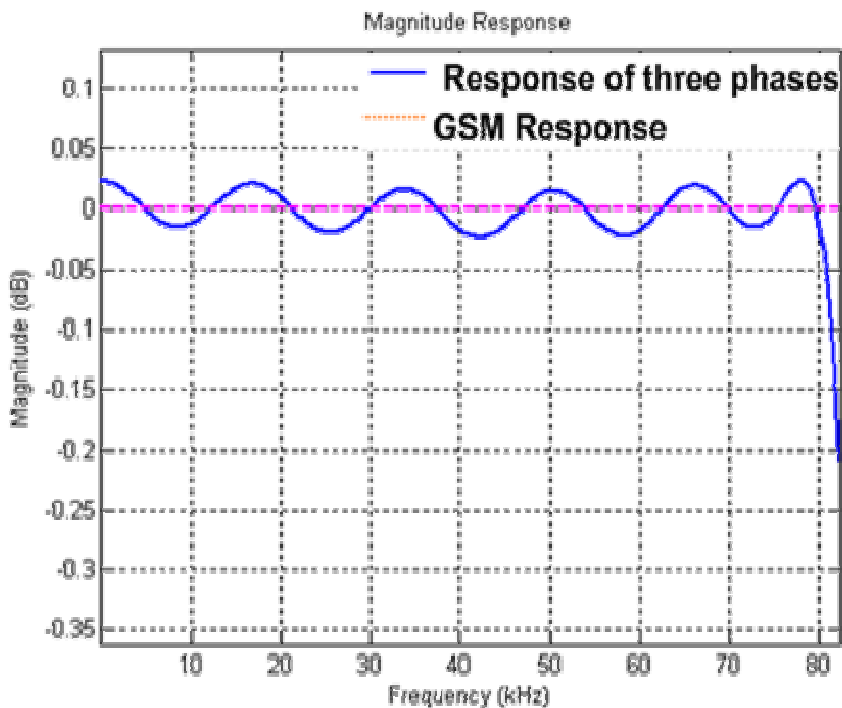


Fig .(10) : Passband ripple

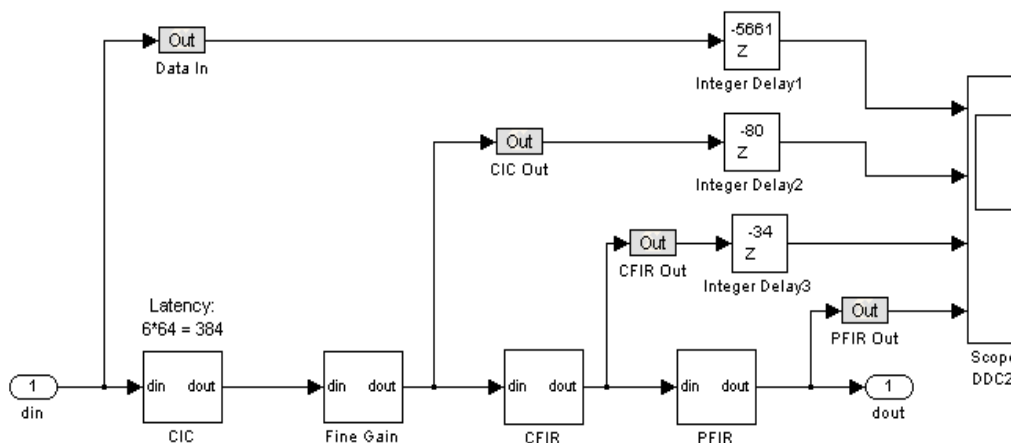
Comparison between the results obtained with the traditional design [9], [10], [11], [12], [13] [14] in terms of the pass band ripple, and rejection of the adjacent band, and blocker requirements of the candidate is illustrated in Table 2. DDC candidate proposed reducing pass band ripple 20% less than conventional candidate, and this development could enhance the ability of the filter to avoid any distortion and error in the wanted signal and reduce energy consumption.

Table 2: Comparison between proposed filter and other filters

PARAMETERS	Douglas 2008	Texas 2009	Proposed 2013	Utilization%
Pass band Ripple	-0.1dB	-0.03dB	-0.022dB	20%
Refused to the next band	-20dB	-25dB	-40dB	15%
Blocker Requirements	--85dB	-105dB	-115dB	10%

4. Decimation Filter Implementation

The combined decimation filter structure contains CIC, CFIR, and PFIR, which are connected in the System Generator to verify the filter performance with the MATLAB design. The filter structure is shown in **Figure (11)**.

**Fig .(11): Decimation filter design using system generator**

The combined of three stage filters response in the System Generator is shown in **Figure (12)**. The combination of chirp and sinusoidal signals in fixed point value as input of the Decimator filter and the filter responses at each consecutive stage in the Decimator filter chain is synchronized. This is achieved by imposing delays upon the CFIR filtered signal, normalized CIC filtered signal, and mixed signal at $(4096 + 256) = 4352$, $4352 + (640 + 128) = 5120$, and $5120 + (157 + 384) = 5661$ unit sample time, respectively, where 1 unit sample time $= (69.333248 \times 10^6)^{-1} \text{ ns} = 14.423095 \text{ ns}$. The first and second terms in parentheses are the respective group and processing delays of the PFIR, CFIR, and CIC filters in the proposed DSP-based decimator.

The decimator response resembles moreover the upper or the lower envelope of the mixed signal while it is down-sampled by 256. Down-sampling is obtained since the envelope is extracted first by the CIC filter with a decimation factor of 64 and normalization gain of

2^{30} , subsequently by the CFIR filter with a down sampler of 2, and finally by PFIR with a down sampler of 2. In addition, the peak values of the decimator filter response maintained at ± 0.5 is equal to that of the envelope of the mixed signal. Though, the sample rate of the decimator filter response is 256 times lower than the sampling frequency of 69.333248 MHz.

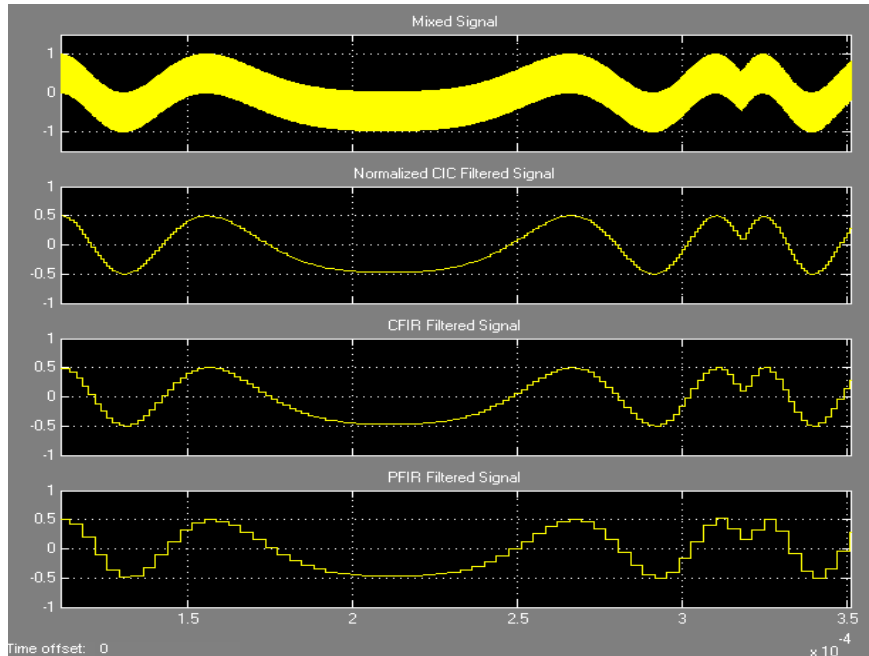


Fig .(12): Three stage Decimation filter response

5. Decimator VHDL Code Generation

To generate the VHDL code of proposed decimator, the FDATATool option in system generator is used to verify the floating point design with fixed point design using ModelSim software. The command line with FDATATool could be used to produce the VHDL or Verilog code and test bench of ModelSim. **Figure (13)** show the Co-Sim in ModelSim of three decimator stages. The verification of HDL code as Simulink model with reference decimator produce the waveforms of tow filters and the difference between them as show in Figure 14. The two signal paths represent simulink behavioral model and VHDL code for reference filter respectively. The difference between the fixed point design and floating point decimator response is less than 2×10^{-4} . This is mainly because of the quantization errors resulting from the limited number of bits representing the numerical values used in the arithmetic functions such as multiplication and summation in filtering process. In this case, the inputs and outputs of the CFIR and PFIR filters are set to fixed point values of 16 bits and 14^{th} binary point. Nevertheless, the difference value below 2×10^{-4} can still be accepted as valid accuracy, as long as the proposed decimator response closely resembles the ideal decimator response and does not jeopardize the performance of the subsequent processing after decimator stages.

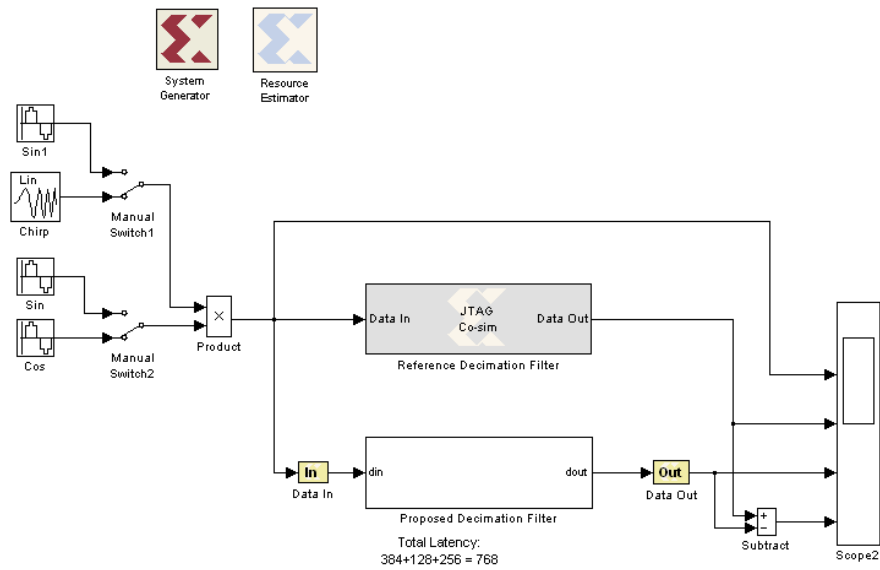


Fig .(13): Decimation filter implementation using Co-Sim

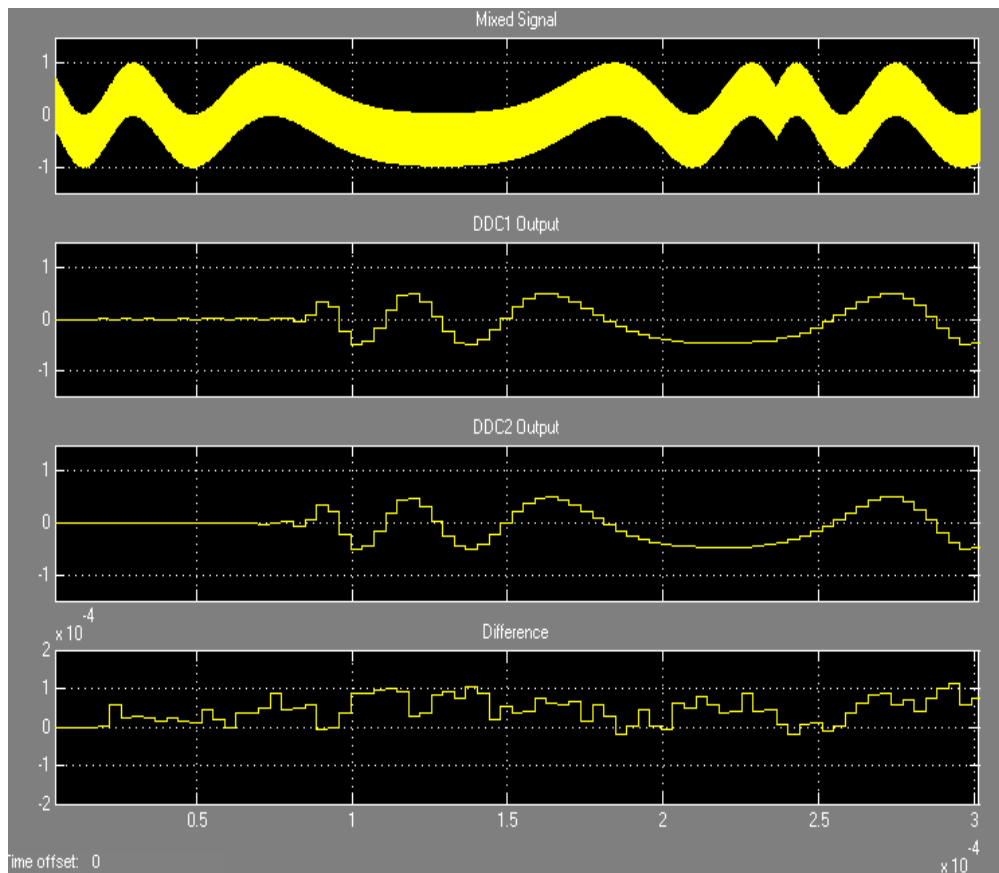


Fig .(14): Decimation filter implementation results

6. Conclusions

In this paper urbanized decimation filter algorithm and promotion of the GSM system and all 4G applications specific radio programs. The proposed algorithm and techniques that are used in this paper to reduce the ripple in the pass-band filter response of the three stages of the decimation filter. The decimation filter design and simulation through programs MATLAB of Mathworks and the generator of XILINX system. To achieve this technique has been used a couple of filters, they are, compensation is limited motivation response (CFIR) the limited programming candidate impulse response (PFIR) filter. However, these techniques are promising, and also the development of a sample conversion rate of GSM and the new generation of wireless communication system.

7. References

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