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A PROPOSED METHOD FOR EVALUATING THE OPTIMUM LOAD IMPEDANCE IN NEGATIVE RESISTANCE RF OSCILLATORS

*Firas Mohammed Ali Al-Raie

Assistant Lecturer, Department of Electrical Engineering, University of Technology, Baghdad, Iraq.

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Abstract: Negative resistance radio frequency (RF) and microwave oscillators are widely used in modern wireless communication systems. In these circuits, the active device is imposed to work in the unstable region in order to present a negative resistance at its input or output port. This paper discusses the effect of the load impedance on the large signal behavior of the oscillator circuit throughout a design process of a practical 900 MHz RF oscillator circuit. New closed-form expressions for the optimum load resistance and reactance that maximize the output power have been derived analytically in terms of the transistor Z-parameters, and a design criterion for the RF oscillator is proposed based on the evaluated optimum load impedance. It has been shown through computer simulation that the optimum load resistance and reactance for maximum output power are dependent on each other. Furthermore, it has been verified that the optimum load impedance for maximum negative resistance differs slightly from its value required for maximum output power and this deviation increases with the increase in the RF power level. The designed oscillator circuit has been implemented and tested successfully.

Keywords: *Negative Resistance Oscillators, Large-Signal S-parameters, Microwave CAD, Nonlinear RF Circuits.*

طريقة مقترحة لإيجاد ممانعة الحمل المثلى في المذبذبات الراديوية ذات المقاومة السالبة

الخلاصة: تستخدم المذبذبات الراديوية ذات المقاومة السالبة بشكل واسع في أنظمة الاتصالات اللاسلكية الحديثة. في هذه الدوائر يتم تشغيل العنصر الفعال (الترانزستور) في المنطقة غير المستقرة لكي يُبدي مقاومة سالبة في منفذ الدخل أو الخرج. يناقش هذا البحث تأثير ممانعة الحمل على أداء المذبذبات الراديوية في حالة الإشارات عالية السعة وذلك من خلال عملية تصميم لدائرة مذبذب عملية تعمل بالتردد 900 MHz. وقد تم اشتقاق معادلات جديدة بصيغة مغلقة لإيجاد ممانعة الحمل المثلى لدائرة المذبذب بدلالة معاملات الممانعة للترانزستور، وتم اقتراح طريقة تصميم للمذبذب الراديوي بالاعتماد على ممانعة الحمل المثلى المخمّنة.وقد لوحظ خلال عملية المحاكاة بالحاسوب بأن مقاومة الحمل المثلى ومفاعلة الحمل المثلى تعتمدان على بعضهما البعض. كما لوحظ ايضا من عملية المحاكاة بأن ممانعة الحمل المثلى اللازمة لتحقيق أقصى مقاومة سالبة تختلف قليلا عن قيمتها اللازمة لتحقيق أقصى قدرة خرج، ويزداد هذا التفاوت عند زيادة مستوى قدرة الإشارة الخارجة. وقد تم تنفيذ واختبار دائرة المذبذب المصممة بنجاح.

**E-mail:*30204@uotechnology.edu.iq

1. Introduction

In negative resistance oscillators, the RF transistor is characterized as a one-port network by its input impedance Z_{in} connected with a resonator of impedance Z_r as shown in Fig. 1. The circuit can oscillate if the loss in the resonator is absorbed by the negative input resistance of the active device.

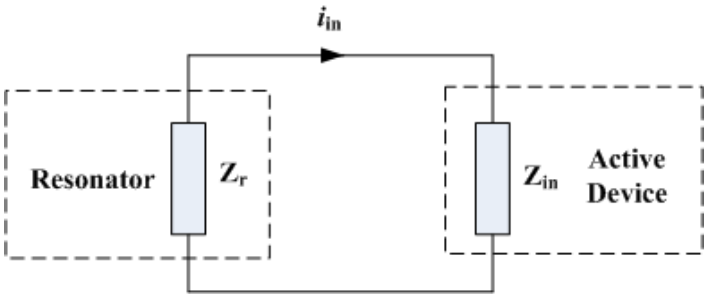

Figure 1. A Simplified Topology of the Negative Resistance Oscillator

The loop equation of the circuit in Fig. 1 is written as:

$$i_{in}.(Z_{in} + Z_r) = 0 \quad (1)$$

Equation (1) can be satisfied if either $i_{in} = 0$ or $Z_{in}+Z_r = 0$. For an existing current signal at the input of the active device, i_{in} should not equal to zero, and therefore:

$$Z_{in} + Z_r = 0 \quad (2)$$

This means that:

$$Z_r = -Z_{in} \quad (3)$$

Or,

$$X_r = -X_{in} \quad (4.1)$$

$$R_r = -R_{in} \quad (4.2)$$

So, at the oscillation frequency, the reactance of the resonator should equal the input reactance of the active device in magnitude but with opposite sign. Similarly, the resistances of the resonator and the active device are equal in magnitude and differ in sign. But since the resonator is a passive circuit then its resistance is positive in all conditions and therefore the active device should present a negative resistance at the oscillation frequency.

The input resistance and reactance of the active device are not solely functions of the frequency but vary also with the power level at the input port of the active device.

So, the large signal magnitude of R_{in} is different from its small signal value due to the inherent nonlinearities in the active device. This resistance usually decreases with power level in most practical RF devices as shown in Fig. 2. In this sketch, the value of the small signal input resistance equals to $-R_o$, while P_{in} represents the available power at the input port, and P_{th} is the threshold input power at which the input large signal device resistance deviates from its small signal value.

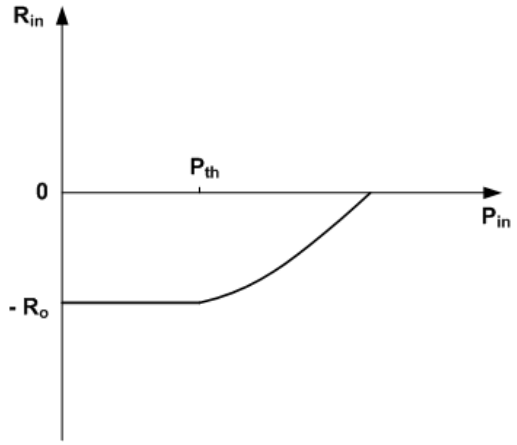

Figure 2. Typical Variation of the Negative Input Resistance with Power Level

So, the necessary condition for oscillation is to make R_r less than the magnitude of the small signal input resistance:

$$R_r < |R_o| \quad (5)$$

The resonator resistance R_r is usually taken equal to $|R_o|/3$ as a practical rule of thumb [1].

2. Literature Review

The foundations of negative resistance microwave oscillators were established by Kurokawa's work through developing the steady state oscillation condition of the circuit [2]. Further attempts involved the design of RF oscillators based on the large signal S-parameters to maximize the output power and efficiency [3-5]. Analytic derivation of the large signal S-parameters in terms of the input and output device terminal voltage amplitudes was carried out [6]. These equations are formulated systematically as a root finder computer algorithm to determine the circuit elements for maximum oscillator's output power.

A technique for the evaluation of different oscillator circuit topologies for optimized output power was carried out depending on the measurements of an optimized power amplifier [7]. This technique takes benefits from the ease of power amplifier measurements when compared with oscillator's measurement. A simplified quasi-linear design technique for gallium-arsenide metal semiconductor field effect transistor (GaAs

MESFET) oscillators was also developed [8]. In this approach the generated oscillator's power is derived in terms of the gate and drain RF voltages. The oscillator circuit elements are derived to maximize the generated power under the limiting conditions of the terminal voltage amplitudes.

Another analytical approach to the design of microwave oscillators with output power prediction was documented [9]. This design method is mainly concerned with the calculation of the oscillator's network elements using small-signal RF device two-port parameters as the starting point. The oscillator output power is estimated with the aid of the DC bias voltage and current. A linearized design method that maximizes the added power in a two-port oscillator was verified [10]. In this technique, different network topologies are analyzed for the sake of optimized output power with the RF device modeled through its small-signal parameters.

Andrei Grebennikov proved analytically that maximum output power of the oscillator can be obtained by maximizing the magnitude of the negative real part of the output impedance for the RF device, and derived expressions for determining the optimum circuit elements based on this assumption [11]. This technique was applied both to bipolar junction transistor (BJT) [12] and field effect transistor (FET) [13] oscillator circuits. In a recent study, it has been shown that increasing the magnitude of the negative output resistance of the RF device does not always lead to greater output power [14].

3. Extension of the Region of Instability in RF Oscillators

In negative resistance oscillators, the circuit can oscillate if the real part of the input or output impedance of the active device is negative. This can happen if the device is potentially unstable at the desired oscillation frequency and power level. The stability of the active device can be tested by evaluating the stability factor, μ, at the desired frequency [15]:

$$\mu = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta . S_{22}^*| + |S_{12} S_{21}|} \qquad (6)$$

where S_{ij} are the S-parameters of the RF transistor, and $\Delta = S_{11}.S_{22}\text{-}S_{21}.S_{12}$.

When μ is less than unity, the device is said to be potentially unstable and oscillation is possible. Otherwise, the device is unconditionally stable and oscillation is not permissible without some sort of positive feedback. If the RF transistor is potentially unstable at the desired frequency, a stability circle can be sketched on the Smith chart using an appropriate RF circuit simulator to select an appropriate load reflection coefficient Γ_L on the unstable region to make $|\Gamma_{in}|$ greater than 1 (or R_{in} less than zero), which is a necessity for oscillation.

The oscillation susceptibility of the RF transistor can be increased by connecting it in common base configuration. Furthermore, the instability region of the common base configuration can further be extended by adding additional series or parallel feedback

elements. In Fig. 3(a), an inductor is inserted in the base terminal to constitute a series feedback network [16]. Additional capacitor is added as shown in Fig. 3(b) to control the emitter-base nonlinear internal capacitance of the transistor [1]. In Fig. 3(c) parallel feedback is formed by a voltage divider capacitance network [16]. The elements of these configurations can be calculated either analytically using a simplified equivalent circuit model for the RF device, or can be optimized using a microwave CAD simulator. To select a certain configuration, the load stability circle of the RF transistor is first sketched on the Smith chart to view the unstable region for all possible load reflection coefficient values. If the stability circle does not cover a considerable part of the Smith chart, then one of the configurations presented in Fig. 3 should be selected to extend the unstable region.

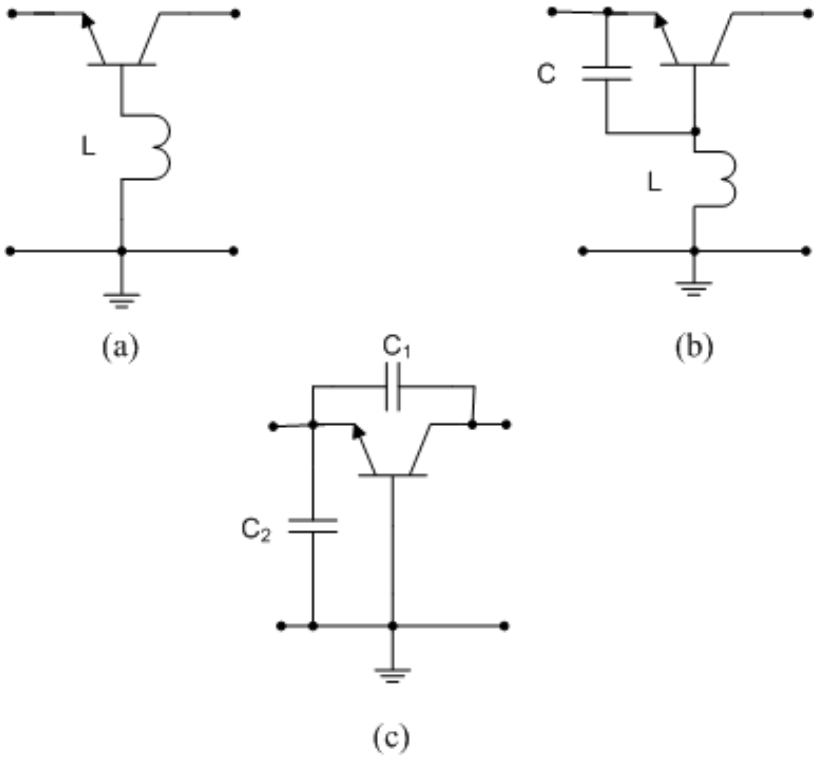

Figure 3. Three Common Base Configurations for Increasing the Negative Input Resistance of the RF Transistor

4. Estimation of the Optimum Load Impedance

In this section, the equations for estimating the optimum load resistance and reactance of the oscillator are derived analytically in terms of the transistor Z-parameters. Optimum load impedance can be selected to maximize the magnitude of the negative input resistance of the oscillator [11]. Fig. 4 presents a simplified block diagram of the negative resistance oscillator [17]. The task is to determine $Z_L=R_L+jX_L$ required to make $|\Gamma_{in}|$ or $|R_{in}|$ maximum. This can be done by finding an equation for $|\Gamma_{in}|$ or R_{in} and partial differentiating it with respect to R_L and X_L respectively after

characterizing the active device with its Y or Z parameters at the required frequency. The active device can also be described with its small-signal hybrid-π high frequency model, and the input impedance looking into the emitter is derived in terms of the RF transistor internal physical parameters.

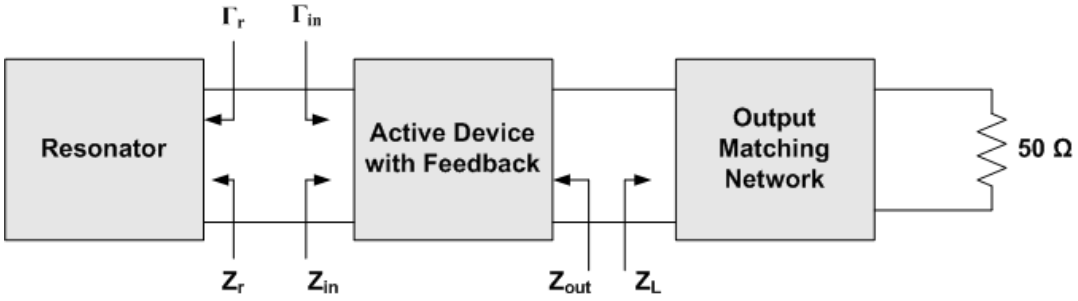

Figure 4. Block Diagram of the Negative Resistance RF Oscillator

From two-port network theory, if the device is described in terms of its Z-parameters then the input impedance can be expressed as:

$$Z_{in} = Z_{11} - \frac{Z_{12}.Z_{21}}{Z_{22} + Z_L} \quad (7)$$

Or,

$$Z_{in} = \frac{Z_{11}.Z_L + \Delta_z}{Z_{22} + Z_L} \quad (8)$$

where:

$$\Delta_z = Z_{11}.Z_{22} - Z_{12}.Z_{21} \quad (9)$$

Equation (8) can be re-written as:

$$Z_{in} = \frac{(R_{11} + jX_{11})(R_L + jX_L) + (R_{11} + jX_{11})(R_{22} + jX_{22}) - (R_{12} + jX_{12})(R_{21} + jX_{21})}{R_{22} + jX_{22} + R_L + jX_L} \quad (10)$$

where$Z_{ij}=R_{ij}+X_{ij}$ are the Z-parameters of the RF transistor at the desired frequency, and $Z_L=R_L+jX_L$ is the load impedance.
Equation (10) should be re-arranged to split the real and imaginary parts where:

$$R_{in} = Re[Z_{in}] \quad (11.1)$$

$$X_{in} = Im[Z_{in}] \quad (11.2)$$

Equation (11.1) can be partially differentiated with respect to R_L and X_L respectively to get the optimum load impedance for maximum negative resistance at the input port:

$$\frac{\partial R_{in}}{\partial R_L} = 0 \tag{12.1}$$

$$\frac{\partial R_{in}}{\partial X_L} = 0 \tag{12.2}$$

In order to differentiate equation (11.1) with respect to R_L, it can be re-written in the form:

$$R_{in} = \frac{N_1}{D_1} \tag{13}$$

The denominator of equation (13) is given by:

$$D_1 = (R_{22} + R_L)^2 + (X_{22} + X_L)^2 \tag{14}$$

and the numerator is arranged as:

$$N_1 = 2\,R_{11}R_{22}R_L + R_{11}{R_L}^2 + X_{12}X_{21}R_L - R_{12}R_{21}R_L + A_1 \tag{15}$$

whereA_1 is given by:

$$A_1 = R_{11}{R_{22}}^2 - R_{12}R_{21}R_{22} + 2R_{11}X_{22}X_L + R_{11}{X_{22}}^2 + R_{11}{X_L}^2 - R_{12}X_{21}X_{22} - R_{12}X_{21}X_L - R_{21}X_{12}X_{22} - R_{21}X_{12}X_L + R_{22}X_{12}X_{21} \tag{16}$$

Applying equation (12.1) and rearranging gives:

$$R_{L(opt)} = \frac{-\alpha_2 + \sqrt{{\alpha_2}^2 - 4\alpha_1\alpha_3}}{2\alpha_1} \tag{17}$$

where:

$$\alpha_1 = 2R_{11}R_{22} + 2R_{12}R_{21} - 2X_{12}X_{21} + A_3 \tag{18}$$

$$\alpha_2 = 2R_{12}R_{21}R_{22} - 4R_{11}{R_{22}}^2 - 2R_{22}X_{12}X_{21} + 2R_{11}A_2 + 2R_{22}A_3 - 2A_1 \tag{19}$$

$$\alpha_3 = A_2A_3 - 2R_{22}A_1 \quad (20)$$

$$A_2 = {R_{22}}^2 + {X_{22}}^2 + 2X_{22}X_L + {X_L}^2 \quad (21)$$

$$A_3 = 2R_{11}R_{22} - R_{12}R_{21} + X_{12}X_{21} \quad (22)$$

Equation (17) is derived in terms of the transistor Z-parameters and the load reactance X_L.

Similarly, in order to differentiate equation (11.1) with respect to X_L, it can be re-written in the form:

$$R_{in} = \frac{N_2}{D_2} \quad (23)$$

The denominator of equation (23) is given by:

$$D_2 = (R_{22} + R_L)^2 + (X_{22} + X_L)^2 \quad (24)$$

and the numerator is arranged as:

$$N_2 = 2\,R_{11}X_{22}X_L + R_{11}{X_L}^2 - R_{12}X_{21}X_L - R_{21}X_{12}X_L + B_1 \quad (25)$$

whereB_1 is given by:

$$B_1 = 2R_{11}R_{22}R_L + R_{11}{R_{22}}^2 + R_{11}{R_L}^2 - R_{12}R_{21}R_{22} - R_{12}R_{21}R_L - R_{12}X_{21}X_{22} - R_{21}X_{12}X_{22} + R_{22}X_{12}X_{21} + R_LX_{12}X_{21} \quad (26)$$

Applying equation (12.2) and rearranging leads to:

$$X_{L(opt)} = \frac{-\beta_2 + \sqrt{{\beta_2}^2 - 4\beta_1\beta_3}}{2\beta_1} \quad (27)$$

where:

$$\beta_1 = 2R_{12}X_{21} - 2R_{11}X_{22} - 2R_{21}X_{12} + B_3 \quad (28)$$

$$\beta_2 = 2R_{11}B_2 - 4R_{11}{X_{22}}^2 + 2R_{12}X_{21}X_{22} + 2R_{21}X_{12}X_{22} + 2X_{22}B_3 - 2B_1 \quad (29)$$

$$\beta_3 = B_2 B_3 - 2B_1 X_{22} \quad (30)$$

$$B_2 = {R_{22}}^2 + 2R_{22}R_L + {R_L}^2 + {X_{22}}^2 \quad (31)$$

$$B_3 = 2R_{11}X_{22} - R_{12}X_{21} - R_{21}X_{12} \quad (32)$$

Since R_{in} is a function of signal level as depicted in Fig. 2, the optimum load resistance $R_{L(opt)}$ and optimum load reactance $X_{L(opt)}$ may also vary with power level. $R_{L(opt)}$ and $X_{L(opt)}$ can also be found from large signal simulation of the circuit at the desired oscillator's power level and frequency using the non-linear model of the transistor to generate a family of curves for R_{in}, $|\Gamma_{in}|$, power gain, and output power as functions of both R_L and X_L. A compromise is to be done for important oscillator performance characteristics such as high output power, low harmonic distortion, minimal stability factor, and high resonator's quality factor when selecting R_L and X_L from the generated curves.

5. Design Strategy

The design strategy of the RF/microwave oscillator can be summarized through the following steps:

1. Select a suitable RF transistor to oscillate at the desired frequency. The maximum frequency of oscillation, f_{max}, for the transistor should be greater than the desired oscillation frequency. The maximum frequency of oscillation represents the frequency at which the maximum power gain of the transistor drops to 0 dB.Low cost BJTs are usually used for frequencies below 1 GHz. However, above 1 GHz gallium-arsenide metal semiconductor field effect transistors (GaAs MESFETs) or silicon-germanium hetero-junction bipolar transistors (SiGe HBTs) give superior performance characteristics [18].
2. Perform DC simulation to sketch the input and output characteristics of the RF transistor in order to select a suitable Q-point. Use the non-linear SPICE model of the RF device in the simulation process. Determine the transistor configuration and design the bias network.
3. Perform large-signal S-parameter simulation by tracing the transistor S-parameter variation with input signal power level at the desired frequency. This simulation process is useful in viewing the threshold power level at which the large signal S-parameters deviate from their small signal counterparts.
4. Test the stability factor of the amplifier (Equation 6), and sketch the output stability circle at the desired frequency. If the circuit is stable, or the instability region is to be extended, series or parallel feedback elements can be inserted for such a task.
5. Simulate the circuit using large-signal S-parameter technique at the desired frequency and a specified power level in the input port with R_L and X_L as sweeping variables. Display R_{in}, $|\Gamma_{in}|$, power gain, and output power against R_L with X_L as a

parameter. From the generated curves, select an optimum value of R_L and X_L for a better compromise between the performance parameters of the circuit. A initial estimation of $R_{L(opt)}$ and $X_{L(opt)}$ can be evaluated from equations (17) and (27) based on the small-signal Z-parameters of the RF device.

6. Design an output matching network to transform the 50 Ω system impedance into the optimum load impedance at the transistor output as depicted in Fig. 4.
7. Simulate the circuit using the harmonic balance or large-signal S-parameter technique to display the variation of device input impedance with input power level. Determine the input impedance (R_{in} and X_{in}) for the required output power level and linearity. The resonator impedance Z_r is found from equation (3).
8. Synthesize the resonator network to present Z_r at the oscillator's input and simulate the oscillator circuit to test its performance characteristics.

6. Design of a 900 MHz Oscillator Circuit

In order to test the effect of the load impedance on the large signal behavior of the RF oscillator, an oscillator circuit is to be designed and implemented at the 900 MHz mobile communication band (GSM-900). The design objective is to achieve an output power level of about +10 dBm at an oscillation frequency of 900 MHz. Throughout the simulation process of the circuit, some concluding remarks are extracted concerning the evaluation of the optimum load impedance.

6.1. RF Transistor Selection and Bias Circuit Design

The low cost BJT RF transistor BFR91 has been selected for this design. This transistor has a unity gain-bandwidth frequency, f_T, of 5 GHz, typical power gain of 10 dB at 1 GHz, and a minimum noise figure of 2.5 dB at 1 GHz. The transistor is to be connected in common base configuration with a bias point of I_C= 10 mA, and V_{CE}= 5 V. The selected Q-point represents a compromise between low noise figure and high gain characteristic. The microwave computer program *Advanced Design System* (ADS 2009) has been utilized in the simulation process for this oscillator. The SPICEGummel-Poon large-signal model of the BFR91 transistor is defined from the RF transistor library of ADS. For an emitter current of 10 mA, the measured base-emitter voltage is 0.78 V, and the measured DC current gain of the transistor, h_{FE}, is 70.

Fig. 5 presents a common base (CB) voltage-divider bias circuit. This bias circuit is designed to hold the Q-point of the transistor against variations in device internal parameters, and is isolated from the RF circuit via two RF chokes, RFC1 and RFC2, while C_b is a bypass capacitor for resistors R_1 and R_2.

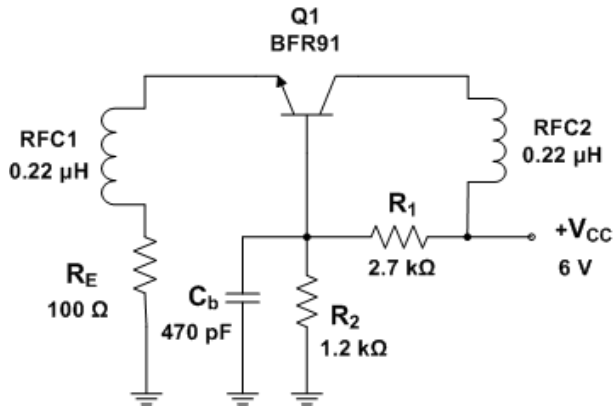

Figure 5. The Bias Circuit for the Common Base Oscillator

6.2. Test of Device Instability

A small signal S-parameter test for the active device can be carried out to view the load stability circle at the desired oscillation frequency. This is helpful to check if the active device requires additional feedback to present negative resistance at the input.

Fig. 6 presents the load stability circle sketched on the Smith chart, which encircles the center point of the chart. All values of Z_L (or Γ_L) inside the load stability circle give negative resistance at the input port which is necessary to bring the circuit into oscillation. It is clear also from this sketch that the stability circle covers a large part of the upper half of the Smith chart which means that X_L should be taken as inductive reactance to sustain oscillation. The stability factor μ equals to -0.207, and the input resistance R_{in} = - 0.782 Ω for Z_L = 50 Ω.

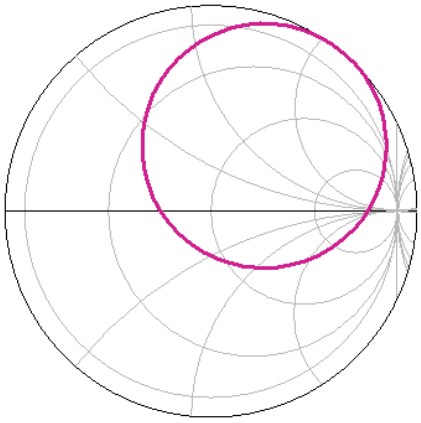

Figure 6. Load Stability Circle on the Smith Chart.

6.3. Large Signal S-parameter Simulation

Large signal S-parameter evaluation can give an indication about the input power level at which these parameters deviate from their small signal values. This is useful in determining the required power level of the input port at the oscillation point. Fig. 7

presents the simulation test setup for large signal S-parameters. In this simulation, the input signal power is swept from -20 dBm up to +10 dBm at a frequency of 900 MHz.

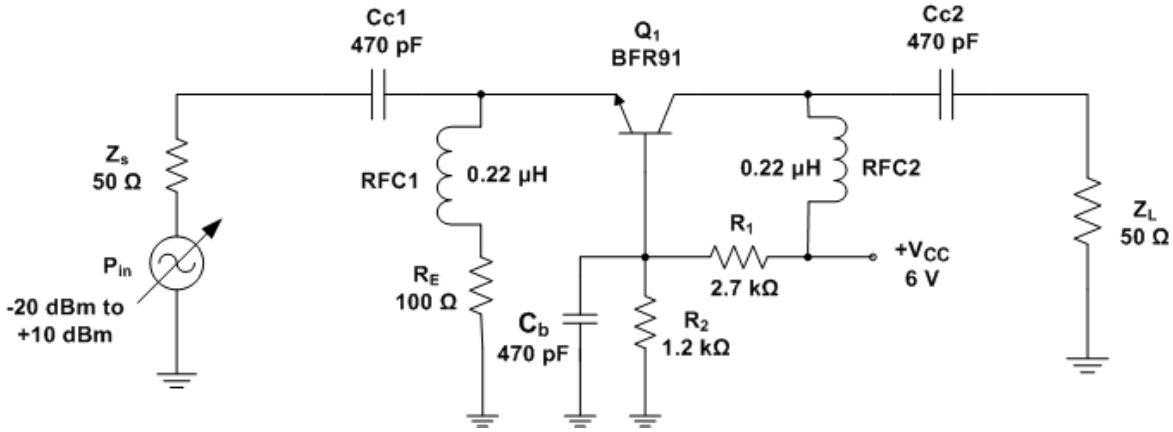

Figure 7. Simulation Test-Setup for the Large Signal S-parameters

Fig. 8 shows the variation of the magnitude of the forward transmission parameter S_{21} with signal power level, while Fig. 9 presents the magnitude of S_{11}versus input power. It is noticed that the large signal S-parameters change after an input signal level of -5 dBm approximately. It is also clear from Fig. 9 that the 1-dB gain compression point for S_{21} occurs when P_{in} = 0 dBm, while the magnitude of S_{11} falls below 1 at P_{in} = -3 dBm. This means that the circuit might be brought out of oscillation for large signal levels when Z_L = 50 Ω. To overcome this problem, Z_L should be selected to maximize the magnitude of the input reflection coefficient, or to make the magnitude of the negative input resistance quite large.

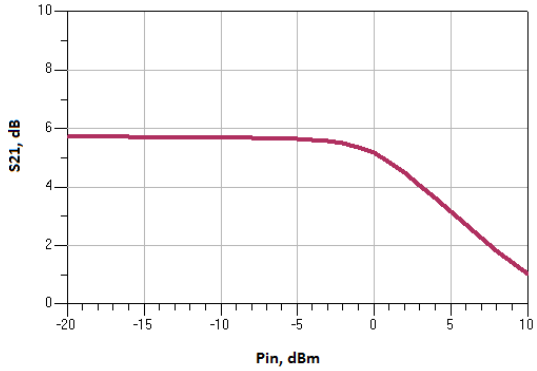

Figure 8. Variation of $S_{21}$with Input Power

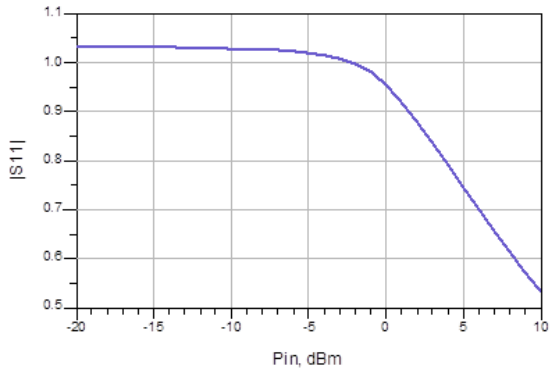

Figure 9. Variation of $|S_{11}|$ with Input Power

6.4. Computer Evaluation of the Optimum Load Impedance

Fig. 10 illustrates a large-signal simulation setup to view the effect of $Z_L$on R_{in}. The RF transistor is characterized with its nonlinear SPICE model, and the large signal scattering parameters are evaluated for a certain power level (-3 dBm) at the input port. At this power level, the device large signal parameters fall below their small signal values.

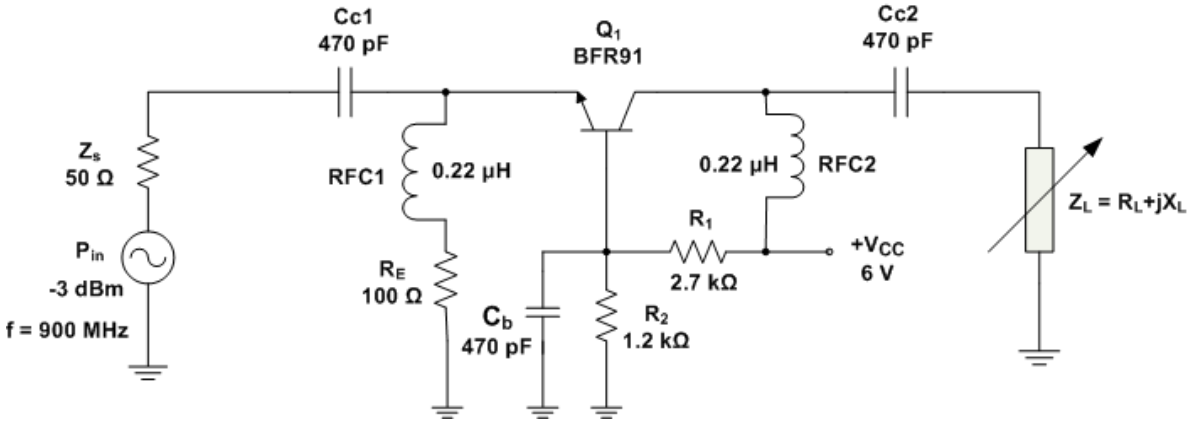

Figure 10. Simulation Setup for Evaluating the Optimum Load Impedance

Fig. 11 presents the variation of the input resistance with R_L for three values of X_L when the available power at the input is -3dBm. It is seen from this sketch that the optimum value of R_L for maximum negative resistance differs in the three cases of X_L. For example when X_L = 150 Ω, the optimum value of R_L is about 80 Ω, and becomes 120 Ω when X_L = 100 Ω, and reaches to 150 Ω when X_L = 50 Ω. This means that $R_{L(opt)}$ is a function of X_L in addition to the large signal device parameters.

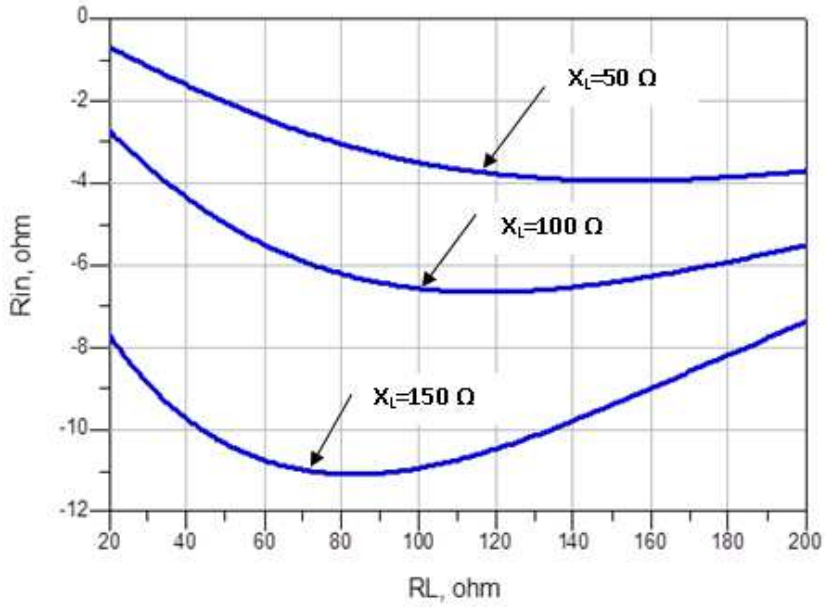

Figure 11. Variation of R_{in} against R_L with X_L as a Parameter

Table 1 presents a comparison between the simulated optimum load resistance values for P_{in} = -3 dBm and the calculated values obtained from equation (17). The calculated values are based on the small-signal Z-parameters of the RF transistor at the desired oscillation frequency (900 MHz), where Z_{11}=5.27+j22.866 Ω,

Z_{12}=1.881+j12.491 Ω, Z_{21}=-43.096-j264.651 Ω, and Z_{22}=5.279-j269.046 Ω. The difference in values is referred to the effect of deviation in the large signal Z-parameters for the simulated circuit.

Table 1. Calculated versus Simulated Optimum Load Resistance for Different Values of Load Reactance

	Calculated			*Simulated*		
X_L	150 Ω	100 Ω	50 Ω	150 Ω	100 Ω	50 Ω
$R_{L(opt)}$	80.5 Ω	116.5 Ω	152.6 Ω	80 Ω	120 Ω	150 Ω

Fig. 12 shows the variation of the magnitude of the input reflection coefficient with R_L. Its value reaches about 1.55 when R_L = 80 Ω, and X_L = 150 Ω. Fig. 13 presents the variation of the input reactance with $R_L$which is inductive for most values of R_L.

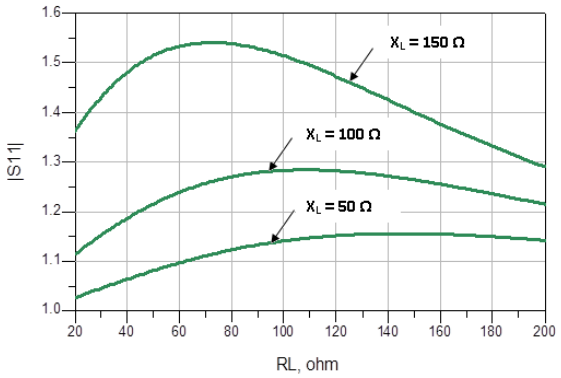

Figure 12. Variation of Γ_{in} with R_L.

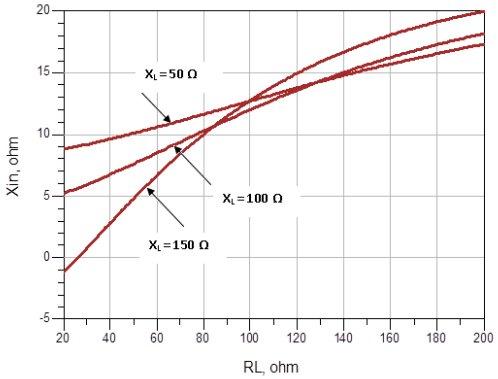

Figure 13. Variation of Input Reactance with R_L

Fig. 14 presents the variation of output power (in dBm) with R_L, while Fig. 15 displays the large signal power gain against R_L. Maximum output power is obtained when R_L = 90 Ω for X_L= 150 Ω. $R_{L(opt)}$ becomes 140 Ω for X_L = 100 Ω, and reaches to 180 Ω when X_L = 50 Ω. It is noticed from Fig. 11 and Fig.14 that the optimum load resistances for maximum $|R_{in}|$ and maximum P_{out} are slightly different. This means that the optimum load resistance $R_{L(opt)}$ takes different values for optimum load power and maximum negative resistance conditions respectively.

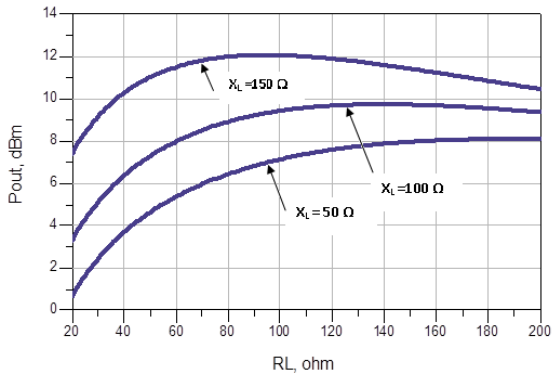

Figure 14. Simulated Output Power versus R_L for Different Values of X_L

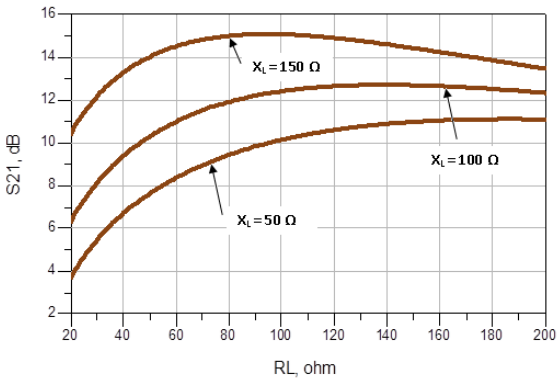

Figure 15. Simulated Power Gain versus R_L for Different Values of X_L

On the other hand, another family of curves can be generated when varying X_L as a sweeping variable for different values of R_L. Fig. 16 presents the variation of the input resistance with X_L for three values of R_L. It is seen from this sketch that the optimum value of X_L for maximum negative resistance differs in the three cases of R_L. For example when R_L = 80 Ω, the optimum value of X_L is about 232 Ω. It becomes 236 Ω when R_L = 100 Ω, and reaches to 238 Ω when R_L = 120 Ω. This means that $X_{L(opt)}$ is a function of R_L in addition to the large signal device parameters.

Fig. 17 presents the variation of the simulated output power with X_L for different values of R_L. In this case, the maximum output power is achieved when X_L = 200 Ω, and R_L = 80 Ω. It is noted from the sketches of Fig. 16 and Fig. 17 that the optimum values of X_L for maximum negative input resistance and maximum output power do not coincide. There is a slight difference in their values for the two cases.

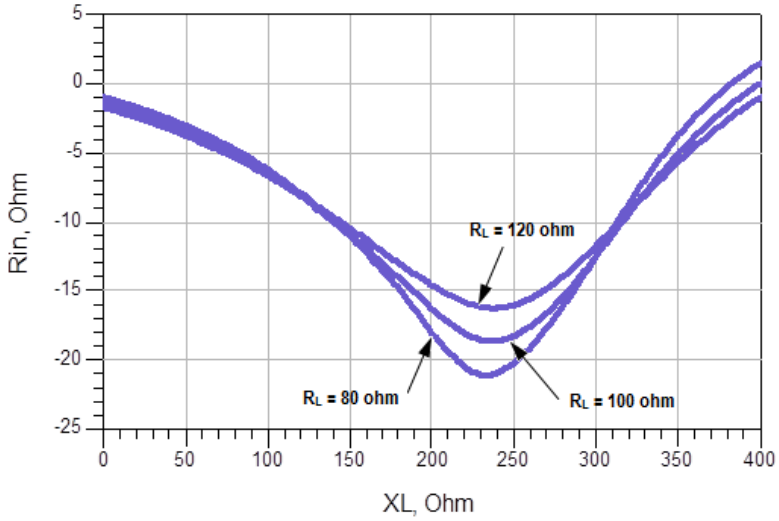

Figure 16. Variation of R_{in} against X_L for Three Values of R_L

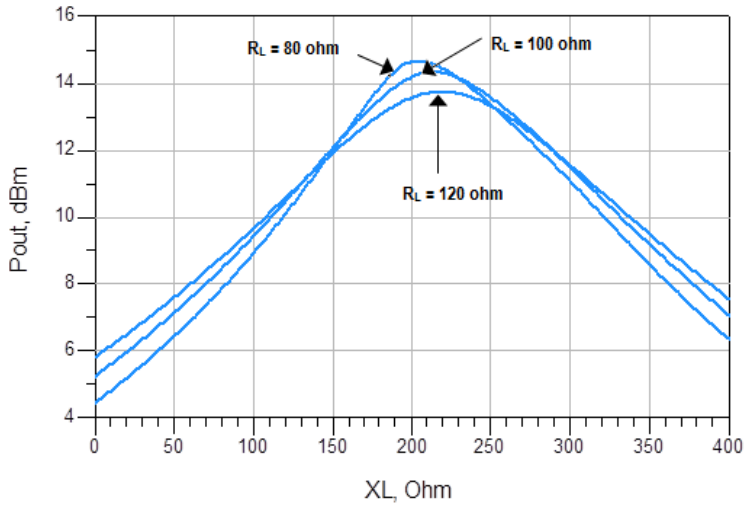

Figure 17. Simulated Output Power versus X_L for Different Values of R_L

Thus, the optimum load impedance of the oscillator can be selected as a compromise for the required output power, negative input resistance, resonator's quality factor, and harmonic distortion. The value of $Z_{L(opt)}$ for maximum negative input resistance does not necessarily coincide with its value for maximum output power as indicated from the previous simulations. This is referred to the nonlinear behavior of the RF device under large signal conditions. From the above family of curves, $Z_{L(opt)}$ is selected to be 80 + j150 Ω. At this point, the maximum attainable output power is about +12 dBm and the large signal input impedance Z_{in} is approximately -11+j10 Ω.

An output matching network is designed to transform the standard 50 Ω load into the optimum impedance $Z_{L(opt)}$ at the oscillation frequency. Fig. 18 presents a topology for the output matching network consisting of a series transmission line and a parallel shorted stub. This circuit is designed using the graphical Smith chart tool of the *Advanced Design System* (ADS) microwave computer-aided design (CAD) program.

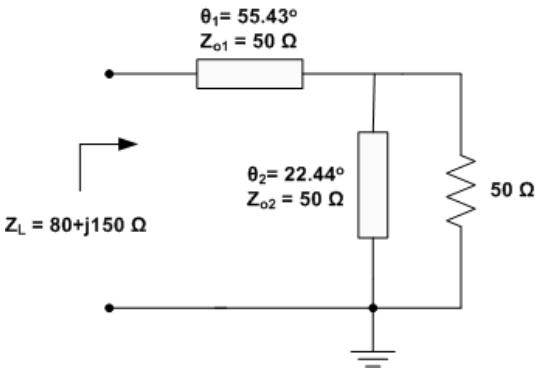

Figure 18. Oscillator's Designed Output Matching Network

6.5. Determination of the Input Impedance

To determine the large signal input impedance and other predictable characteristics of the oscillator at the desired oscillation point, a simulation test setup is carried out to

sweep the available power at the input port while viewing the oscillator performance characteristics. Fig. 19 shows this simulation setup. In this schematic, the output matching network is inserted at the output to present the optimum load impedance to the oscillator output port at 900 MHz. The available input power is swept from -20 dBm to +10 dBm.

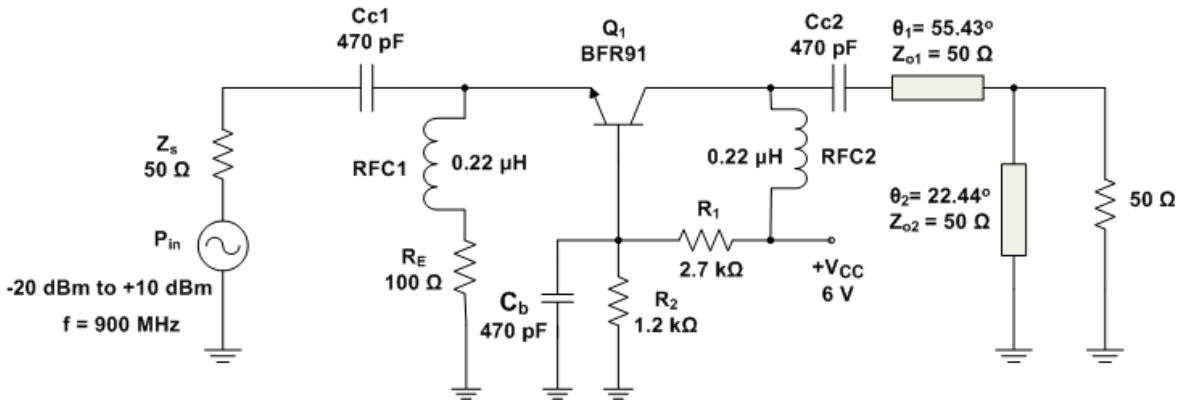

Figure 19. Circuit Schematic for Input Power Sweep

Fig. 20 shows the variation of the input resistance R_{in} with input power level, while Fig. 21 presents the change of the input reactance X_{in} with power. It is noticed that the characteristic in Fig. 20 is similar to the curve of Fig. 2. The input resistance R_{in} is negative and equals to -13 Ω at low power levels, but its magnitude decreases with the increase of the input power level reaching to 0 Ω when P_{in} = +3.5 dBm approximately. So, at relatively high power levels in the input port, the circuit may fail to oscillate. For an input power level of -3 dBm, the input impedance of the RF device Z_{in} = -11+j10 Ω as shown in Fig. 20 and Fig. 21. At this power level, the input reflection coefficient is about 1.5 as depicted in Fig. 22, while the output power is about 11.9 dBm as illustrated in Fig. 23. At this point the output power is relatively high but not deeply saturated.

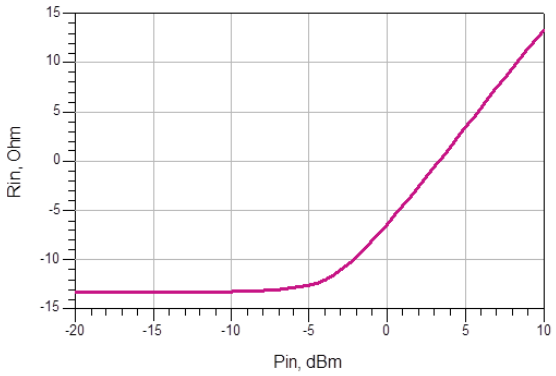

Figure 20. Variation of Negative Input Resistance with Power Level

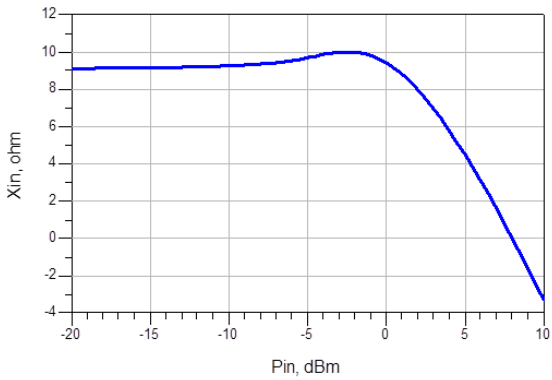

Figure 21. Variation of Oscillator's Input Reactance with Power Level

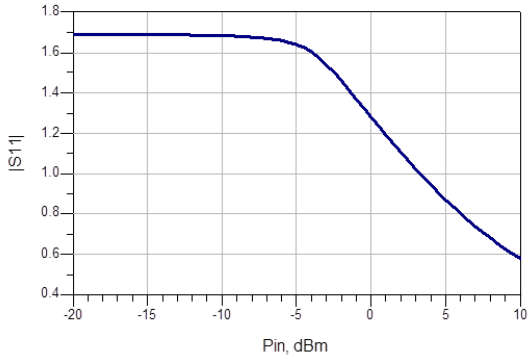

Figure 22: Variation of the Input Reflection Coefficient with Power Level

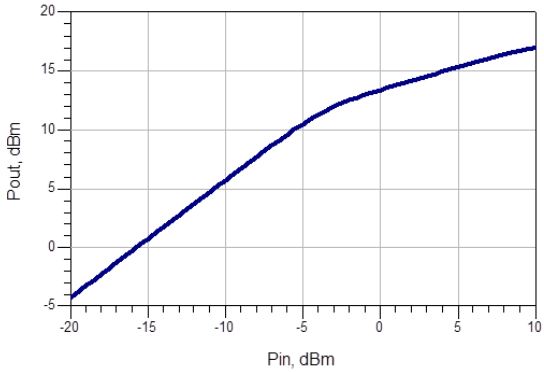

Figure 23: Output Power versus Input Power

6.6. Design of the Resonator Network

Based on the selected working point for the oscillator circuit, the resonator network of the oscillator is to be designed in order to present an impedance of Z_r = 11-j10 Ω according to equation (3). If the input port is terminated with a 50-Ω standard resistance, then a transforming network can be designed to match the 50-Ω resistance with Z_r. Fig. 24 shows a π-section topology for the resonator consisting of a series transmission line and two parallel capacitors. This circuit has been designed using the Smith chart tool of ADS. The two capacitors are necessary to tune the frequency of the practical oscillator circuit.

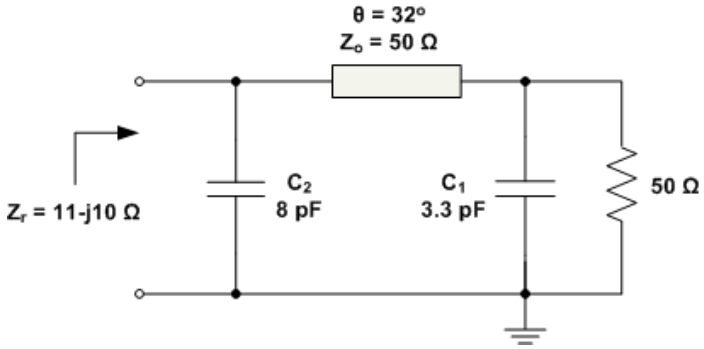

Figure 24.The Designed Resonator Network

6.7. Oscillator Performance Evaluation and Testing

Up to this stage, the oscillator circuit has been designed to oscillate at 900 MHz with a load power of more than 11 dBm. This circuit needs computer simulation with the ADS harmonic balance simulator to view its performance characteristics. Fig. 25 presents the schematic diagram of the designed oscillator circuit with the transmission line sections implemented using Microstrip-line elements. The selected Microstrip substrate is the epoxy-glass (FR-4) which has a relative dielectric constant of 4.5 and a thickness h = 1.6 mm. The tangent loss of this substrate is about 0.01, while the copper conductor thickness is 0.05 mm. The Microstrip line lengths and widths were tuned for practical purposes.

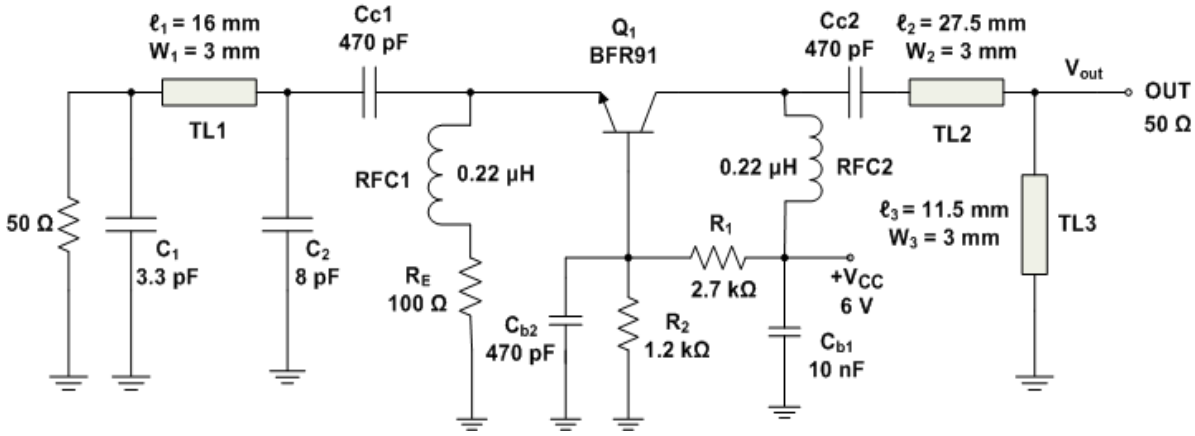

Figure 25. Circuit Schematic of the Designed RF Oscillator

The output signal of the circuit is displayed in Fig. 26 while its spectrum is shown in Fig. 27. The obtained frequency of the output signal is 901.6 MHz, and the power level of the fundamental component is 11.3 dBm. As shown from Fig. 27, the second harmonic distortion level is about 20 dBc below the fundamental signal component.

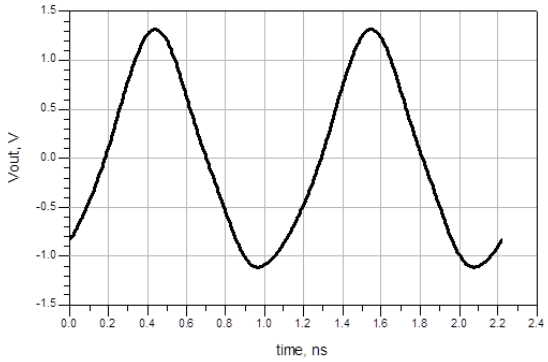

Figure 26. Simulated Output Voltage Waveform of the Oscillator

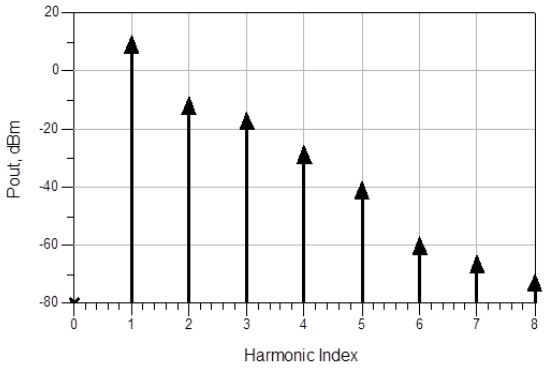

Figure 27. Simulated Power Spectrum of the Output Signal

The fundamental output power is calculated from:

$$P_{out} = 0.5\, Re[V_{o1}.I_{o1}^{*}] \qquad (33)$$

Where V_{o1} is the amplitude of the fundamental component of the output voltage, and I_{o1} is the amplitude of the fundamental output current flowing into the 50 ohm load resistor and is evaluated by means of a current probe placed at the output.
The input impedance of the oscillator is calculated from:

$$Z_{in} = \frac{V_{i1}}{I_{i1}} \qquad (34)$$

Where V_{i1} is the amplitude of the fundamental component of the voltage at the emitter of the transistor, and I_{i1} is the amplitude of the fundamental component of the current entering the active device, and is evaluated by means of a current probe at the device input.

The input resistance and reactance of the active device are evaluated from equations (11.1) and (11.2) respectively. The evaluated value of the input impedance using computer simulation for the oscillator circuit is Z_{in} = -10.47+j10.43 Ω, while the evaluated value of the magnitude of the input reflection coefficient $|\Gamma_{in}|$ is found to be 1.501.

An experimental model for the circuit was implemented on a printed 8 cm × 6 cm FR4 board. Fig. 28 shows the PCB layout of the printed board, while Fig. 29 presents a picture for the assembled circuit. The upper ground of the board was connected with the lower ground through VIA holes to reduce the RF ground currents. Capacitors C_1 and C_2 were implemented by using high quality ceramic trimmer capacitors to adjust the frequency of oscillation for the circuit. The shorted stub at the output matching network was connected to ground through a 470 pF bypass capacitor. The output signal is taken from an SMA connector soldered between the output of the circuit and the ground plane.

The circuit was thereafter tested with the aid of a commercial spectrum analyzer (PSA-3000 of ED Co., Ltd.) as depicted in Fig. 30. Fig. 31 shows the fundamental signal component of the generated waveform. The practical attainable frequency is 896.75 MHz with a fundamental power level of 6.15 dBm. Fig. 32 presents the second harmonic component compared with the fundamental signal. As depicted from this plot, the second harmonic level is about 22 dBc below the fundamental signal component. As shown from Fig. 31 and Fig. 32, the signal purity is acceptable and there is no spurious frequency components generated by the circuit.

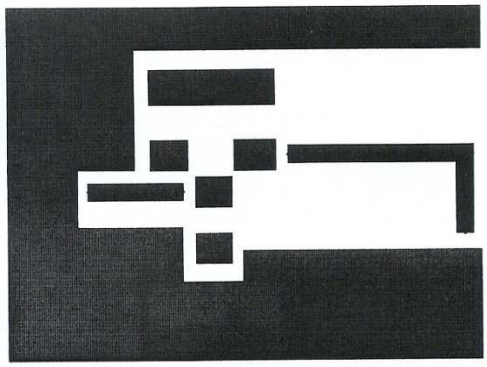

Figure 28. Layout of the Printed Circuit Board

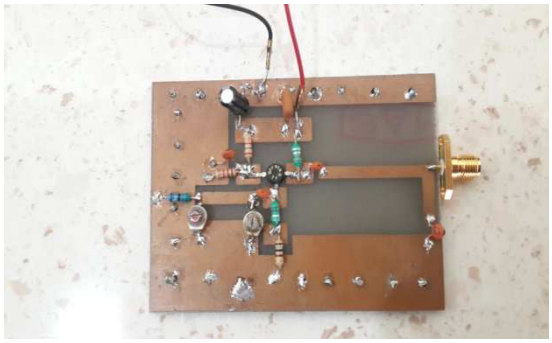

Figure 29. The Constructed Oscillator Circuit

7. Conclusions

A design technique of negative-resistance RF oscillators based on the effect of the optimum load impedance has been proposed and confirmed. Explicit-form equations for estimating the optimum load impedance of the oscillator circuit have been derived in terms of the terminal Z-parameters of the RF transistor. Generally, the convenience of

this approach is that the results for small-signal analysis can be taken as initial guess for large-signal computer optimization.

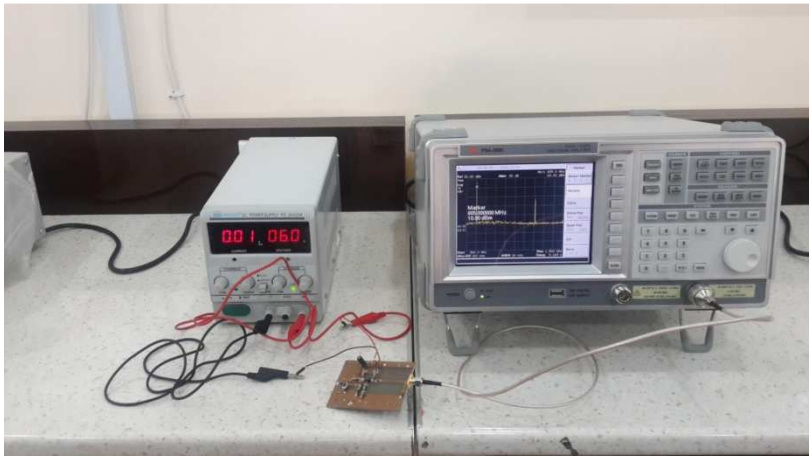

Figure 30. Test Setup for the Implemented Oscillator Circuit

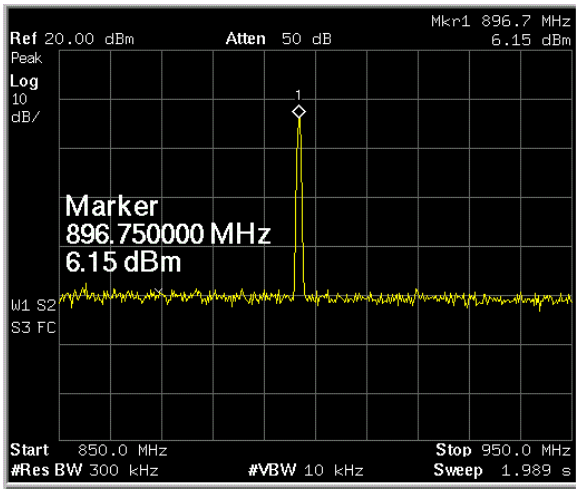

Figure 31. Spectrum of the Fundamental Component of the Generated Signal

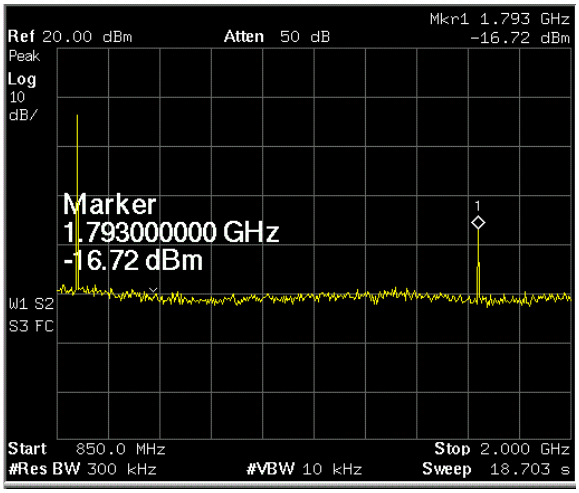

Figure 32. Measured Second Harmonic Level

It has been shown that the performance characteristics of the oscillator circuit can be predicted if the optimum load impedance is selected at the desired power level and input negative resistance with the active device well represented through its large signal model. It has been verified also that both the optimum load resistance and optimum load reactance are dependent on each other. Families of curves have been generated through computer simulation with either R_L or X_L as the sweeping variable to select the load resistance and reactance for the required large signal negative input resistance and output power level. It has been shown also that the optimum impedance for maximum negative resistance does no coincide with its value for maximum output power. This difference may be referred to the variation of the device internal parameters under large signal nonlinear conditions, and may probably be different for different types of RF devices.

A 900 MHz RF oscillator circuit has been designed and simulated based on the proposed design strategy. The simulated circuit offered a fundamental output power level of more than +11 dBm at an oscillation frequency of 901.6 MHz with a second harmonic level of about 20 dBc below the fundamental signal. The circuit was then implemented experimentally and produced a pure RF signal with a frequency of 896.75 MHz and output power level of +6.15 dBm, with a second harmonic distortion of about 22 dBc below the fundamental signal component.

8. References

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