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Suppression of the Capacitor Voltage ripple in Modular Multilevel Converter for Variable-Speed Drive Applications

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Keywords:
HMMC Topology; Individual Capacitor Balancing Control; Minimization of Capacitor Voltage Ripple; Phase-Shift PWM; Vector Control.

Highlights:

- *Reduce the capacitor voltage fluctuations of MMC at low frequencies and reducing the capacitance size of the SM capacitor.*
- *Show the ability of HMMC to start up a medium voltage induction Motor at wide speed range with full load torque.*
- *To obtain high quality waveforms of voltage and current without use any filter.*

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Abstract: The modular multilevel converters (MMC) utilization has brought about a transformative impact on high voltage direct current (HVDC) transmission relying on voltage-sourced converters (VSC). However, their application in medium-voltage (MV) variable-speed motor drives has not achieved broad acceptance due to the substantial voltage fluctuation in the capacitor, especially at lower frequencies. The present study introduces a hybrid MMC (HMMC) aimed at markedly limiting capacitor voltage fluctuations, particularly during low motor speeds. Vector control was used to achieve the required motor speed. The proposed HMMC validity was confirmed through the MATLAB/ SIMULINK environment. The results were compared with conventional MMC from the standpoint of the capacitor voltage fluctuation at low frequencies.

قمع تموج جهد المكثف في المحول المعياري متعدد المستويات لتطبيقات المحركات المتغيرة السرعة

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الخلاصة

أدى استخدام المحولات المعيارية متعددة المستويات (MMC) إلى إحداث تأثير تحويلي على نقل التيار المباشر عالي الجهد (HVDC) بالاعتماد على محولات مصادر الجهد (VSC). ومع ذلك، فإن تطبيقها في محركات متغيرة السرعة ذات الجهد المتوسط (MV) لم يحقق قبولًا واسعًا بسبب تقلبات الجهد الكبيرة في مكثف الوحدة الفرعية (SM)، خاصة عند سرعات المحرك المنخفضة. تقدم هذه الورقة (HMMC) MMC الهجين الذي يهدف إلى الحد بشكل ملحوظ من تقلبات جهد المكثف، خاصة أثناء سرعات المحرك المنخفضة. يتم استخدام التحكم المتجه لتحقيق سرعة المحرك المطلوبة. يتم تأكيد صحة HMMC المقترحة من خلال بيئة MATLAB/SIMULINK. تتم مقارنة النتائج مع MMC التقليدي من وجهة نظر تقلب الجهد من الذروة إلى الذروة للمكثف عند الترددات المنخفضة.

الكلمات الدالة: طوبولوجيا HMMC، التحكم في موازنة المكثفات الفردية، موازنة الجهد SM، مرحلة التحول وتوليد النبضة.

1.INTRODUCTION

The inverter unit converts the input DC voltage into a constant magnitude voltage and frequency, which is then used to power the designated loads, such as the induction motor (IM). The Pulse Width Modulation (PWM) approach is employed generate a sinusoidal output voltage. In addition, the modulation index control is utilized to regulate inverter output [1]. IMs are commonly used in industrial applications, aerospace, electrical vehicles, and hybrid electrical vehicles. These motors have gained popularity because of their numerous advantages, including their relatively low production cost, sturdy construction, moderate power factor, high reliability, and improved ease of control, particularly in recent times. Induction motors serve as the primary component in numerous applications, wherein they are commonly employed alongside power electronic drivers to regulate parameters such as speed, torque, and starting conditions [2,3]. Recently, multilevel converters have been widely accepted in industrial and energy systems. The IM motor drives have garnered significant attention in a wide range of applications [4] due to their ability to design medium and high-voltage systems with excellent output voltage quality. Simple implementation of redundancy, low filter expense, and reduction of power semiconductor losses and common-mode voltage are significant additional advantages compared to two-level voltage source converters [5,6]. Among the different topologies of multilevel converters, multi-cell converters have the highest degree of modularity and the lowest redundancy cost because of their large cells number, and the lowest harmonic content because they generate a large number of output voltage levels. Units large number significant increases the requirements on the converter controllers, however each unit provides a simple structure, which reduces manufacturing costs. Currently, multi-unit converters are used in medium-voltage drives (MVDs), active filters, integration of renewable energy into the grid, and high-voltage direct current (HVDC) transmission systems [7–9]. In 2003, Professor Marquardt of the Bundeswehr University in Munich, Germany, proposed a new multilevel converter topology called Modular Multilevel Converter (MMC) [9], which has shown in terms of conversion efficiency, voltage power level, and other parameters [10]. MMC had a series of excellent performances, such as multi-level voltage output, modular structure, and easy installation and maintenance. Also, it saves the need for cascaded H bridges. The costly and loss-heavy phase-shifting transformers in bridge drives are directly connected to the grid and powered via a common DC bus. The MMC's flexibility, simple structure, and easy-to-expand characteristics make applying the voltage/power level no longer limited. In contrast, MMC uses multi-winding phase-shifting input transformers, and the AC output requires no additional filtering devices [11–15]. Fig. 1 shows the MMC topology. In this topology, two arms form a converter phase where the DC system is connected to the upper and lower of the phases and the three-phase. The AC system is connected to the center of each phase j (a,b,c) point. The arm connected to the positive rod is usually called the positive or upper arm, and the arm connected to the negative rod is called the negative or lower arm. Each arm consists of N sub-modules (SMs) either half-bridge or full-bridge and they are connected in series. AC and DC systems are usually modeled as voltage sources and lines as inductors. Fig. 1 also shows the arm inductance

L, which must be connected in series with each set of power cells to limit the current due to instantaneous voltage differences across the arms. Due to the common DC bus of the MMC it can easily expand to a Back-to-Back (BTB) structure [16].

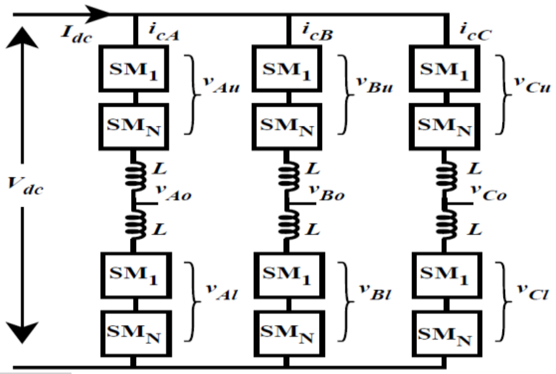


Fig. 1 Modular Multilevel Converter Topology.

Compared with a two-level inverter, the two-level inverter output voltage is a square wave with a significant amount of harmonics. These harmonics have larger amplitudes than the amplitude of the fundamental [17]. Compared with cascaded H bridge (CHB) and neutral point clamped (NPC), the frequency converters have been commonly used in industry. For CHB inverters, each sub-module needs an independent isolated DC power supply, so a multi-winding phase-shifting transformer has to be used. The phase-shifting transformer is bulky, difficult to transport, complex in the manufacturing process, and expensive, especially in the case of high voltage and high power, which is challenging to design and realize which restricts the voltage and power level of the CHB inverter. Since the CHB does not have a common DC bus, it is challenging to realize the four-quadrant operation of the motor [18, 19]. NPC and MMC have a common DC bus and can use a standard input transformer. However, the disadvantage of NPC is that the number of output voltage levels is small, and the harmonic content is large. It needs to install a filter device to connect to the motor. In addition, a higher number of levels will significantly increase the topology complexity and control difficulty. The NPC inverters levels number is usually limited to three levels, and its voltage and power levels are also limited [20,21]. Although the MMC has certain advantages, the MMC application in frequency conversion and speed regulation of high-voltage motors requires many capacitors to support, and the capacitor voltage fluctuates more seriously at low frequencies. Therefore, when the MMC drives the motor to run at high torque and low speed, it is necessary to use a capacitor with a large capacity to ensure that the capacitor voltage fluctuation is within a reasonable range, resulting in the problems of high cost and bulky converter [22–25].

- In 2021, Wang et al. [26] used conventional MMC for driving the IM with development control method by model predictive control to reduce voltage fluctuation of the SM capacitor.
- In 2022, Aarzoo and Poddar [27] used a controlled variable current source derived from a thyristor and it is connected on the IM side to ensure that the voltage fluctuation of the SM capacitor is closely connected to the torque only.
- In 2022, Liu and Dong [28] hybrid MMC converter with a flying capacitor for medium voltage to minimize the number of SMs, the capacitor size, and the conduction losses, improving the power efficiency.
- In 2022, Ali and Hassan [22] used a high-frequency dual half-bridge (DHB) with an isolated transformer with variable speed IM drive that connected adjacent to the SM of the MMC to allow power interchange between the SM capacitors, leading to transmission of the energy between each phase and reduce the voltage ripple of the SM capacitor. In this method, the DHB number is the same as SMs, which requires increasing the switches numbers, increasing the losses, cost, and size. Also, the control becomes complex if the SMs numbers increases.
- In 2023, Jia et al. [29] used conventional MMC for variable speed drive with the injection voltage method with variable a frequency depending on the output frequency to reduce the voltage fluctuation of the SM capacitor. However, this method causes a common mode voltage that may damage the IM winding insulation and bearings.

The present paper introduces a hybrid MMC topology by connecting a switch in series between the supply voltage and the MMC to limit the voltage ripple of the capacitor at low frequency. A suitable control for HMMC based on vector control for IM is presented to achieve wide speed ranges.

2.THE PROPOSED HMMC

Figure 2 shows the proposed HMMC. This topology characteristic is a controllable switch connected in series on the MMC DC side , and the MMC DC voltage is reduced equivalently by chopping, which reduces the power ripple of the bridge arm, suppressing the voltage fluctuation of the capacitor [30]. This HMMC does not inject high-frequency common-mode voltage and circulating current, which avoids the problem of common-mode voltage. The circulating current amplitude is consistent with the traditional MMC, and will not increase the bridge arm current stress. To limit the harmonics caused by the series switch an RC filter is used and connected in parallel [31].

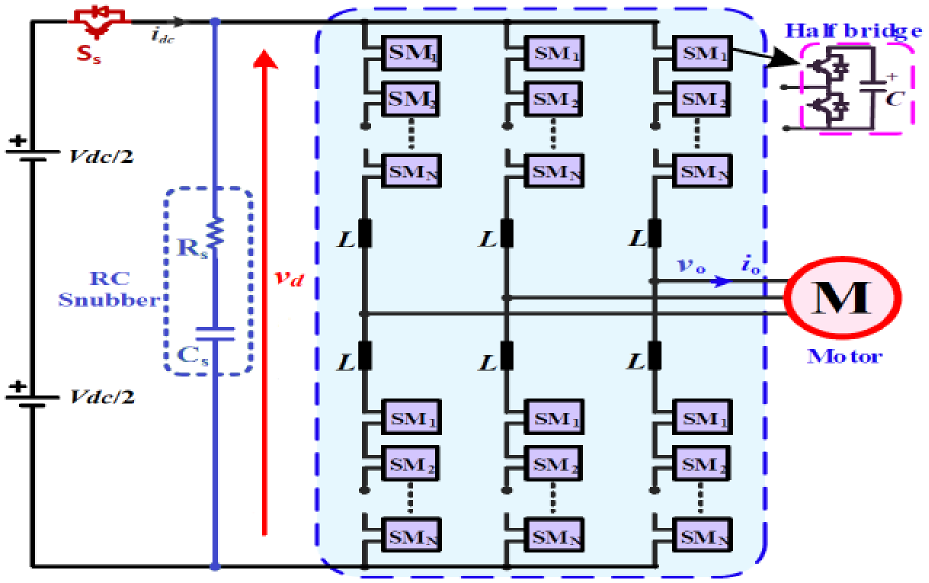


Fig. 2 Proposed HMMC Topology.

2.1. Analysis of the Conventional MMC

From Fig. 1, the conventional MMC output voltage and current of can be written as [32]:

$$v_{jo} = V_O \cos(\omega t + \alpha_j) \quad \textbf{(1)}$$

$$i_{jo} = I_O \cos(\omega t + \alpha_j - \delta) \quad \textbf{(2)}$$

where ω is represent angular frequency, α_j is the phase angle (0, -120, and 120), δ is the phase lag angle, the V_O and I_O are the amplitudes of voltage and current, respectively, the V_O equals to ($V_O = m\frac{1}{2}V_{dc}$), and m is the modulation ratio coefficient from (0 to 1) . By neglecting the voltage drop across the inductor L, the upper v_{ju} and lower v_{jl} arms voltages of the MMC can be written as:

$$\begin{aligned} v_{ju} &= {}^{1}/_{2}\ V_{dc} - V_O \cos(\omega t + \alpha_j) \\ v_{jl} &= {}^{1}/_{2}\ V_{dc} + V_O \cos(\omega t + \alpha_j) \end{aligned} \quad \textbf{(3)}$$

It should be pointed out that the output current passes through the bridge arms. Then; the upper arm current i_{ju} and lower arm current i_{jl} of the MMC are obtained from:

$$\begin{aligned} i_{ju} &= i_{cj} + {}^{1}/_{2}\ I_O \cos(\omega t + \alpha_j - \delta) \\ i_{jl} &= i_{cj} - {}^{1}/_{2}\ I_O \cos(\omega t + \alpha_j - \delta) \end{aligned} \quad \textbf{(4)}$$

where i_{cj} is the circulating current of phase j, which flows between the upper and lower bridge arms with an amplitude of $I_{dc}/3$. Assuming that the loss can be neglected, the input and output power conservation $V_{dc}I_{dc} = {}^{3}/_{2}\ m\, V_O I_O \cos\varphi$, then MMC DC current I_{dc} is expressed as:

$$I_{dc} = {}^{3}/_{4}\ m\, I_O \cos\varphi \quad \textbf{(5)}$$

The SM capacitor peak-to-peak voltage fluctuation $\Delta V_{C(pp)}$ of the conventional MMC can be expressed as [32]:

$$\Delta V_{C(pp)} = \frac{I_O}{4\pi F C} \quad \textbf{(6)}$$

From Eq. (6). The peak-to-peak voltage fluctuation of the conventional MMC capacitor is proportional to the output current amplitude; and inversely proportional to the frequency. If the MMC operates at low frequencies and rated currents, the voltage fluctuation of the capacitor will increase, leading to the converter's failure to work.

2.2. Analysis Operation Principle of HMMC

Figure 3 shows the operation principle waveforms of the proposed HMMC topology. Due to the action of the controllable switch Ss, the MMC DC-bus side voltage can be minimized: therefor, the power ripple of the bridge arms can also be reduced, reducing the SM capacitor peak-to-peak voltage ripple. The switch signal of Ss is synchronous with DC bus current I_{dc}, and circulating current i_{cj}. The operation of the HMMC is similar to conventional MMC when the HMMC operates at rated frequency (D=m).

From Fig. 3, the DC terminal voltage (v_d) can be obtained as:

$$v_d = \begin{cases} v_{dc}. & (\textit{when the } S_s \text{ is switced ON}) \\ m\, v_{dc}. & (\textit{when the } S_s \text{ is switced OFF}) \end{cases} \quad \textbf{(7)}$$

From Fig. 3, it can be seen that the average value of the DC terminal voltage $\bar{V}_d$ is closely connected with the duty ratio (D) of the Ss and it can be calculated from:

$$\bar{V}_d = DV_{dc} + (1 - D)mV_{dc} \quad \textbf{(8)}$$

The upper v_{ju} and lower v_{jl} arms voltages of the HMMC can be written as:

$$\begin{cases} v_{ju} = {}^{1}/_{2}\, v_d - v_{jo} - \Delta v_d \\ v_{jl} = {}^{1}/_{2}\, v_d + v_{jo} - \Delta v_d \end{cases} \quad \textbf{(9)}$$

Also, the DC current I_{dc} and circulating current i_c are discontinuous waveforms and synchronous with the switching signal of the Ss, and they can be expressed as:

$$I_{dc} = \begin{cases} I_{dc(rated)}. & if\ (S_s = 1) \\ 0. & if\ (S_s = 0) \end{cases} \ and\ i_c = \frac{1}{3}\, i_{dc} \quad \textbf{(10)}$$

The voltage fluctuation of the HMMC's SM capacitor is obtained from [30]:

$$\Delta V_{C(pp)} = \left(2 - \frac{\omega}{\omega_{rated}}\right) \frac{I_{O(rated)}}{2\omega_{rated} C} \quad (11)$$

Comparing Eq. (6) with Eq. (11), it can be seen that the peak-to-peak voltage of the SM capacitor of the voltage HMMC reduces if the HMMC operates at low frequency and it is less than of the conventional MMC.

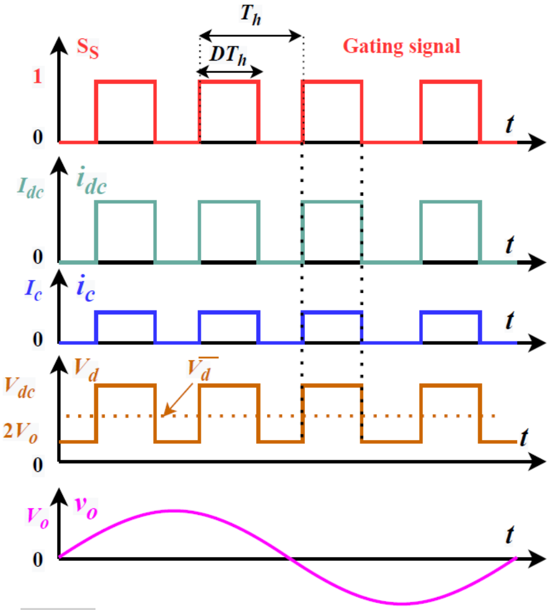


Fig. 3 Waveforms of the HMMC Topology.

2.3.Operation Proses of the HMMC Based IM Drive

Fig.4 shows the HMMC operation Proses flowchart. The first process selects the number of SM cells, and the second process measures the SMs capacitor voltages to make balance with V_{dc}/N. If the SMs capacitor voltages are unbalanced the Ss duty cycle must be regulated to ensure a stable operation of HMMC. The third process is circulates control to achieve the voltage balance of each SM capacitors between each arms and each phase. The fourth process is vector control to produces the reference voltages with variable frequency to get a wide speed range. The fifth process is capacitor-balancing control to ensure that the voltage of the SM capacitor remains close to its reference value. The final process is a Phase-shifted carrier PWM to generate the desired IGBT switching signals. When the output frequency equals the rated frequency, the HMMC operates as a conventional MMC.

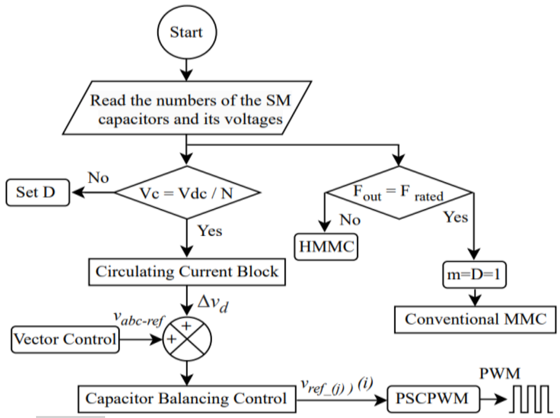


Fig.4 Flowchart of the HMMC Operation Proses.

3.CONTROL SCHEME OF HMMC

This section focuses on the proposed HMMC control. As shown in Fig. 5, the control strategy consists of a series switch, circulating current control, vector control, individual capacitor balancing control, and Phase-shifted PWM.

3.1.Series Switch Control

To achieve a stable HMMC operation, it should maintain a balance between its input and output power. The energy stored in the SM capacitor is influenced by the power disparity between the input and output. To maintain an overall energy balance, the control system, depicted in Fig. 6, ensures that the average value of the SM capacitor voltage $\boldsymbol{V_{c\,(avg-all)}}$ is constrained to match its reference value $\boldsymbol{V_{dc}/N}$; therefore, the duty cycle D is controlled for this reason. The switching frequency of Ss depends on the output frequency which is equal to (10 × output frequency). MATLAB function is used to obtain the frequency of Ss, as shown in the appendix.

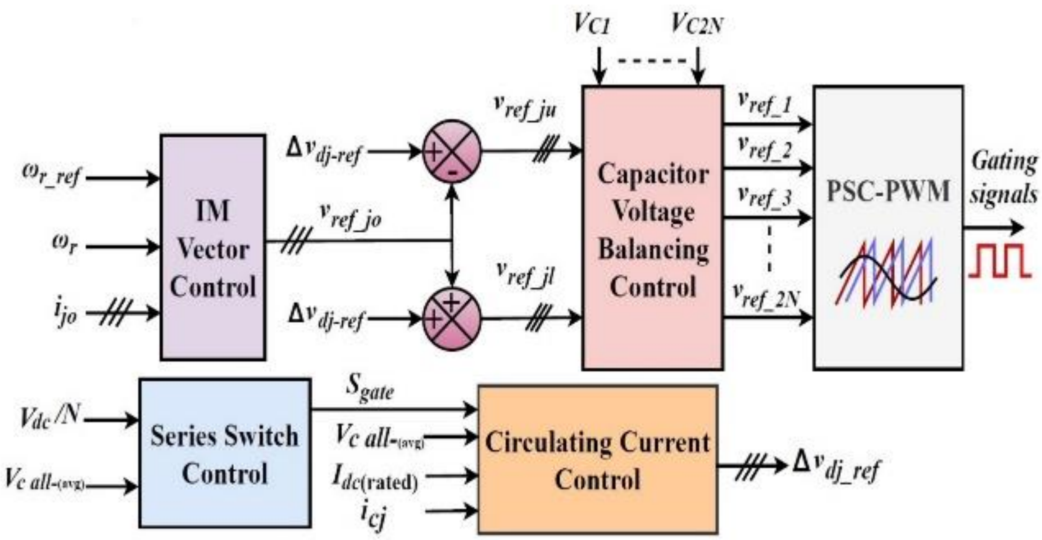


Fig.5 Control Block Diagram of the Proposed HMMC.

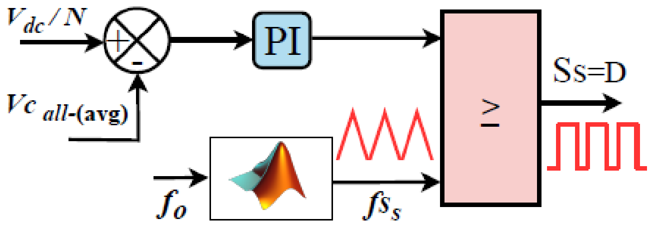


Fig.6 Schematic of Ss Control.

The average voltage of the SM capacitor for the upper and lower arms can be written as [33]:

$$V_{C\_avg\_ju} = \sum_{i=1}^{N} V_{cap\_ju}(i) \quad \textbf{(12)}$$

$$V_{C\_avg\_jl} = \sum_{i=1}^{N} V_{cap\_jl}(i) \quad \textbf{(13)}$$

The average voltage of the SM capacitor for each phase j can be expressed as [34]:

$$V_{C\_avg\_j} = \frac{10}{2N} \sum_{i=1}^{2N} V_{cap\_j}(i) \quad \textbf{(14)}$$

The overall average voltage of the SM capacitor for the HMMC $V_{c\,(avg-all)}$ is obtained from:

$$V_{c\,(avg-all)} = \frac{\sum V_{C\_avg\_j}}{3} \quad \textbf{(15)}$$

3.2.Circulating Current Block

The principle of phase energy balance control and bridge arm energy's balance control is similar to the traditional MMC control method as shown in Fig. 7. The phase balance control maintains the average capacitor voltage of the phase sub-module equal to $\boldsymbol{V_{C\_avg}}$ by adjusting a DC circulating current adjustment value $\boldsymbol{\Delta Ic}$, while the energy balance of the bridge arm ensures equal energy between the upper and lower bridge arms by controlling a fundamental frequency circulating current adjustment value $\boldsymbol{\Delta Ic1}$. Add the obtained current adjustments to obtain the circulating current amplitude $\boldsymbol{Ic-ref} = ⅓\boldsymbol{Idc(rated)} + \boldsymbol{\Delta Ic} + \boldsymbol{\Delta Ic1}$, and multiply $\boldsymbol{Ic-ref}$ with the duty cycle $\boldsymbol{D}$ to obtain the final circulating current reference signal. The signal is tracked and controlled by the circulating current controller to obtain the voltage output $\boldsymbol{\Delta v_d}$, and the final voltage command of the upper and lower bridge arms is obtained according to Eq. (8). MATLAB function is used to obtain the average value of the capacitors as shown in the appendix. MATLAB/ SIMULINK calculates the phase lag angle $\boldsymbol{\delta}$ as shown in the appendix.

3.3.Vector Control

Vector control, as shown in Fig. 8, is a technology that uses a frequency converter to control a three-phase AC motor [35]. Its characteristic is that the magnetic field and torque of the motor can be individually controlled, similar to the characteristics of a separately excited DC motor [36]. The two components of the motor current vector can be controlled separately using two PI current controllers [37]. These conversions are based on the actual rotor angle $\boldsymbol{\theta_e}$. One current controller controls the torque of the motor torque, called a torque controller, and the other current controller is used to control the magnetic flux $\boldsymbol{\lambda_r}$ inside the motor. The stator current and rotor speed are measured first, then the rotor angle is derived from the calculated value of the rotor speed and slip, and then the angle of the magnetic flux is obtained [17]. From the value calculated of the rotor speed and slip, and then the magnetic flux angle is obtained [17].

3.4.Individual Capacitor Balancing Control

Figure 9 shows the individual capacitor balancing control block. The main objective of the individual control is to ensure that the voltage of the SM capacitor remains close to its reference value [38]. The individual balance control forces each module's capacitor voltage to follow its average value. The difference between the capacitor voltage and its reference voltage is used as the input of the proportional controller, which is then, multiplied by the arm current. The output is a second additional reference voltage. An additional reference voltage obtained by separate balance control is in phase with the arm current [34, 39]. Finally, the reference voltages of each SM are sent to the phase-shift PWM to produce the required PWM. The reference voltages of the upper and lower arms can be expressed as [22].

$$v_{ref\_j}(i) = v_{j-ref} + K_p\left(v_{ci\,j-avg} - V_{cap\_j}(i)\right) \times \operatorname{sgn}(i_j)\, i \quad \textbf{(16)}$$

where $K_p$is the proportional gain, and "sgn" is sigm function, which it can be written as:

$$sgn(x) = \begin{cases} 1\ , & x \geq 0 \\ -1 & ,x < 0 \end{cases} \quad \textbf{(17)}$$

3.5.The Phase-Shifted Carrier PWM Block

The Phase-shifted carrier pulse width modulation (PSCPWM) is a suitable PWM modulation technique for MMC inverters because it is easy to use, high equivalent switching frequency, and small output harmonics [40], and can be used when the number of the SMs is small. It consists of an identical N triangular carrier with an amplitude of $\boldsymbol{V_{dc}/N}$ [41] as shown in Fig. 10. The utilization of PSCPWM enables the attainment of balanced power distribution, rendering it a more appropriate choice for implementation in the field of MMC frequency conversion [42].

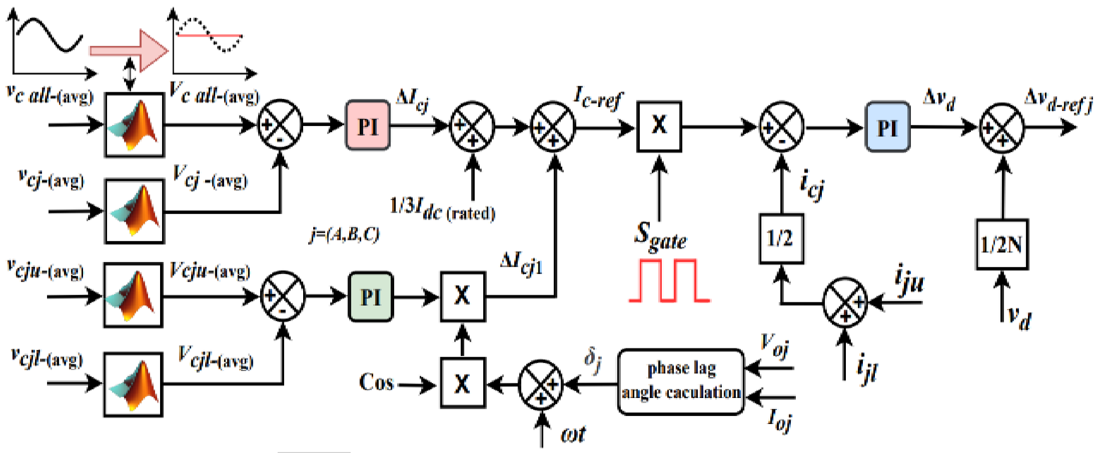


Fig. 7 Schematic of Circulating Current Block.

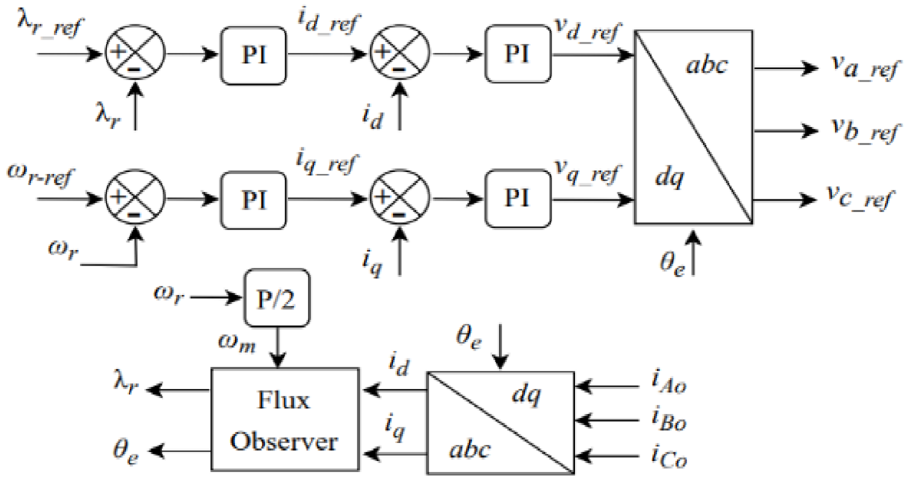


Fig. 8 Vector Control Scheme.

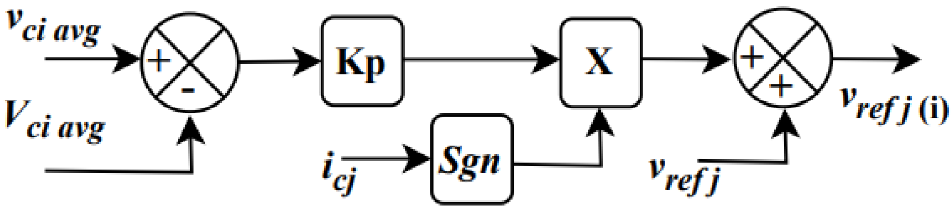


Fig. 9 Individual Capacitor Balancing Control.

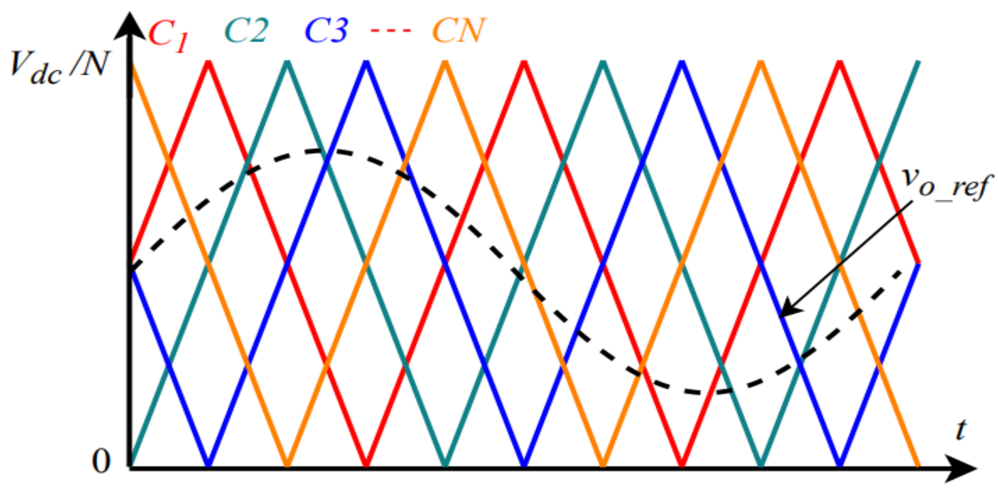


Fig. 10 Phase-Shifted Carrier PWM.

4.HMMC BASED IM DRIVE

In this section, the proposed HMMC supplies a three-phase induction motor IM drive, as shown in Fig. 11. The HMMC was implemented and designed in MATLAB/ SIMULINK environment with 20 half-bridge SM per phase (total 60 SM) with capacitance value of 4000μF. The DC bus voltage was 7000 V so the SM capacitor voltage was 700 ($Vdc\backslash N$). The swithcing frequency of the SM IGBT switches was 1 kHz.

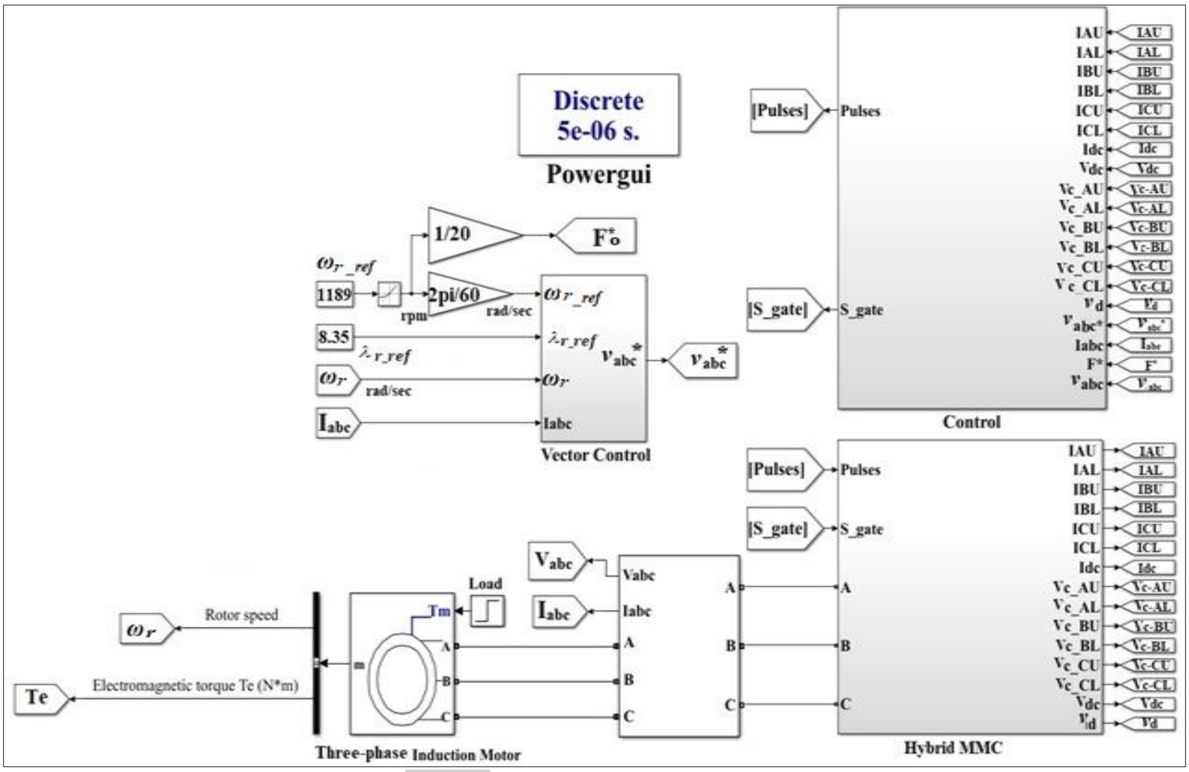


Fig. 11 HMMC Based IM Drive.

5.SIMULATION RESULTS AND DISCUSSION

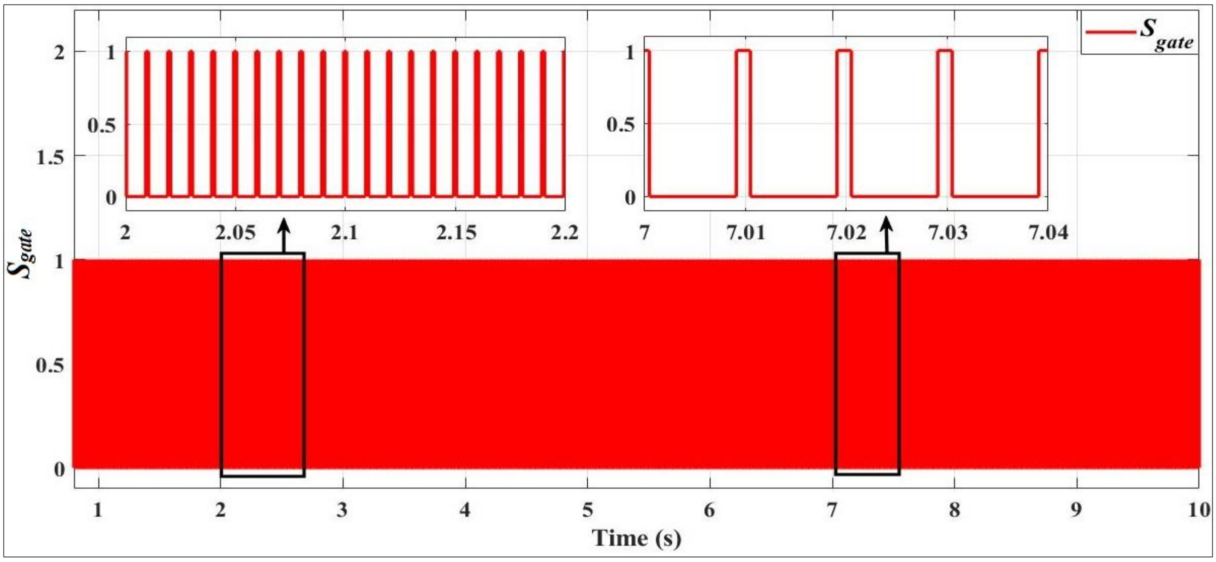
A 4160V medium-voltage IM was simulated in the MATLAB/Simulink environment to test the HMMC reliability. Table 1 details the IM parameters. The proposed HMMC was tested under three states at low frequency; these tests aimed to evaluate the dynamic performance of the HMMC and demonstrate its ability to suppress voltage ripple in the SM capacitor compared to the standard MMC.

Table 1 IM Parameters Values.

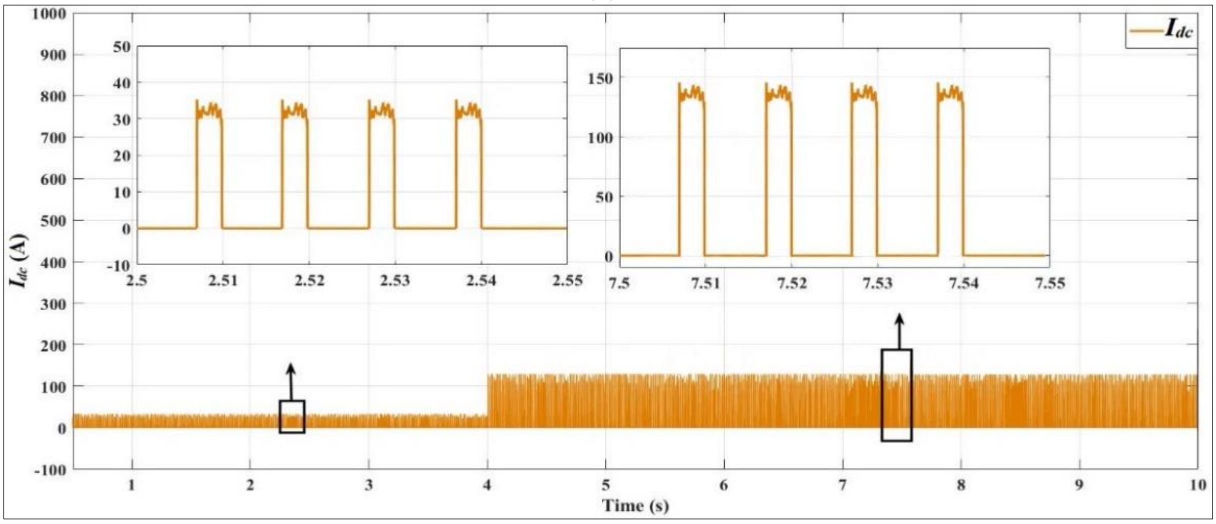
Parameter	Value
Rated powers Ps	930kw
Stator current amplitude	212A
Rated Speed	1189 rpm
Line to Line rms voltage	4160V
Number of poles pair *pp*	6
Power Factor	0.96
Rotor Flux λ_r	8.5 Wb
Stator Flux	9.1 Wb
Rated Torque	7490 N.m
Magnetizing Inductance L_m	158 mH
Stator Leakage inductance L_{ls}	4.1 mH
Rotor Leakage inductance L_{lr}	4.1 mH
Stator Resistance *Rs*	0.26 Ω
Stator Resistance *Rr*	0.165 Ω
Motor Inertia *J*	40.7 Kg-m²

5.1.State 1:

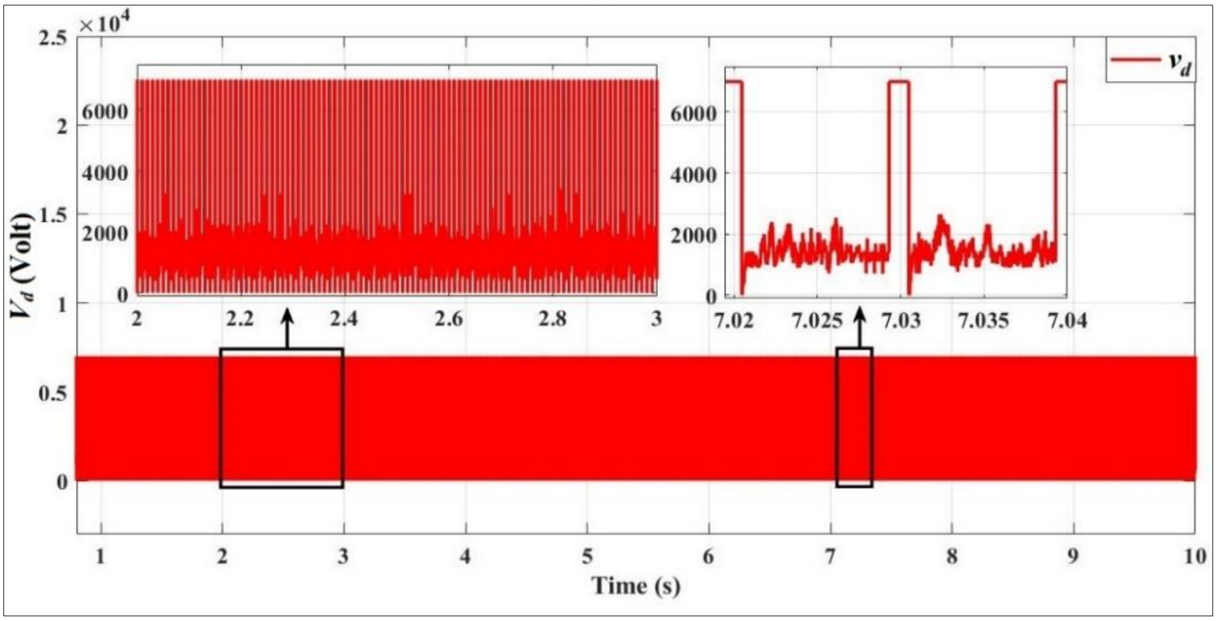
In this state, the HMMC and the conventional MMC operate at a frequency of 10Hz at no load. After 4 seconds the applied load torque was suddenly raised to its rated value of 7490 N.m. Since the output frequency was 10 Hz the switching frequency of the Ss was 100Hz ($fss = 10fo$); as shown in Fig. 12 (a). The DC bus current I_{dc} and the DC terminal voltage v_d were synchronous with the Ss and they appeared after every 0.01 sec, as shown in Fig. 12 (b) and (c). Because the load torque increased the stator currents increased from (50 A to 212 A) to produce the torque counterpart. Also, the iq current increased because it was closely connected with the torque, as shown in Fig. 13 (a), (b) and (c). The capacitor voltages of the HMMC and the conventional MMC were balanced on 700V (Vdc/N) with voltage fluctuation of (40 V to 140 V) for the proposed HMMC according to Eq. (11), and (115 V to 432 V) for the conventional MMC, according to Eq.(6), as shown in Fig. 14 (a) and (b). Because of the converter operated at 10Hz, the IM speed was 200 rpm. When the load torque increased, the PI controller tuned the speed to its reference value of 200 rpm with good dynamic response as shown in Fig. 15 (a). The Converter output voltage was tuned to achieve the required speed as shown in Fig. 15 (b).



(a)

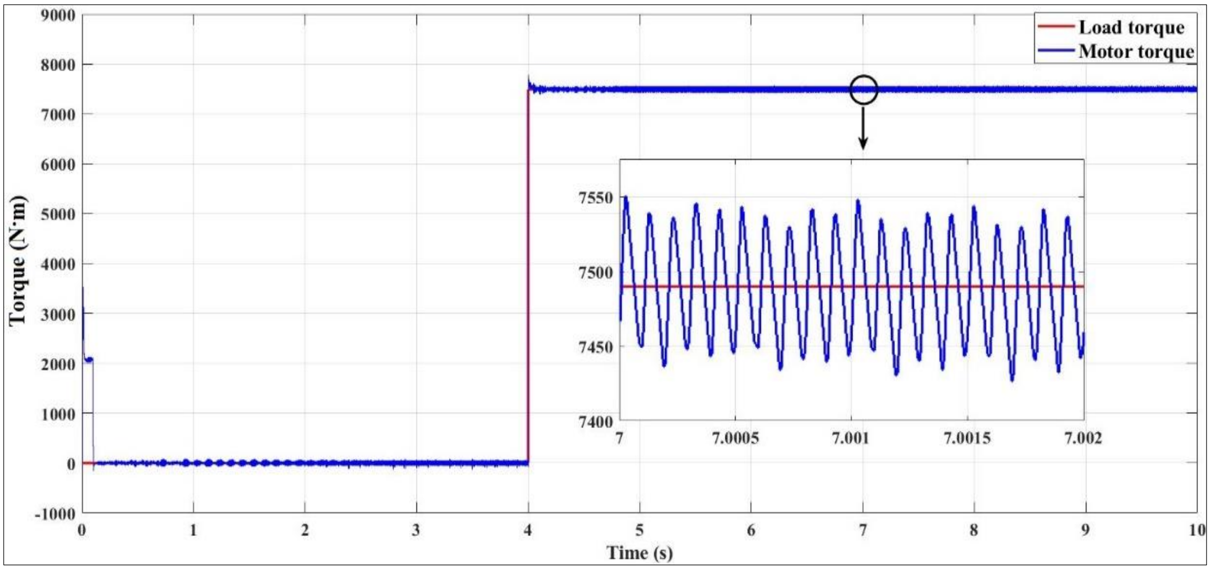


(b)

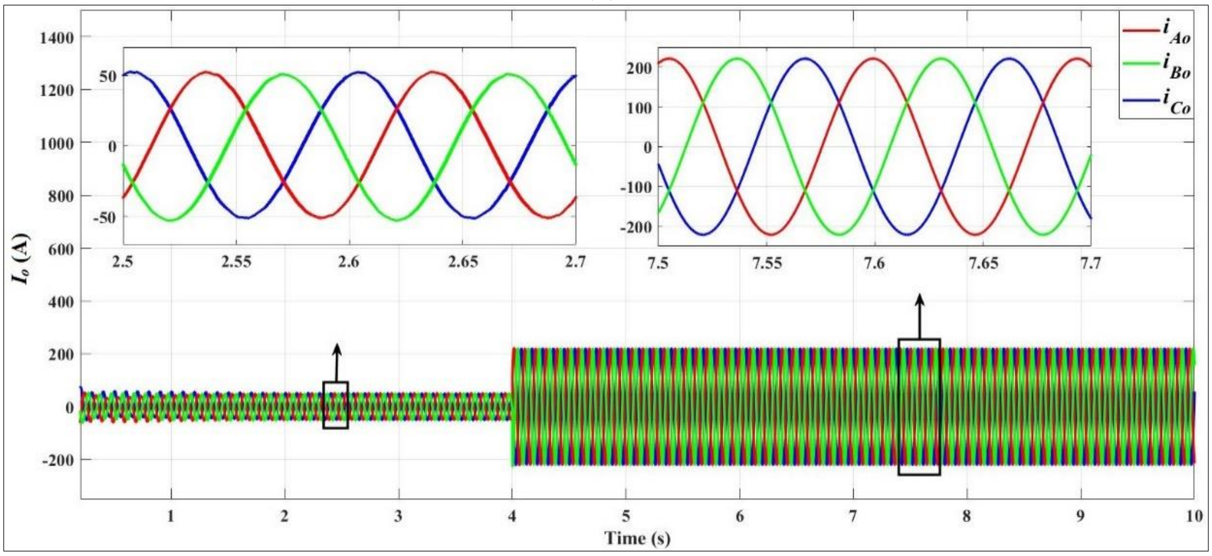


(c)

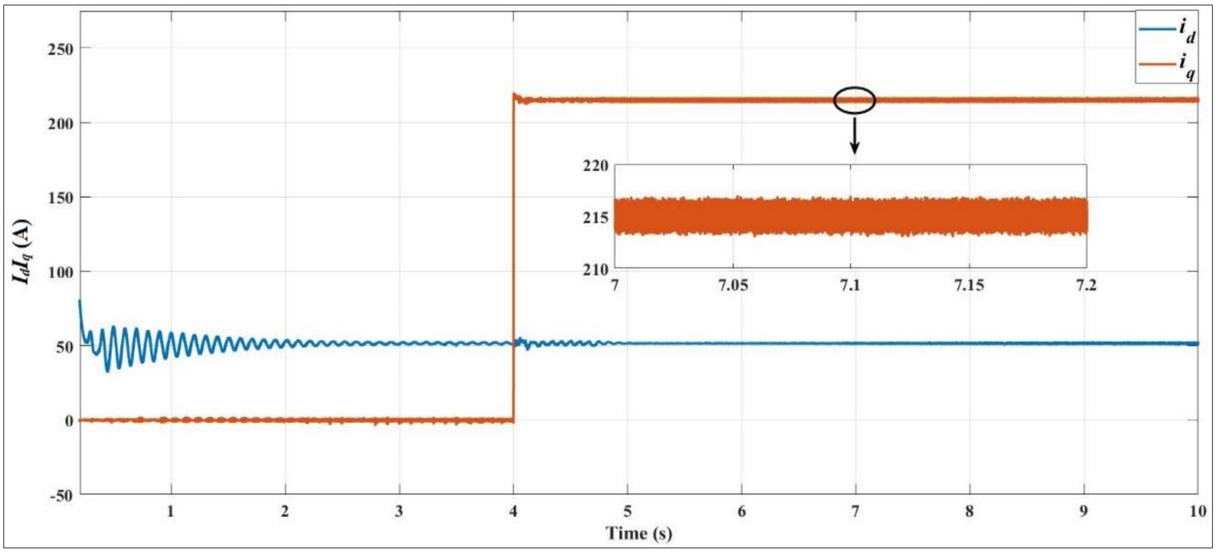
Fig. 12 (a) Switching Signal of Series Switch S_S, (b) DC-Bus Current, (c) DC Terminal Voltage.



(a)

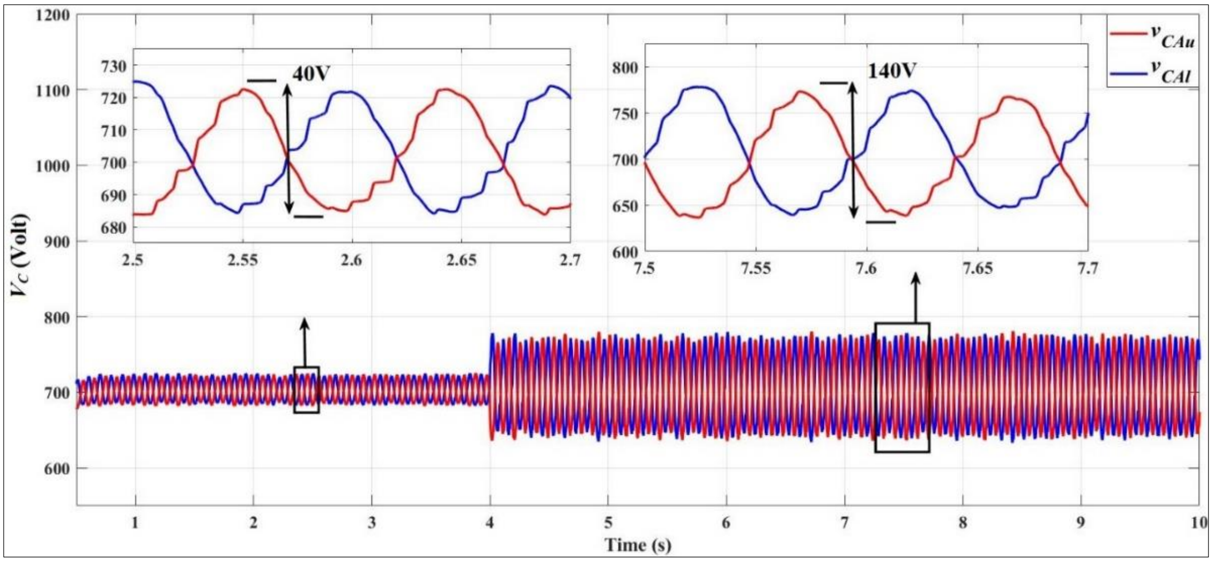


(b)

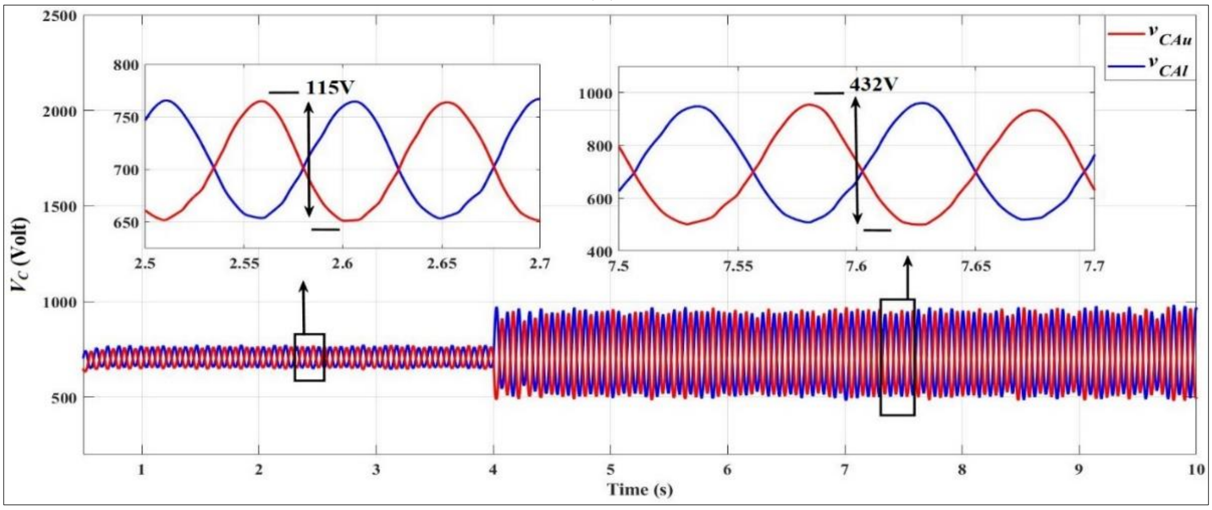


(c)

Fig. 13 (a) Load Torque and Motor Torque, (b) Stator Currents, (c) id, iq Currents Components of IM.

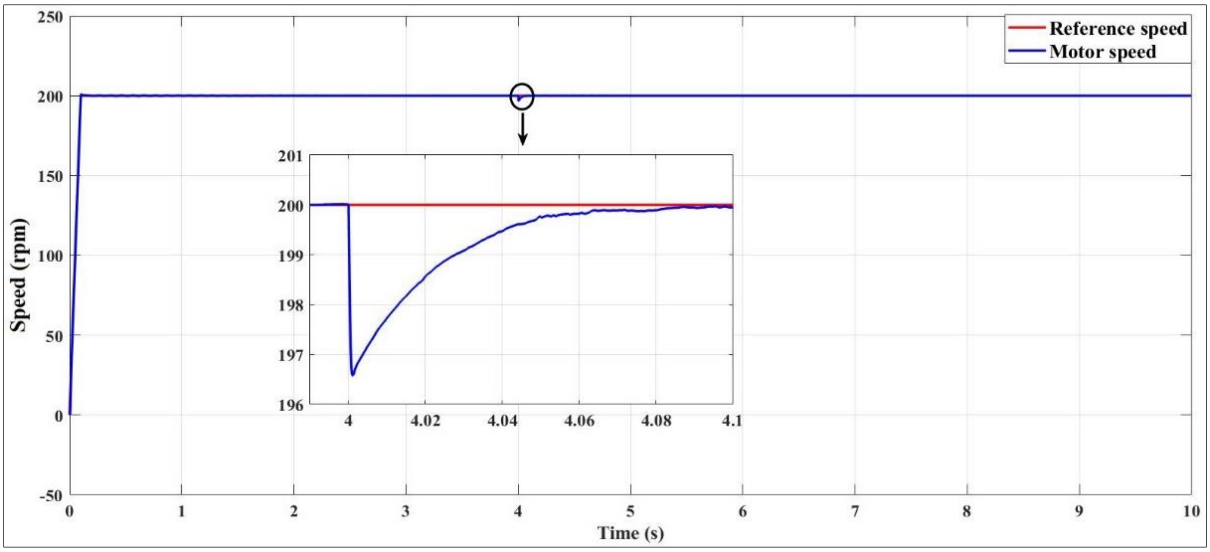


(a)

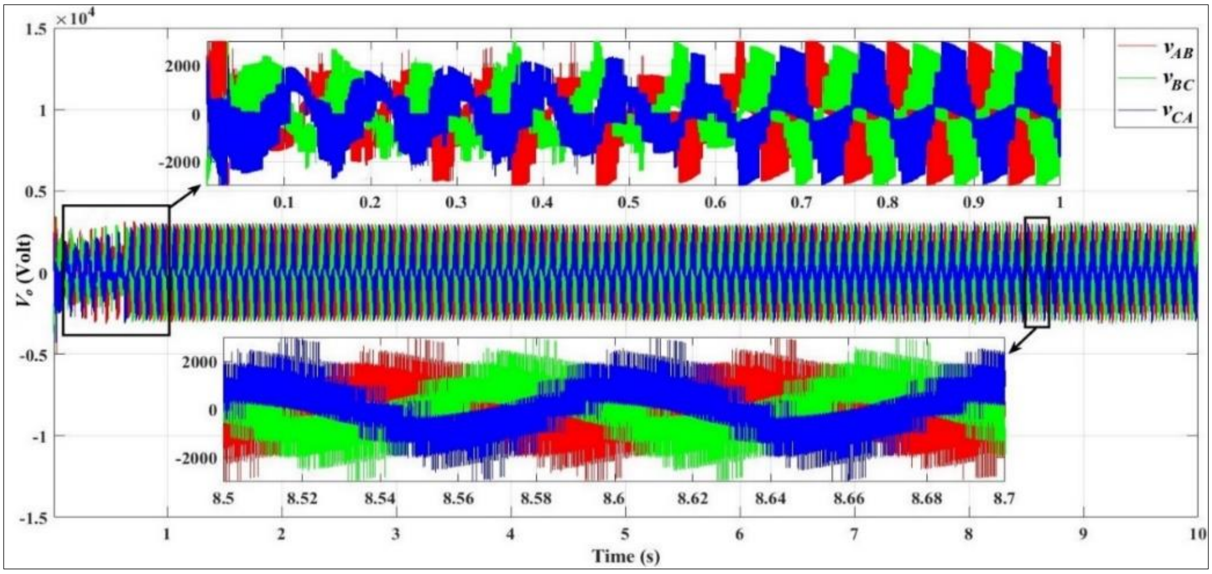


(b)

Fig. 14 (a) SM Capacitor Voltage of HMMC, (b) SM Capacitor Voltage of Conventional MMC.



(a)

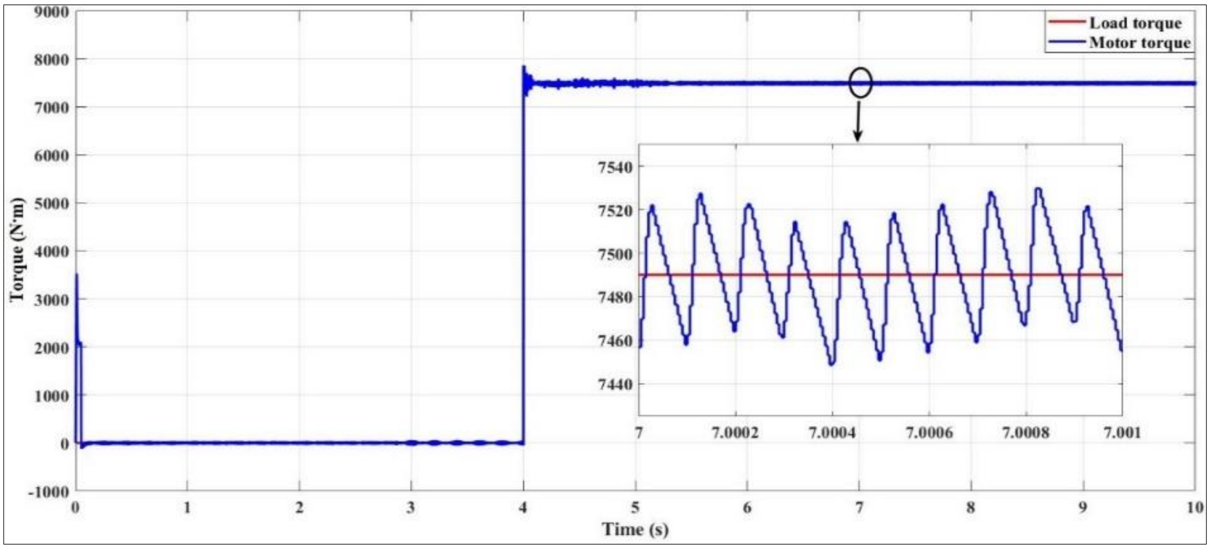


(b)

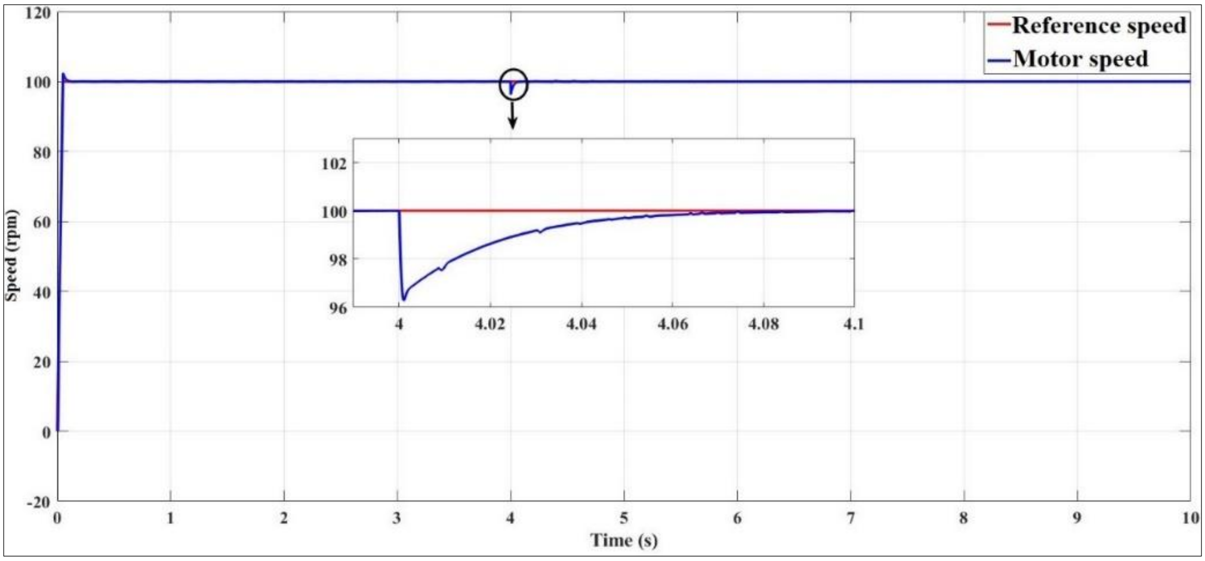
Fig. 15 (a) Motor Speed, (b) Output Voltage of the HMMC.

5.2.State 2:

In this state, the HMMC and conventional MMC operated at very- low frequency 5Hz. So the IM was operate at 100 rpm, after 4 sec a step load torque was applied with the rated value, at this point, the PI controller turned up the speed to the desired value of 200 rpm as shown in Fig.16 (a) and (b). As the load torque sharply increased, the stator currents increased to its rated value with high quality and smooth sinusoidal waveform, as shown in Fig. 17 (a) and (b) shows the DC-bus current that papered after every 0.02 sec (50Hz) with an amplitude of (38 A to 150 A). As the converter operated at a very-low frequency 5Hz, the peak-to-peak voltage fluctuation of the HMMC increased with an acceptable value of (60 V to 170 V) with an average voltage of 700 V because the action of Ss reduced the power ripple of the bridge arm, suppressing the peak-to-peak voltage fluctuation of the SM capacitor. While the peak-to-peak voltage fluctuation of the conventional MMC SM capacitor became a large-value of (225V to 860 V) with an average voltage of 700 V. Practically, the conventional MMC will fail to operate at low frequency, requiring increasing the SM capacitor capacitance, which increase the size and cost as shown in Fig. 18 (a) and (b). The converter output voltage was regulated to achieve the desired speed as shown in Fig. 18 (c).

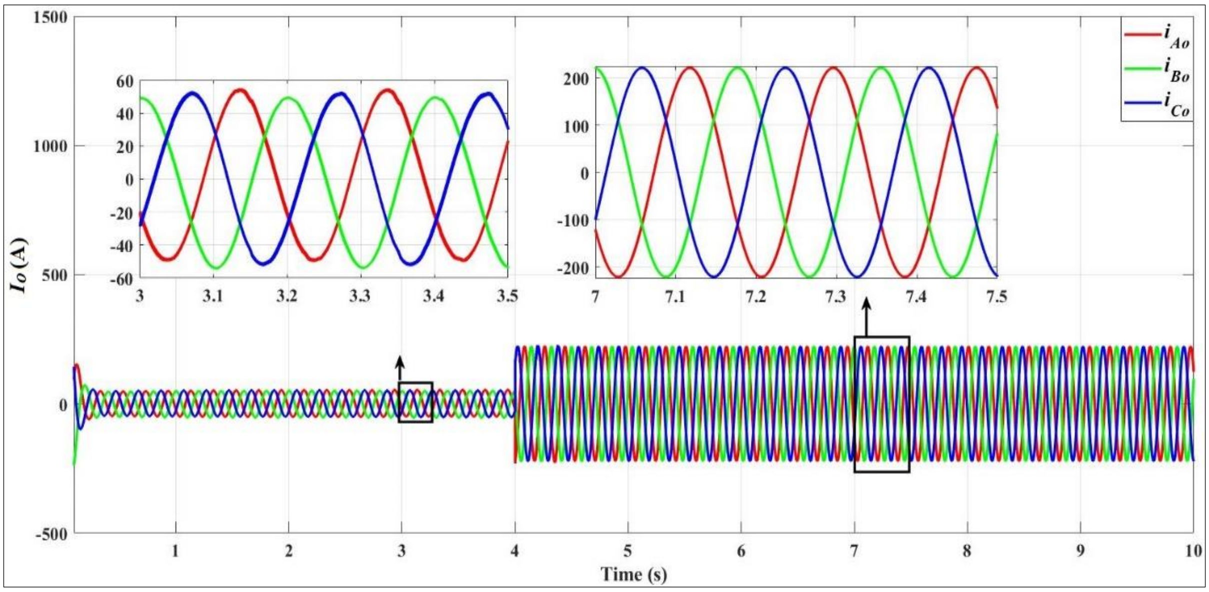


(a)

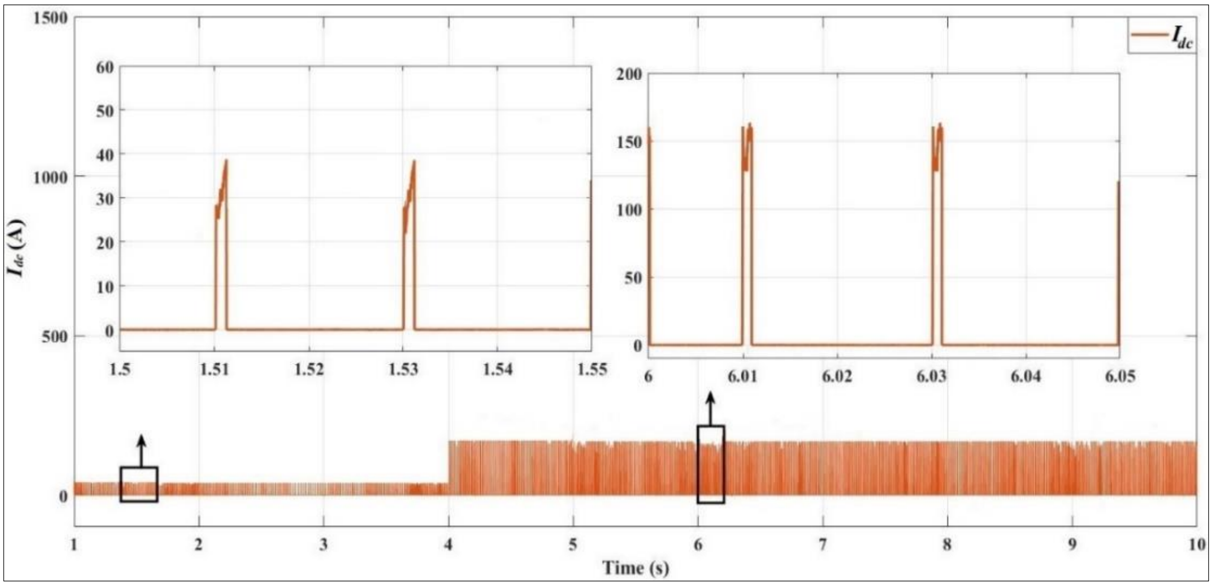


(b)

Fig. 16 (a) Motor Torque, (b) Motor Speed.

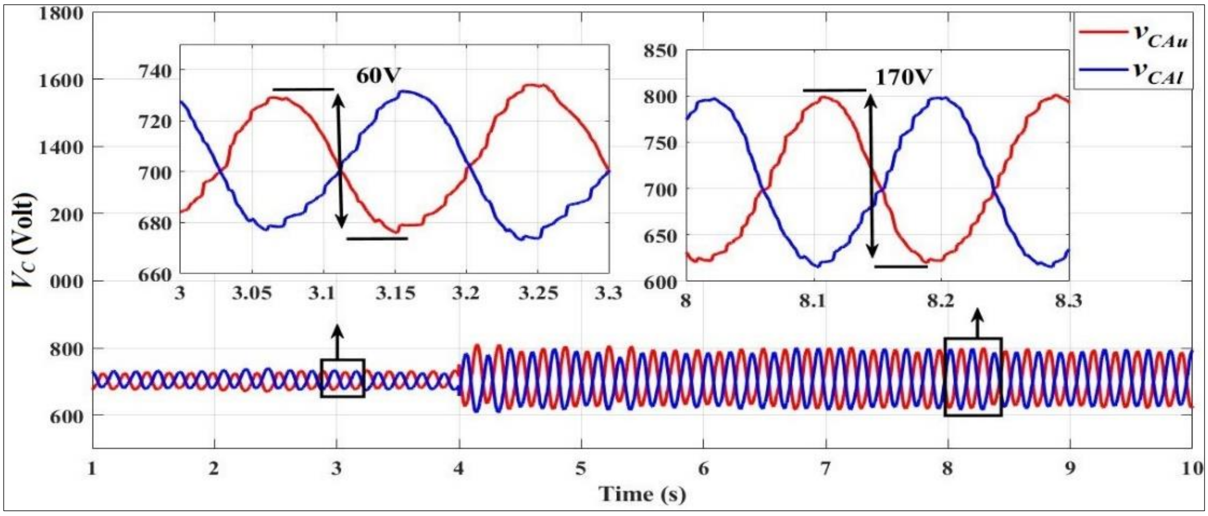


(a)

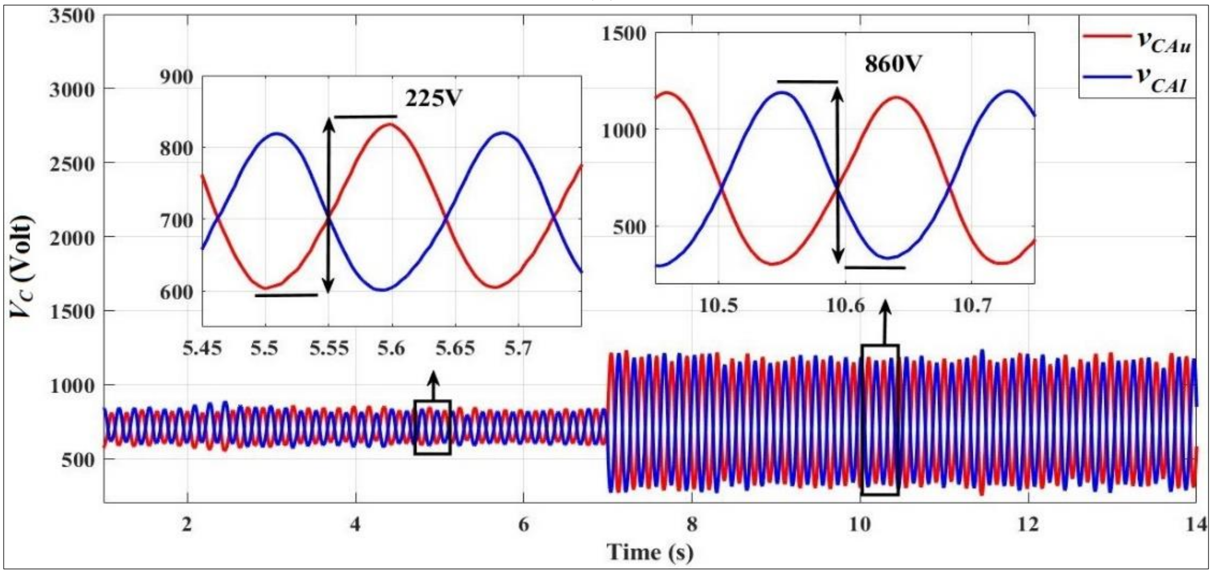


(b)

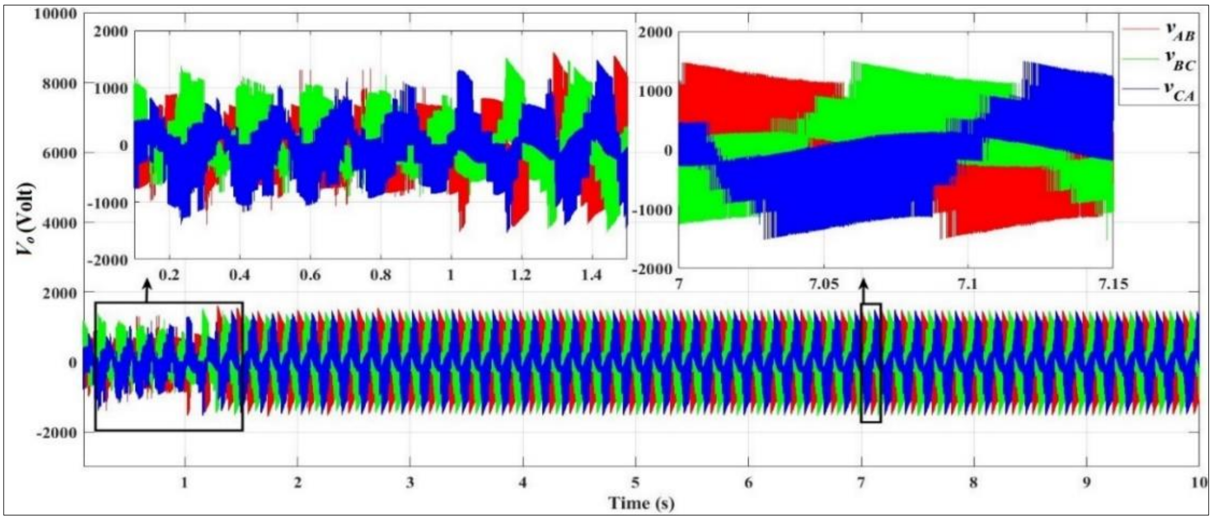
Fig. 17 (a) Stator Currents, (b) DC-Bus Current.



(a)



(b)

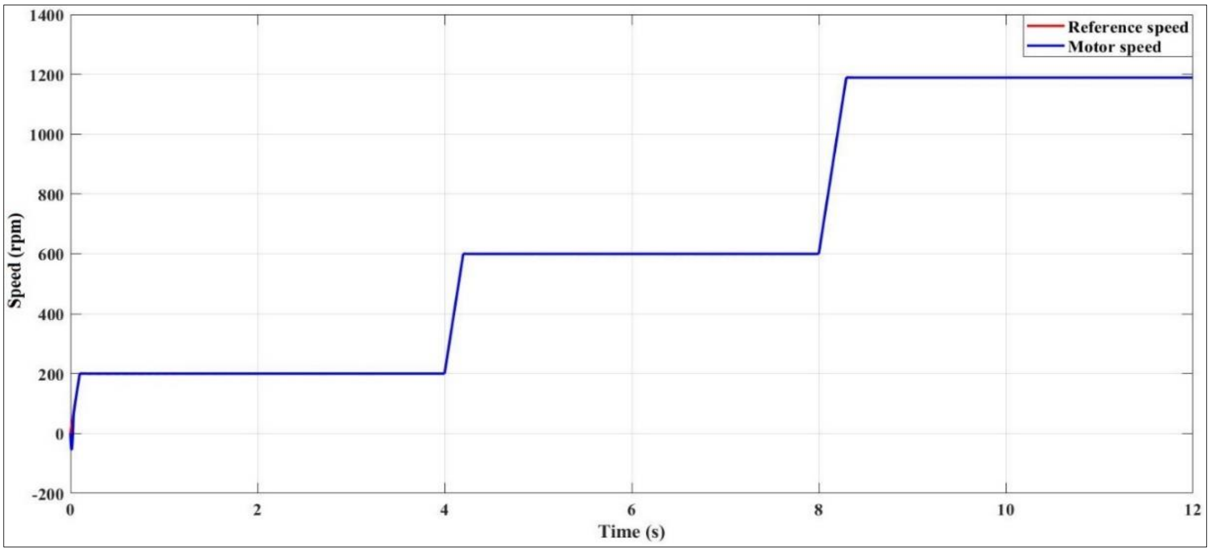


(c)

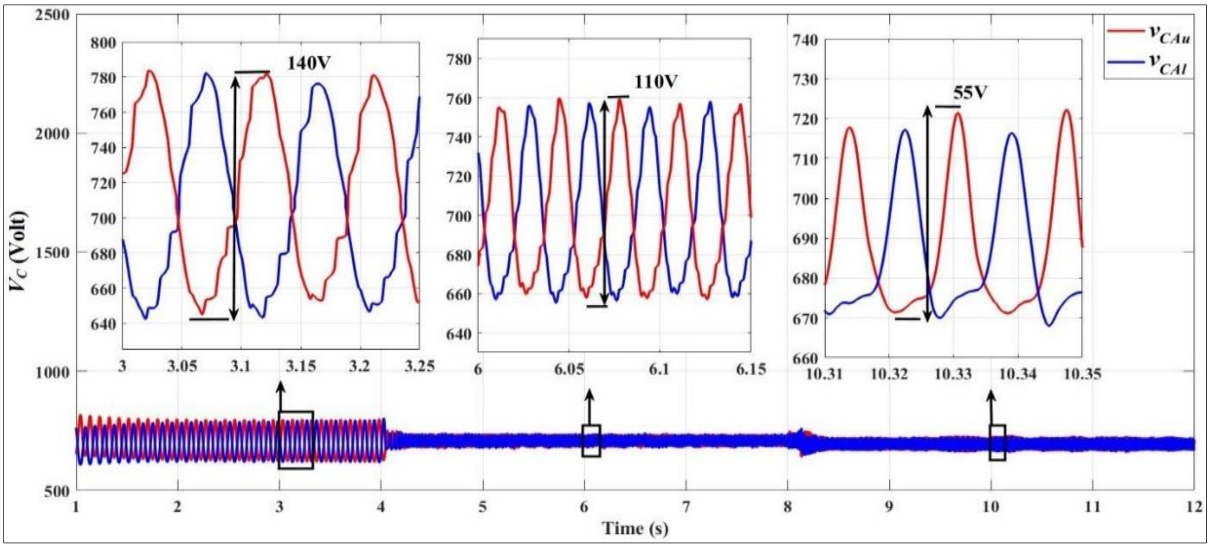
Fig. 18 (a) SM Capacitor Voltage of HMMC, (b) SM Capacitor Voltage of Conventional MMC, and (c) Converter Output Voltage.

5.3.State 3:

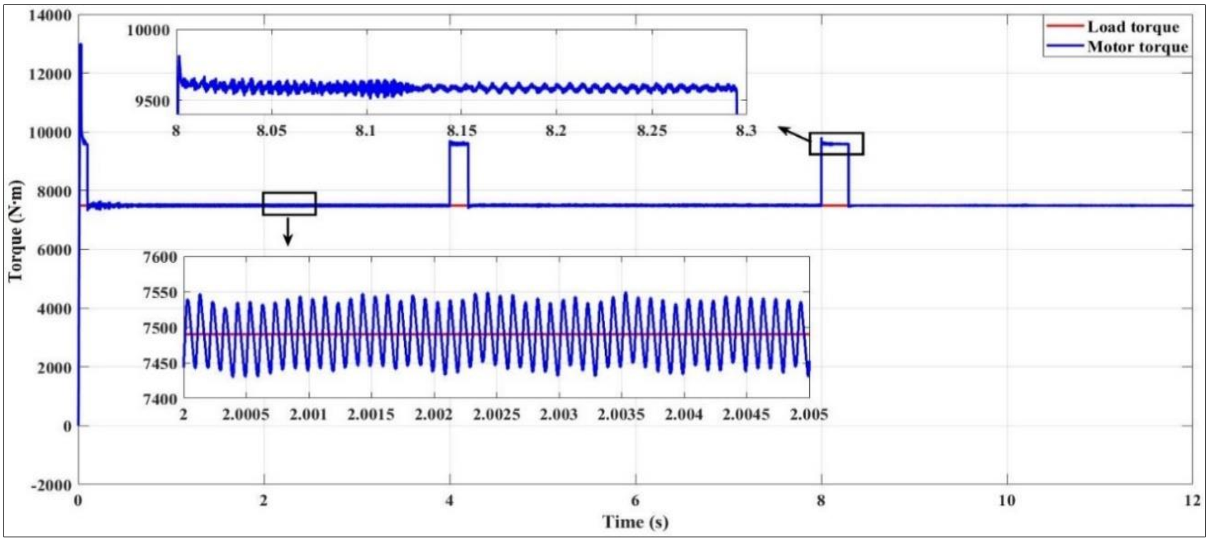
In this state, the HMMC operated with variable frequency for verifying the feasibility of the HMMC based on a vector control drive system with full load torque from a stand still. Form (0 to 4) sec, the HMMC drive motor operated at a low frequency of 10 Hz (200 rpm) with peak-to-peak voltage fluctuation of 140 Volt. After that, the motor speed was increased to its medium value of 600 rpm (25Hz), so the SM capacitor peak- to-peak voltage fluctuation was reduced to 110 V due to increasing frequency. Finally, the speed was increased to its rated value of 1189 rpm (50Hz). In this case, the HMMC operated as a conventional MMC because (D=m), and the peak-to-peak voltage fluctuation of the SM capacitor was 55 V as shown in Fig. 19 (a) and (b). As the motor speed was increased, the motor torque also, increased according to the torque equation of IM ($T_e = T_L + J\frac{d}{dt}\omega_r$), as shown in Fig. 19 (c). Increasing the applied load torque increased the stator currents with smooth sinusoidal waveform; and the iq current, which is proportional to toque, as shown in Fig. 19 (d) and (e). As the motor speed increased, the converter output voltages also increased, as shown in Fig. 19 (f).



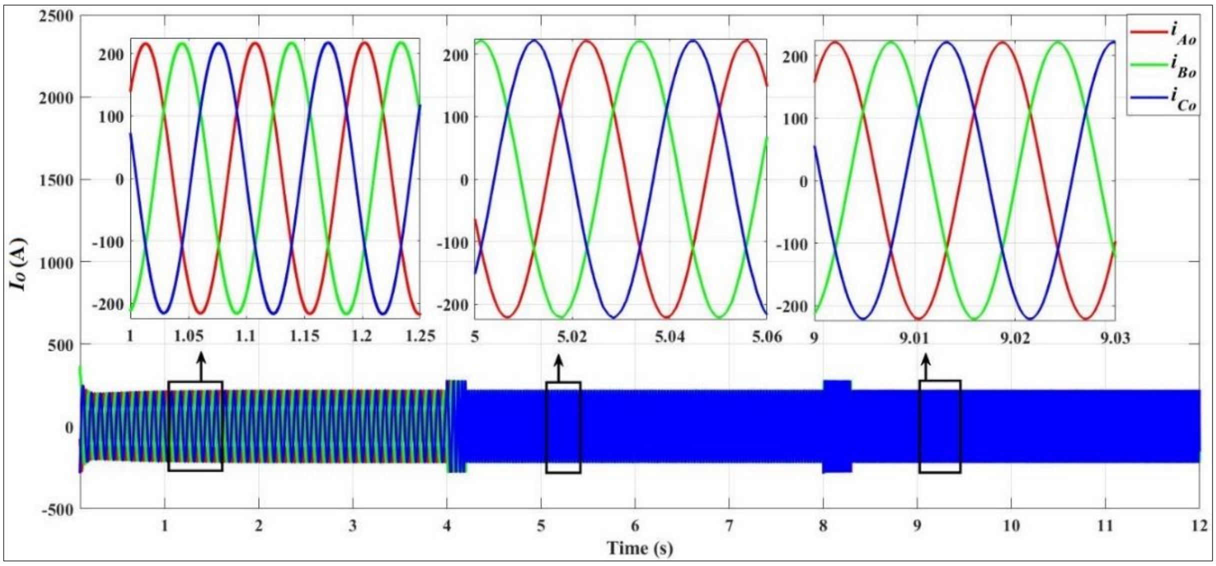
(a)



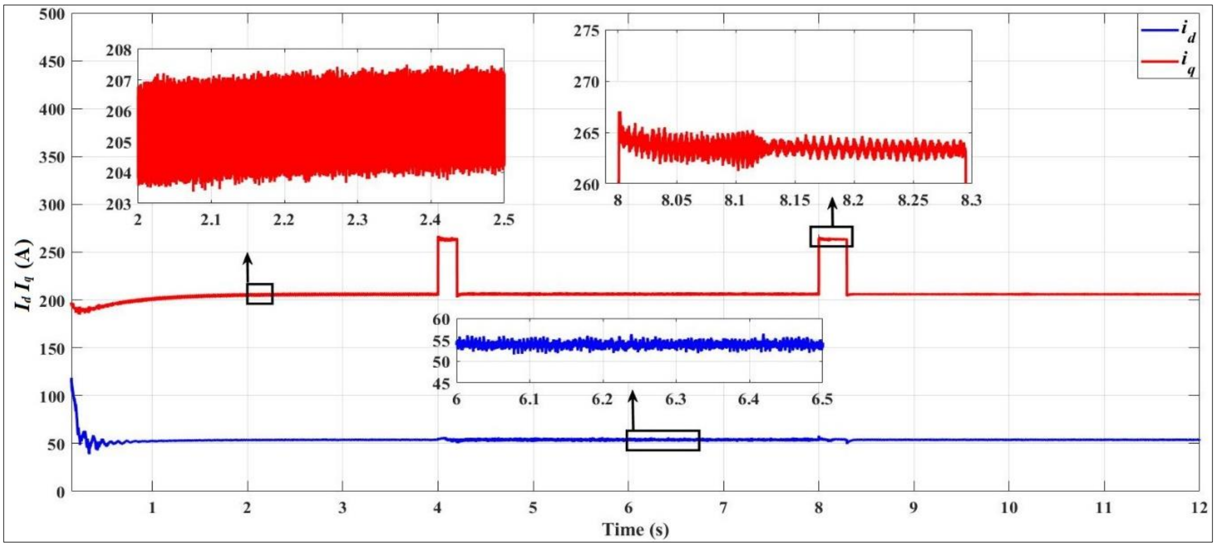
(b)


Load torque
Motor torque
Torque (N·m)
Time (s)

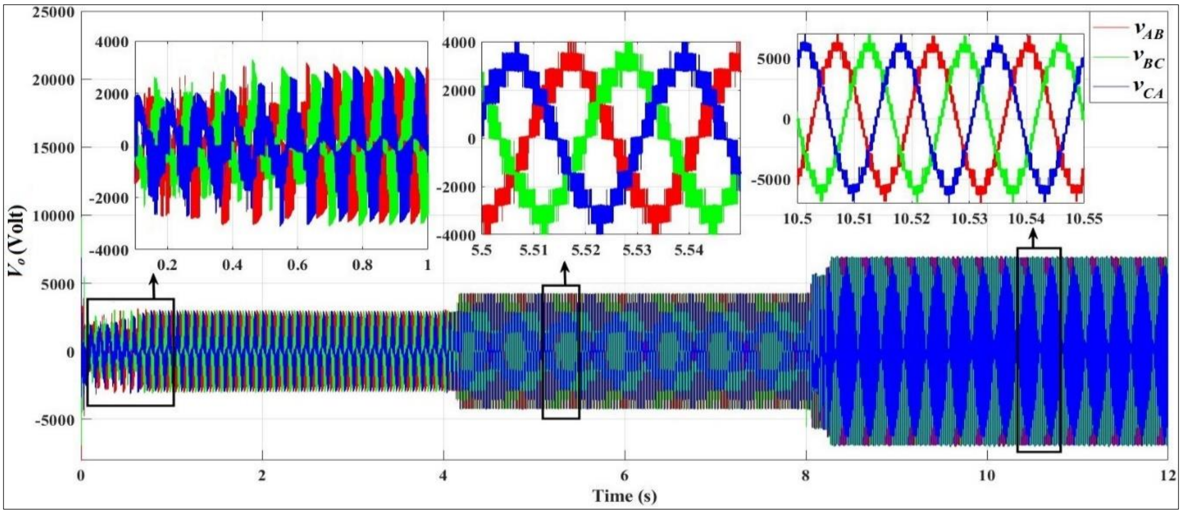
(c)


i_{Ao}
i_{Bo}
i_{Co}
I_O (A)
Time (s)

(d)


i_d
i_q
I_d I_q (A)
Time (s)

(e)



(f)

Fig. 19 (a) Motor Speed, (b) SM Capacitor Voltage of HMMC, (c) Motor Torque, (d), Motor Stator Currents, (e) id, iq Currents Components of IM, (f) Converter Output Voltage.

6.CONCLUSIONS

The main conclusions of the present study could be summarized as follows:

- This paper presented the HMMC to drive IM, and the simulation results showed the effectiveness of the HMMC for driving IM with full load at variable speed with high-quality sinusoidal waveforms of the voltage and current of the converter without adding any filter.
- The HMMC limited the SM capacitor voltage fluctuation without requiring increasing in the capacitance value of the SM capacitor, such as the conventional MMC, reducing the size and cost of the converter.
- The HMMC suppressed the voltage fluctuation of the SM capacitor without injecting common-mode voltage and circulating current reducing in the power losses, switching losses, current stress on the IGBT switches, and system cooling requirements.
- The simulation results showed the suppression the HMMC capacitor voltage ripple at a very-low frequency with a peak-to-peak voltage of the SM capacitor is 170V. While for conventional MMC, the voltage ripple of the SM capacitor was 860V, increasing the of conventional MMC capacitance.

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APPENDIX

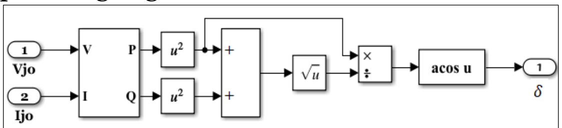
The M-file program of Series switch S_S triangular generator

```
function y = fcn (f,Ts)
t=1/10*f
if t<=Ts/2
y=2*t/Ts ;
else
y=2*(Ts-t)/Ts ;
end
```

The M-file program of average DC voltage of the SM capacitor

```
function s = fcn (u)
x=max u;
y=min u;
z=(x+y)/2;
s=z
```

The MATLAB/ SIMULINK to calculate the phase lag angle δ



V_{jo}= Converter output voltage per phase

I_{jo}= Converter output current per phase

P= Real power

Q= reactive power

S= Apparent power

$S = \sqrt{(P)^2 + (Q)^2}$

Power factor ($\cos\delta$) = S / P

$\delta = \cos^{-1}\frac{S}{P}$