MULTI –OUTPUT PHASE SHIFTER USING PHASE LOCKED LOOP [+]

مزيح الطور المتعدد بأستخدام حلقة مسك الطور

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Abstract:

This paper introduce the construction of multi-band phase shifter based on steps sweeping phase-locked loop (PLL).The desired phase shift can be selected to have any value between$(0 and \pi)$.In addition multi-phase shift output can be also obtained simultaneously. The phase shifter can be operated over a wide range of input frequencies.The maximum error of the phase shift is$\pm 1.8°$ which is controlled by the division factor (n).

المستخلص:

هذا البحث يعرض بناء منظومة انحراف طور الموجة بأستخدام حلقة مسك الطور الذي يمسح الترددات بخطوات . بأستخدام هذه المنظومة يمكن الحصول على فرق طور بين الموجة الداخلة والخارجة المختارة بأية قيمة محصوره بين$(0 - \pi)$ ولمدى واسع من الترددات الداخلة. يمكن الحصول على عدة مخارج بأزاحةأطوار مختلفه وفي نفس الوقت بغض النظر عن تردد الدخول . اكبر خطأ للطور بين الدخول والخروج في هذا البحث $\pm 1.8°$ والذي يمكن السيطرة عليه بواسطة عامل التقسيم (n).

Introduction

Frequency-independent phase shifting networks giving quadrature phase shift have a variety of applications in communications, electronic instrumentation & measurement.In $[1]$ a circuit which gives a digital$(rectangular)$output of only $\pi/2$ phase shift is described. Another technique$[2\&3]$is to utilize the property of the field effect transistor (FET) as an ohmic resistance channel whose value is a function of the gate to source voltage . However this concept has a limited frequency range owing to the limited linear region of the (FET). In$[4]$a (PLL) is used to give aphase-shift of only$\pi/2$.This paper is an outgrowth of$[4]$.The (PLL) is used in a different way to give multi-value phase shift output $(from\ 0\ to\ \pi)$simultaneously.The system has a wide range of input frequencies, limited only by the gain and saturation of the voltage controlled oscillator (VCO). The error of the phase shift is no more than π/n where (n) is the division factor in the feedback path of the(PLL) .Therefor the accuracy can be adjusted by varying the parameter. In this paper (n) is taken equal to 100 , hence the maximum error is $\pm 1.8°$.

Principle of operation

The block diagram of the system is shown in $Fig.(1)$. The principle operation of the phase shifter is basically to generate clock pulses whose frequency is a frequency multiple of the input frequency (if the input frequency is fo then the generated clock frequency is

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$n * fo$). These clock pulses are applied as triggering pulses to an m-bit shift register .The register is used for shifting ($delaying$) the input signal by an amount D given by:

$$D = m * clock\ period = m/(n * fo) \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Where m is the number of the output shift register used.

Therefore the input signal will be shifted in phase by an amount S given by:

$$S = wo * D = 2\pi fo * m/(n * fo) = 2\pi\,(m/n) \ldots\ldots\ldots (2)$$

A (PLL) which contains a divide by (n) circuit in the feedback path, is used to generate the required clock.This (PLL) is forced to lock onto the input frequency by changing the free running frequency of the (VCO)(after division)to be equal to the input frequency. The process of locking onto the input frequency is performed using two stages. The first stage is the coarse tuning loop which locks onto the input frequency, while the second stage is the fine tuning loop, where the phase error is adjusted to be no more than certain limits.

In the coarse tuning loop ($seeFig.1$) the VCO is made to sweep in steps .The VCO frequency is divided by (n). The divider output is phase shifted by $\pi/2$ through another shift register having $n/4$ stages, and applied to an auxiliary phase detector (APD) serving as a lock indicator .When the (PLL) is out of lock with the input signal the (APD) output is a sinusoidal signal which is attenuated by the decision filter Bd. Consequently the amplitude of the decision filter output is very low, and falls below the decision level б, hence the sweep signal is applied to the VCO input. As soon as the VCO frequency is brought to a value such that the frequency difference between the VCO and the input signal is less than Bd bandwidth, the (PLL) enters the lock condition.The filter output (after rectification) exceeds the threshold δ, the sweep signal is stopped and kept at its current value. At the same time, the fine tuning loop is initiated to adjust further the phase difference between the input signal and the divider output such that the error voltage of the (PLL) is within the limits of the window comparator threshold voltages. Once coarse tuning occurs, any sweep or drift in the input frequency is tracked by the fine tuning loop, and the system does not need to search through the whole frequency range.

System design

A prototype system has been designed as shown in $Fig(1)$. It consists of a second order (PLL) whose feedback path contains a divide by 100 circuit .The number of stages (m) of the shift register was chosen to be 50 in-order to provide an output phase shift ranging from ($0 to m$).

Coarse tuning loop:

The output of the divider circuit is applied to a shift register which provides a phase shift of $\pi/2$. The out put of the shift register is applied to the APD serving as a lock indicator .When the (PLL) is out of lock with the input signal the APD output is a signal which is attenuated by the decision filter **Bd**. As soon as the VCO frequency (after division) is brought to a value such that the frequency difference between the frequency divider output and the input signal is less than the **Bd** bandwidth, a DCcomponent is applied to the decision comparator.This in turn

stops the coarse tuning loop (searching loop) and initiates the fine tuning loop (tracking loop). The DC component applied to the decision comparator in the presence of noise is: [5&6]

$$Z = K1 \cdot exp(-\sigma^2) - (R/w^2)^2 \quad \ldots\ldots\ldots\ldots\ldots (3)$$

Where $K1$ is the APD gain constant, which is equal to $5.4V/rad$, σ is the standard deviation of the frequency divider fluctuation induced by noise R.The system sweep rate in rad/sec and wis the (PLL) natural frequency in rad/sec. For a noise free signal using the system parameters given later , Z is equal to $1.86V$.

The bandwidth of Bd should be very low and in any case less than the (PLL) capture range which is given by [5&6].

$$Capture\ range = 2(2K\xi w) \ldots\ldots\ldots\ldots\ldots (4)$$

Where ξ is the damping factor of the(PLL), K is the(PLL)loop gain in rad/sec The capture range is measured and then calculated to be $2.7KHz$.

When the decision filter has a very narrow band width the system will give a better performance[5&7]. This involves a relatively large decision delay which must be small in order to make the rapid decision necessary to stop the sweeping.However the decision filter bandwidth must be larger than the Frequency step(which is 390Hz in our system)caused by the sweeping generator in-order to prevent the actuation of the coarse tuning loop by this step. Other wise the system will restart searching and go out of lock ,the decision filter bandwidth is chosen to be equal to $500Hz$.

System sweep rate(R):

In the limiting case as the voltage step size is small and due to the integration process following the output of the sweep generator, the sweep voltage can be considered a linear ramp voltage . The sweep rate is chosen to guarantee an acquisition probability of 0.9 as given by [8]

$$R = 0.5^2(1 - 2\sigma) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

The sweep rate used in the system was $50KHZ/sec$

Fine tuning loop:

When the signal frequency is acquired by the coarse tuning Loop, the fine tuning loop is initiated . This acts to null any drift or sweeping in the input frequency, such that the (PLL) remains in lock and the system does not initiate any search. The polarity of the output voltage of the loop filter gives an indication of the increase or decrease in the input frequency .The loop filter output is applied to a window comparator.The thresholds of the window comparator are equal to $0.2V$. The aperture of the window has no effect on the phase error of the phase shift of the signal**.** However this aperture should not be too narrow in order not to be effected by the frequency step caused by the sweep generator, otherwise the system may oscillate. Also this aperture should not be too wide so that the (PLL) may loose lock beforethe signal being sensed and tracked by the fine tuning loop .The aperture of the window comparator imposes additional limits on the choice of the frequency step. This step should not give a transient error voltage greater than $0.4V$(the widow comparator aperture)at the input of the window comparator , otherwise the system may oscillate.

Results and conclusions:

The system designed was practically implemented.The rang of operation is $100KHz$ and the center of operation is determined by the free running frequency of the VCO, it can therefore be adjusted according to the requirements .The over all system parameters are given below: [7&9].

a) PLL parameters

loop gain K rad/sec ω rad/sec	VCO gain MHz/V in dB	natural frequency KHz	damping factor	capture range
124536	5	918	0.65	2.7

(b) Sweep generator parameters

1 An 8-stage up-down counter is used.
2 The counter clock rate is equal to $128Hz$.
3 The peak to peak output voltage of the sweep generator is equal to $2V$.
4 The range of input frequencies which can be handled by the system is $100KHz$ for a VCO gain constant after division of $50KHz/V$.
5 The frequency step size is equal to $10^5/2^8$, i.e $390Hz$.
6 The system sweep rate $R = clock\ rate * frequency\ range\ /256 = 50KHz/sec$
7 The maximum system sweep rate for a noise free input using (equation3)is equal to $67KHz/sec$.

(c) The decision filter band width is equal to $500Hz$.

(d) The threshold of the decision comparator is equal to $0.39V$which is equal to $0.5 * Z$since thisleads to a minimum dispersion on the stop sweeping instant [5].

(e) The window comparator thresholds are equal to $0.2V$.

(f) A 12 -stages shift register CMOS IC (45905) are used .

$Fig.(2)$ shows the wave forms of the phase shifter for an input signal and different phase shifted outputs . From practical measurements, it is observed that the error in the phase shift did not exceed π/n .This fact can be explained as follows:

Since the generated clock is not necessarily in exact phase with the input frequency (although still in lock), then the maximum error expected in the phase shifted output is one half the clock period i.e. $1/2(nfo)$. Therefore the maximum error in the phase shift S is given by:

$$\text{Max . Error in } S = \omega_o * \text{max. error in D}$$

$$= \omega_o * 1/(2nFo) = \pi/n \ldots\ldots\ldots(6)$$

In order to demonstrate the response and the tracking capability of the system to a sweeping input signal .$Fig.(3)$shows the error voltage of the window comparator input during the tracking of an FM signal modulated by a triangular waveform .It can be noticed from $Fig.(3)$ that the fine tuning loop tries toreduce the error voltage of the (PLL) such that it remains within $+0.2V$. The output of the sweep generator and the search /track control are shown in $Fig.(4)$. Here the system was forced manually to loose lock by a sudden change in the input frequency, so as to illustrate the searching and tracking operation . The system described above can be easily manufactured and can be used in many application. Any phase

shift from $(0 to \pi)$ can be obtained with accuracy depending on n. This phase shifter is an outgrowth of the system introduced in [4] with added grater flexibility and accuracy.

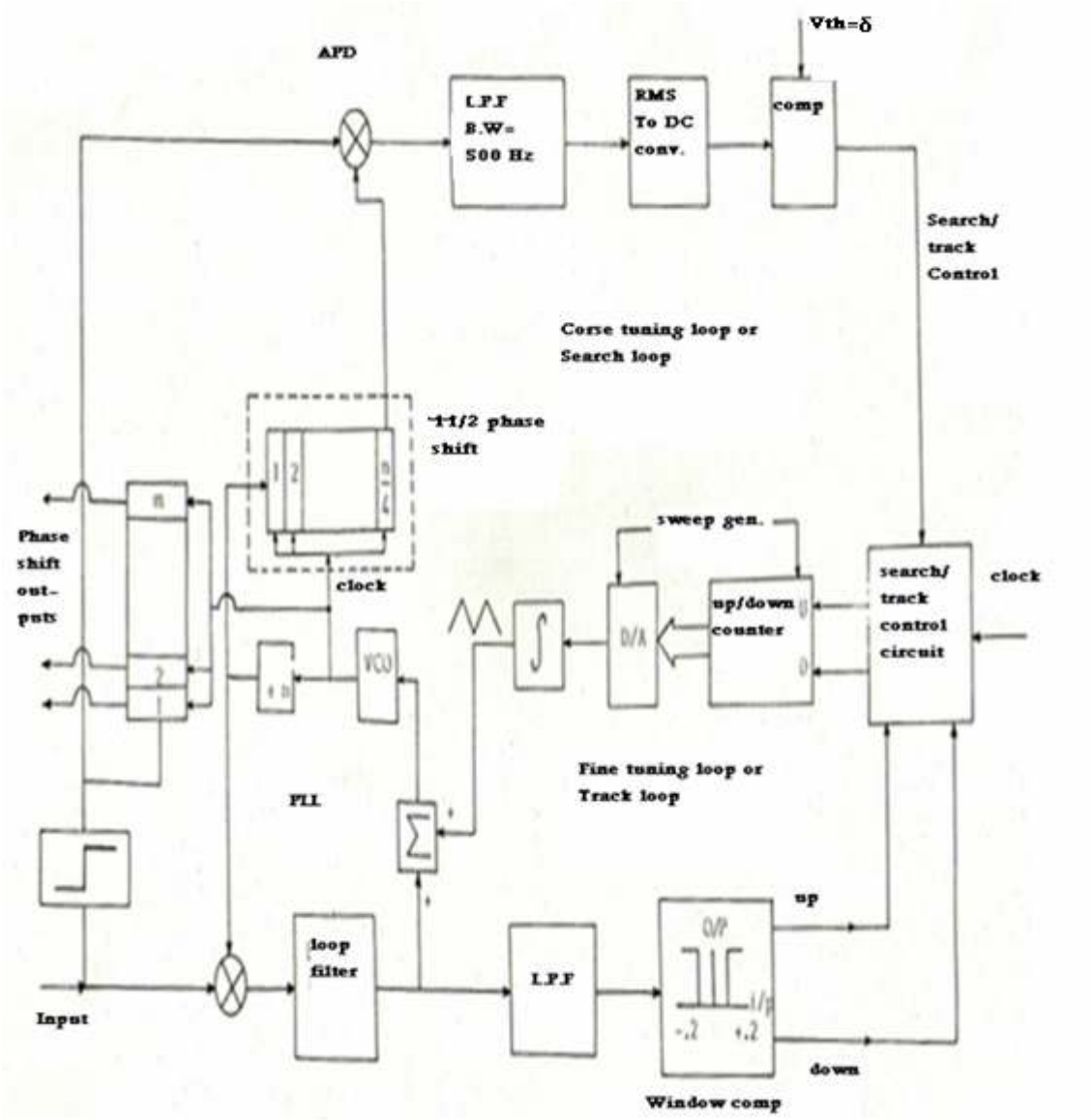

Fig.(1) Detailed block diagram of the system .

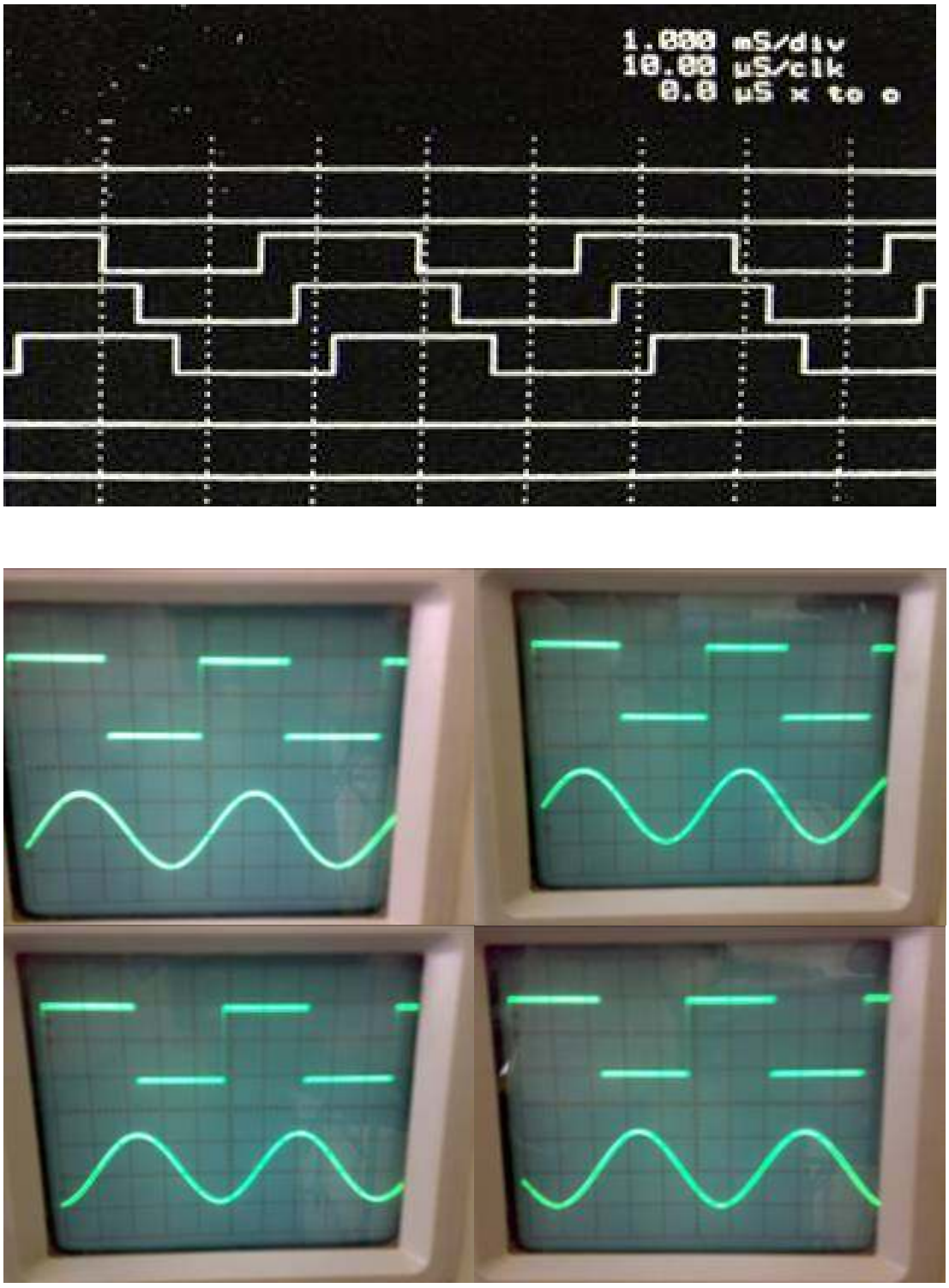

Fig. **(2)** Input signal and its different phase shifted outputs .

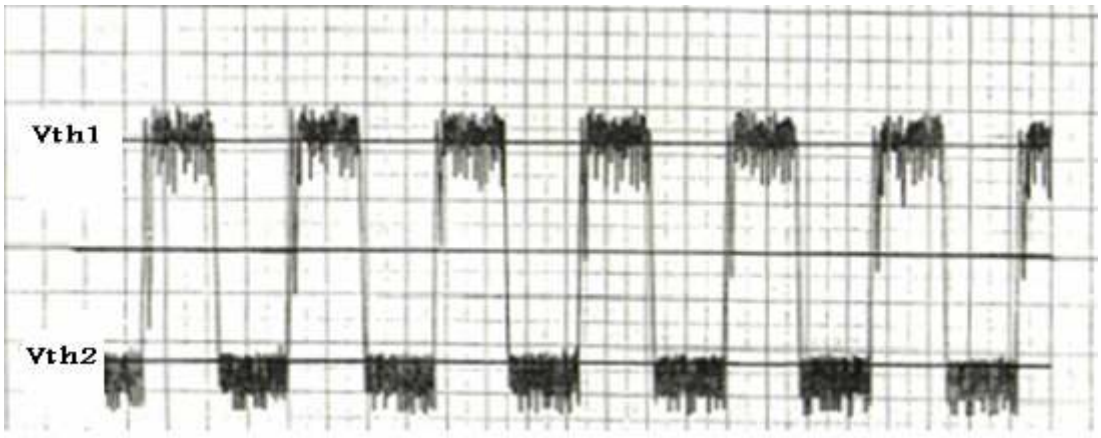

Fig. **(3)** The error voltage at the input of the window comparator during tracking an ***FM*** signal modulated by a triangular signal **.**

Time base= **1*sec./cm.***

Sensitivity=**0.1*volt/cm.***

(Vth1&*Vth2* are the threshold voltages of the window comparator)

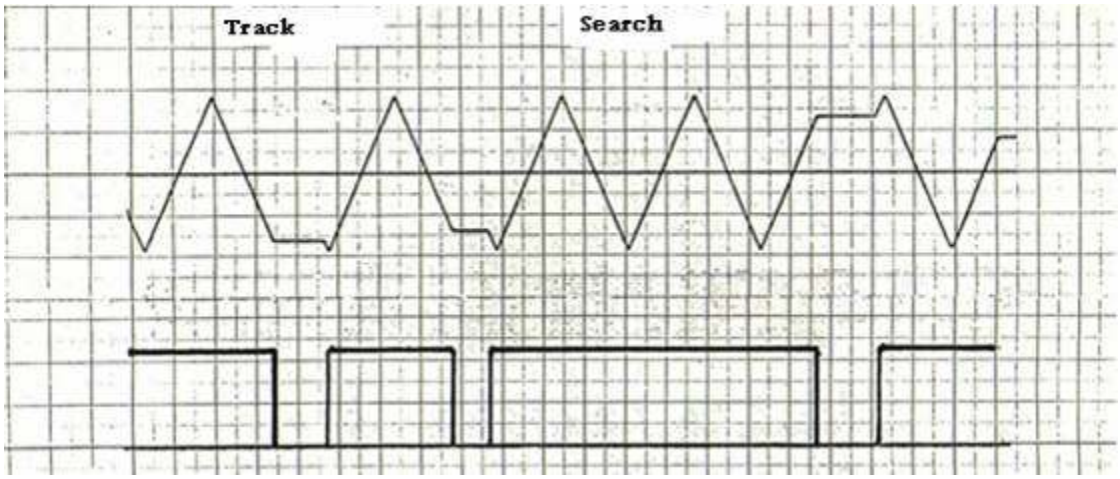

Fig. **(4)** Upper :The output of the sweep generator during searching and locking onto a stationary signal

Lower :The output of the search/track control.

Timebase **=** **1*sec./ cm.*** **(*forboth*).**

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