Design and Implementation of JPEG 2000 Image Compression using FPGA

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Abstract

This paper investigates the use of a Field Programmable Gate Array (FPGA Xilinx Virtex-II) to perform hardware implementation for low speed part of JPEG2000 to achieve a real time JPEG2000 system.

In this paper multi processes modules written in the VHDL is proposed that can be used to accelerate an existing software implementation of JPEG2000.

الخلاصـــــة

يبحث هذا العمل استخدام مصفوفة البوابات المبرمجة الواسعة لتنفيذ تصميم الجزء بطيء السرعة في طريقة كبس الصور ***(JPEG2000)*** *للحصول على نظام كبس الصور* ***(JPEG2000)*** *بزمن حقيقي.*

في هذا العمل تم تقديم عمليات متعددة تم كتابتها بلغة ***(VHDL)*** *وهي اللغة المستخدمة لوصف الأنظمة الرقمية والتي تؤدي إلى تسريع تنفيذ نظام كبس الصور* ***(JPEG2000).***

1. Introduction

With the increasing usage of multimedia technologies, image compression requires higher performances as well as new features. To address these needs in the specific area of continuous tone still image encoding, a new standard is currently being developed, the JPEG2000.

A VHDL implementation of the low speed part of JPEG2000 is presented, suitable for implementation on an FPGA. An FPGA is a general-purpose, multi-level, programmable device with a very high logic density that allows the user to implement logic circuits in a very short period [1,2]. The presented design has been verified in simulation using ISE4.1i software.

The scheme of fast lifting wavelet transform (FLWT) is selected as fast implementation of Discrete Wavelet Transform and the optimal method for adder/subtractor is proposed in order to reach minimum cost and high speed requirements. Also, multi types of spatial storages are designed to hold the needed data according to the sequence of data access and for faster future process.

The implementation of the system designed is achieved using Xilinx Virtex-II/x2v2000 platform as a suitable selected programmable device.

2. JPEG 2000 Standard

JPEG2000 is an image compression standard being developed by the Joint Photographic Experts Group (JPEG). Work on the JPEG-2000 standard commenced with an initial call for contributions in March 1997 [3,4]. The purpose of having a new standard was twofold. First, it would address a number of weaknesses in the existing JPEG standard. Second, it would provide a number of new features not available in the JPEG standard [5].

The preceding points led to several key objectives for the new standard, namely that it should:

- **i.** Allow efficient lossy and lossless compression within a single unified coding framework.
- **ii.** Region of interest coding, whereby different parts of an image can be coded with differing fidelity.
- **iii.** Progressive recovery of an image by fidelity or resolution.
- **iv.** Random access to particular regions of an image without needing to decode the entire code stream.
- **v.** A flexible file format with provisions for specifying information and image sequences.
- **vi.** Good error resilience [5,6,7].

Due to its excellent coding performance and many attractive features, JPEG 2000 has a very large potential application base. Some possible application areas include: image archiving, Internet, web browsing, document imaging, digital photography, medical imaging, remote sensing, and desktop publishing [8,9].

3. The JPEG 2000 Algorithm

Having briefly introduced the JPEG-2000 standard, it is now possible to begin examining the JPEG-2000 codec in detail. The codec is based on wavelet/subband coding techniques [8].The same algorithm can be used for lossy and lossless compression.

The general structure of the codec is shown in **Fig.(1)** with the form of the encoder given by **Fig.(1-a)** and the decoder given by **Fig.(1-b)**. From these diagrams, the key processes associated with the codec can be identified as follows: preprocessing/postprocessing, intercomponent transform, intracomponent transform, quantization/dequantization, tier-1 coding, tier-2 coding and rate control.

The decoder structure essentially mirrors that of the encoder. Each functional block in the decoder either exactly or approximately inverts the effects of its corresponding block in the encoder. Since tiles are coded independently of one another, the input image is (conceptually, at least) processed one tile at a time [5,8]. In the sections that follow, each of the above processes is examined in more detail.

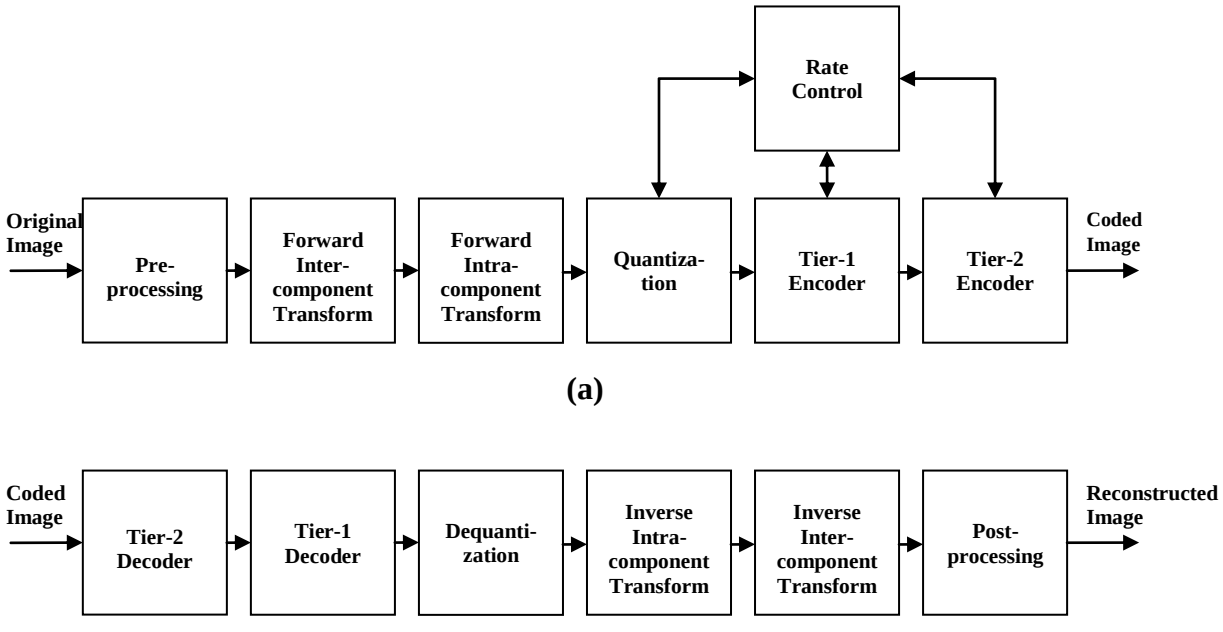


Figure (1) JPEG2000 codec structure
(a) encoder, and (b) decoder

3-1 Preprocessing/Postprocessing

From the point of view of JPEG2000, an image is a collection of components, where each component consists of a rectangular array of samples called tiles. In the signed and unsigned cases, the component sample values have a nominal dynamic range of $[-2^{P-1}, 2^{P-1}-1]$ and $[0, 2^{P}-1]$ respectively. If the sample values are unsigned, the nominal dynamic range is clearly not centered about zero. Thus, the nominal dynamic range of the samples is adjusted by subtracting a bias of 2^{P-1} from each of the sample values. If the sample values for a component are signed, the nominal dynamic range is already centered about zero, and no processing is required [8, 10].

3-2 Intercomponent Transforms

This transformation is active in the case of an input images represented in the RGB space color; it allows then the transformation of an image into the YCrCb space. This transformation operates on the entire component together, and thus, serves to reduce correlation among them in order to obtain a more performing coding. The standard supports two different component transformations, one irreversible component transformation (ICT) that can be used for lossy coding and one reversible component transformation (RCT) that may be used for lossless and/or lossy coding [5].

3-3 Intracomponent Transform

Each tile component of an input image is transformed into different resolution levels. These decomposition levels contain a number of subbands, which consist of coefficients that describe the horizontal and vertical spatial frequency characteristics of the original tile component. Due to the statistical properties of these subband signals, the transformed data can usually be coded more efficiently than the original untransformed data.

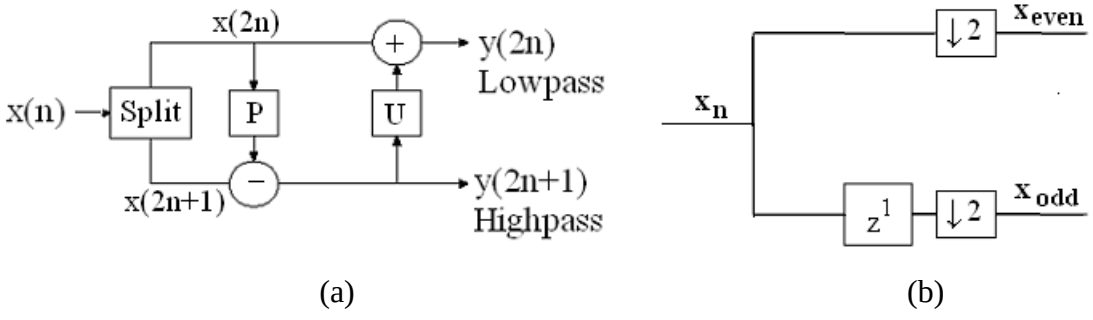
JPEG2000 baseline part I supports two filter banks. The first is based on 5/3 wavelet filters, reversible and integer-to-integer. Usually, it is used for lossless compression. The second is based on 9/7 wavelet filters [8], non-reversible and real-to-real which are used for lossy compression.

Fast Lifting Wavelet Transform-based filtering consists of a sequence of very simple filtering operations for which alternately odd sample values of the signal are updated with a weighted sum of even sample values, and even sample values are updated with a weighted sum of odd sample values as shown in **Fig.(2)**. For the reversible (lossless) case the results are rounded to integer values. The lifting-based filtering [9, 11, 12, 13, 14] for the 5/3 analysis filter is achieved by means of:

$$y(2n+1) = x(2n+1) - \lfloor P \rfloor \quad \text{..... (1)}$$

$$y(2n) = x(2n) + \lfloor U \rfloor \quad \text{..... (2)}$$

where: $P = \frac{1}{2}\left(x(2n+2) + x(2n)\right)$, $U = \frac{1}{4}\left(y(2n+1) + y(2n-1)\right)$.



(a) (b)

Figure (2) The forward fast lifting scheme
(a) forward transform, (b) split step described using down sampling and delay

3-4 Quantizations

The transform coefficients are quantized with a deadzone scalar quantizer. A different quantizer is employed for the transform coefficient of each subband. In the case of lossy coding, the quantizer step size is chosen in conjunction with the rate control. In the lossless case, the quantizer step sizes are forced to be one [8].

3-5 Tier-1 Coding

Tier-1 coding is the first of two coding stages. The quantized indices for each subband are partitioned into code blocks. Code blocks are rectangular in shape, typically 64x64. After a subband has been partitioned into code blocks, each of the code blocks is independently coded using the bit-plane coder [10].

The code block is partitioned into horizontal stripes, each having a nominal height of four samples. The stripes are scanned from top to bottom and from left to right. There are three coding passes per bit plane:

i. Significance pass.
ii. Refinement pass.
iii. Cleanup pass [5].

3-6 Tier-2 Coding

The input to the tier-2 coding process is the set of bit-plane coding passes generated during tier-1 coding. In tier-2 coding, the coding pass information is packaged into data units called packets. The resulting packets are then output to the final code stream. A packet is nothing more than a collection of coding pass data [5].

3-7 Rate Control

In the encoder, rate control is achieved through two distinct mechanisms:

1) The choice of quantizer step sizes, and

2) The selection of the subset of coding passes to include in the code stream.

The standard does not specify how these mechanisms should be employed, and it is possible to use either mechanism exclusively or both together [8].

4. The Proposed JPEG2000 Encoder System Design

The system of the JPEG2000 encoder can be divided into two categories low speed part and high speed part depending on the speed and the complexity of their operations needed as shown in **Fig.(3)**.

Low speed part consists of Preprocessing (Pre.), Forward Intercomponent Transform (Color Tr.) and Forward Intracomponent Transform which named as Fast Lifting Wavelet Transform (FLWT). This requires continuous configurations, computations and parallel execution compared to high speed part which consists of Quantization (Quan.), Tier-1 Encoder, Tier-2 Encoder and Rate Control (RC).

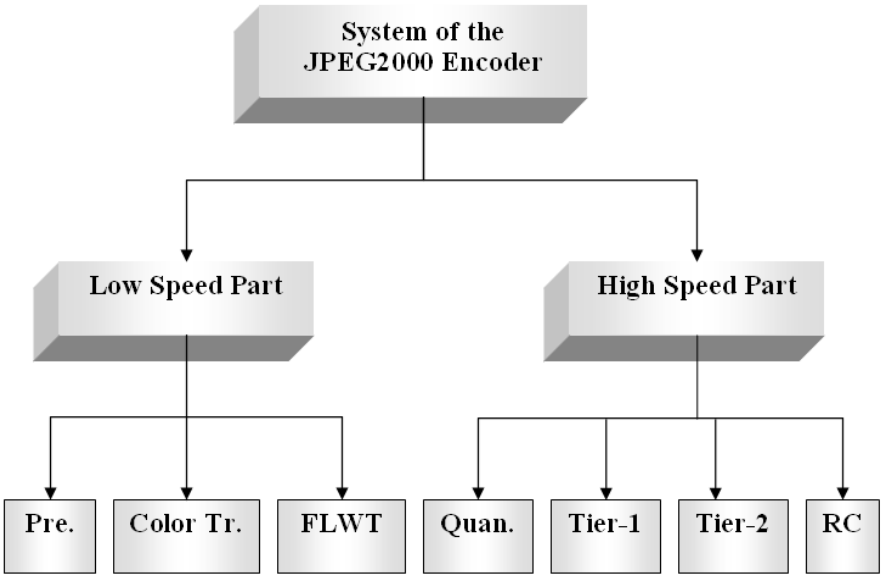


Figure (3) General parts of JPEG2000 encoder system

Thus low speed part of JPEG2000 encoder system will be implemented in hardware (H/W) platforms using FPGA to accelerate their operations for high-seed applications. This is to be compatible with the real-time that will be discussed later in the next section. High speed Part of JPEG2000 algorithm does not need to be implemented in hardware because it can be executed using software programming.

5. Low Speed Part of JPEG 2000 Encoder Implementation

This unit represents the proposed design for the low speed part of the JPEG2000 image compression system encoder. The implementation of this unit can be done as in the structure labeled as SYSTEM shown in **Fig.(4)**.

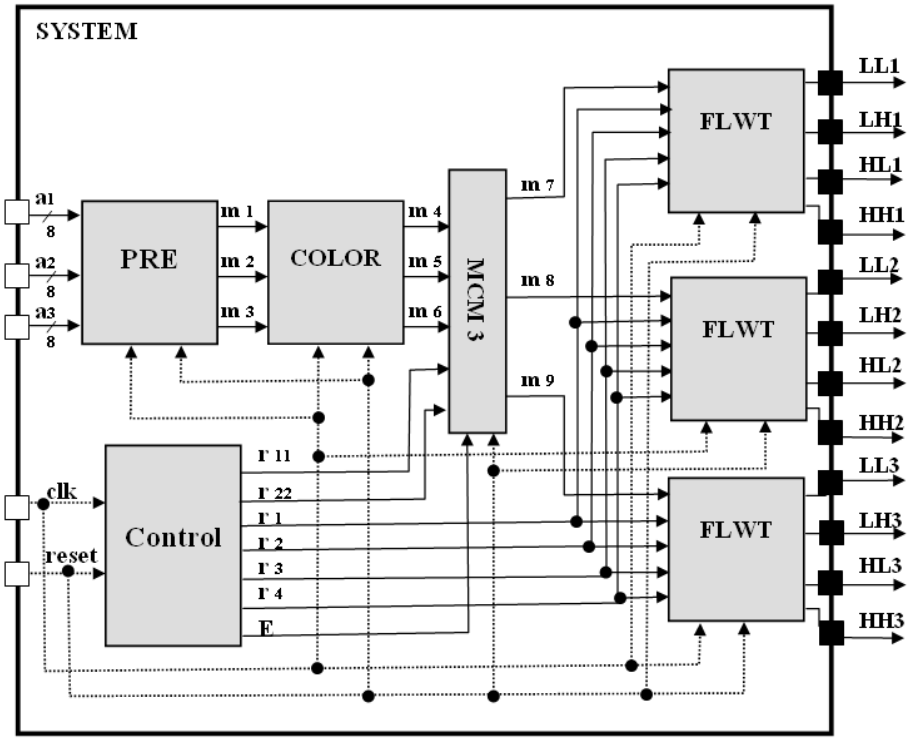


Figure (4) The structure of SYSTEM unit

The structure of this unit consists of the following components:

- PRE unit which is the first stage of the system algorithm as demonstrated in section (3-A).
- COLOR unit that represents the second stage of the system algorithm as explained in section (3-B).This unit is designed using an optimal method for adder/subtractor which is selected here and that according to the characteristics of Xilinx FPGA in order to achieve an optimal speed/cost for the design of the 8-bit and 9-bit adder. The basic idea of this method will depend on splitting the design into groups of 2-bit adders to decrease the delay to half.
- Storage unit named as MCM3 used to store the output data of COLOR unit. The design of this unit has memory unit and counter unit for addressing. **Figure (5)** shows the structure implementation of this unit that consists of one six bit up counter unit and three units of memory 64 (2^6 ×8) which are used to store each transformed color plane separately to be accessed simultaneously in the next operation at FLWT unit.

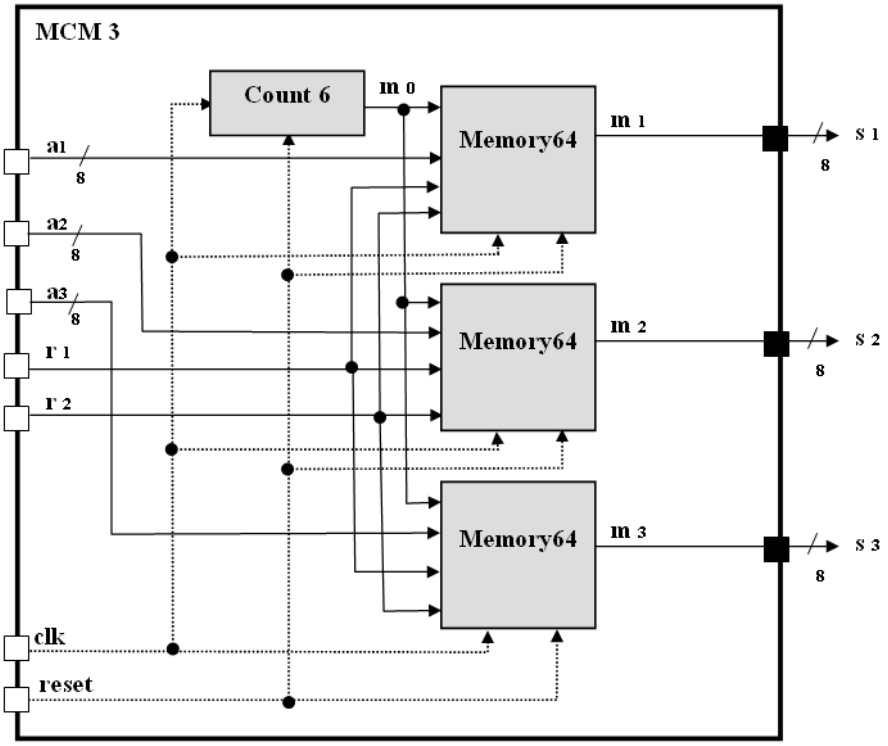


Figure (5) Structure of MCM 3 unit

- FLWT (Fast Lifting Wavelet Transform) unit which is the third stage in the system algorithm as demonstrated in section (3-C). The design of this unit is based on the optimal method for adder/subtractor. This unit is duplicated three times in the design of SYSTEM unit each one operating on one of the transformed color plane simultaneously after reading them from the MCM 3 unit.
- Control unit is designed for generating control pulses to achieve system synchronization.

The input to the SYSTEM unit is the original tile color image (8-bit for each three colors) and the output will be the four sub band for each color.

6. Image Compression System

Figure (6) illustrates the major data pathways of the implementation of the JPEG2000 Image Compression System. The personal computer (PC) runs software that reads the image, transmits it to the FPGA (one pixel at a time) to process the low speed part of the system, and receives the output data to execute the high speed part of the system by software to obtain the compressed image data (one byte at a time).

The transmission of pixels from the software to the FPGA, and of bytes from the FPGA to the software, is done one byte at a time using software-handshaking through the PCs interface (PCI). Implementation the compression system as hybrid design led to improve the performance with high speed and low cost.

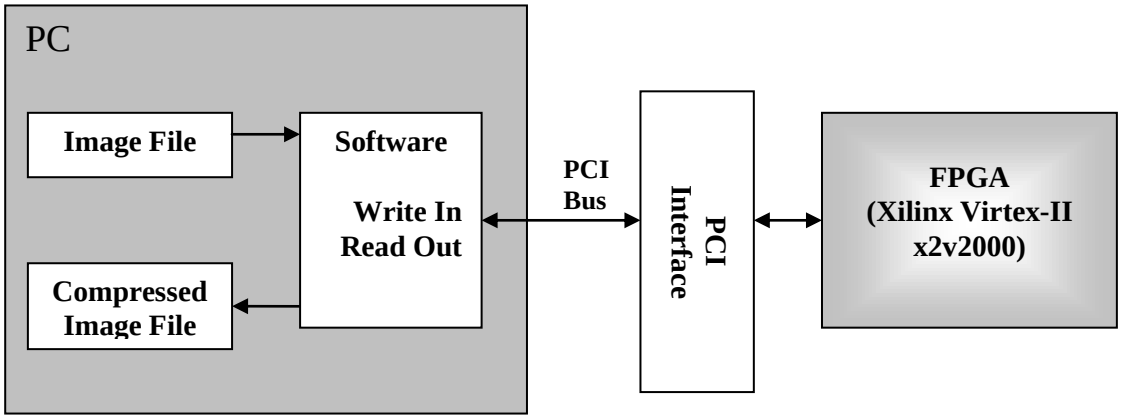


Figure (6) The flow of data among components

7. Tests and Results

The results of active information about the system of Low Speed Part proposed design and its general parts from map and asynchronous delay reports of Virtex-II x2v2000 target device is given in the **Table (1)**.

Table (1) The result of the system and its parts reports

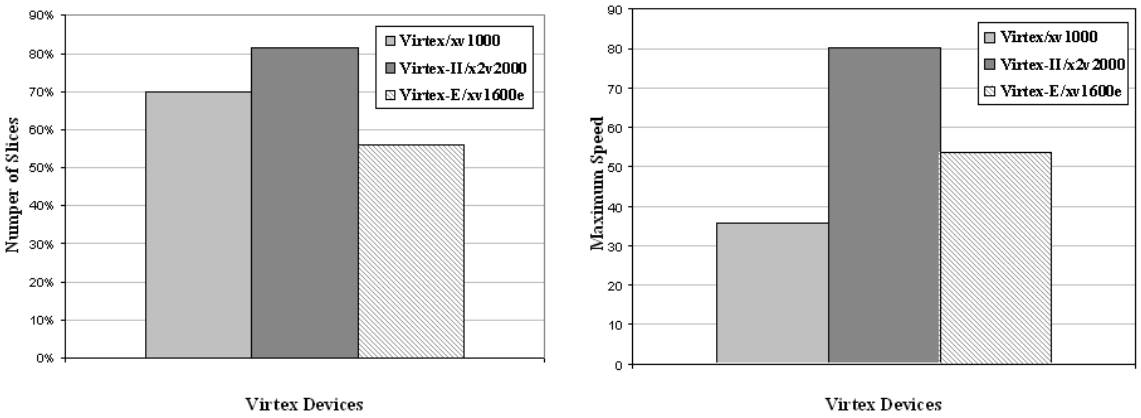
Program Name	Task	Space (CLB)	Run Speed (MHZ)
PRE.vhd	Preprocessing	3	404.728*
COLOR.vhd	Intercomponent Transform	45.5	182.548*
MCM3.vhd	Data Storage	434.5	91.979 *
FLWT.vhd	Intracomponent Transform	576.5	86.544 *
Control.vhd	Generate control signals	17.25	290.36 *
SYSTEM.vhd	Low Speed Part Design	2224.25	80.19 *

* Safety Factor (SF) is 1.2

As shown from the value of the space illustrates the number of Configurable Logic Block (CLB) and the run speed represents the reversed value of the maximum asynchronous time delay for the data multiplied by Safety Factor (SF) that ranged between 1.1 and 1.5 because the silicon chip is usually effected by Vcc., heat temperature and surrounding environment. The results in **Table (1)** showed that there is a high difference between each part of the system and the total system in space and maximum speed. The space and the maximum speed of the total system is less than that obtained by adding the value of each part of the system. These differences are due to the place and routing processes.

8. Performance Analysis of Different Virtex Devices for the Designed System

To evaluate performance of different type Virtex devices for the proposed system design, three types of devices were used in order to compare its performance (space and maximum speed) as shown in **Figs. (7a)** and **(7b)**.



(a) **(b)**

Figure (7) Comparison of performance between different virtex devices (a) comparison on space (N. of slices), (b) comparison on max speed

From **Fig.(7)**, the device Virtex-II of x2v2000 family was chosen because it performs well with the system design due to two important notes which can be summarized as follows:

i. This device has an efficient space for placing the designed system. It has a greater number of slices which has a percentage ratio 82% compared with the other as shown in **Fig.(7a)**.

ii. Accelerating the designed system as shown in **Fig.(7b)**. It has a maximum speed with SF 80.19 MHz which is higher compared with other devices.

9. Conclusions

The work in this project includes design and implementation the low speed part of the JPEG2000 Image Compression by using VHDL language based on field programmable gate array (FPGA). The design utilizes different techniques as pipelining, parallel execution, data reusability and specific features of Xilinx Virtex II FPGA series to achieve a performance that is it possible to give a higher than a pure software implementation.

It Introduces a micro-architectural design named as fast lifting wavelet transform for hardware acceleration of the Discrete Wavelet Transform based on the Lifting scheme and the design uses internal spatial storage unites instead of external memory, optimization adder/subtractor method to speedup the system and therefore leads to increasing the performance.

The designed system can be considered as a real time system due to its high speed, high accuracy and using a universal chip with maximum speed 80.19 MHz and cost 82%. The proposed design of implementation three stages (preprocessing, intercomponent transform and intracomponent transform) using FPGA has a maximum speed which is higher compared with other system designed of one stage (intracomponent transform) with a maximum speed 40 MHz [12] and 50 MHz [14].

10. References

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