# A MICROCONTROLLER BASED - 400 HERTZ FREQUENCY CONVERTER [+]

# المسيطر الدقيق المستند الى العاكس ذات التردد 400 HZ

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**المستخلص :**

**يتناول هذا البحث تصميم وتنفيذ مصدر عاكس للفولتية (VSI) وذلك للسيطرة على الفولتية بتردد ٤٠٠ هيرتز. يستخدم المسيطر الدقيق89c51 بواسطة تضمين عرض النبضة لتوليد نبضات مختلفة في دورات التشغيل عند تردد ٤٠٠ هيرتز، وتتغير الفولتية المسلطة على محرك حث بواسطة تضمين عرض النبضة بأستخدام مصدر عاكس للفولتية احادي الطور. يُبرمج المسيطر الدقيق لتوليد سلسلة من النبضات ذات دورات تشغيل مختلفة بتردد ثابت ٤٠٠ هيرتز حيث يكون مدى دورة التشغيل من ٠% الى ٦٠% وبدقة ٥% .**

**يستلم العاكس اشارة ال DC من المقوّم ويحوّلها الى قدرة AC لتغذية المحرك. وتستخدم (MOSFETs) كمفاتيح عاكس قدرة ويتم التحكم بها بواسطة النبضات التي يتم توليدها وحسابها بواسطة المسيطر الدقيق. يُمثل عاكس الفولتية بواسطة المحاكاة الحاسوبية بأستخدام برنامج اوركاد (Orcad 9.2) يطبق البرنامج عمليا بتنفيذ التصميم.**

## Abstract

**This research deals with constructing and implementing voltage source inverter to control voltage at any frequency. The microcontroller 89c51 is used by pulse width modulation (PWM) generating different pulses in the duty cycle at any frequency. The voltage applied to an induction motor is varied by using a single phase, 400 HZ, voltage source inverter. The microcontroller is programmed to generate a train of pulses with different duty cycles at constant frequency 400 HZ. The range of duty cycle is from 0% - 60% at 5% resolution.**

**The inverter receives the DC signal from the rectifier and converts it to AC power to feed the motor. MOSFETS are used as inverter power switches which are controlled by pulses calculated and generated by the microcontroller. Voltage inverter is represented by computer simulation applying orcad 9.2 program. The system is applied practically by implemting the design.**

## Introduction:

The converter control gating signals are originally generated by using analogue electronic hardware. To control the electronic switching of power inverters, PWM are widely used [1]. Many papers have been written on the PWM inverter and PWM strategies. In a previous work, Jameel (2003) designs and implements a three phase, 1000 Hz, voltage source inverter

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to satisfy the load requirements for missile control. The microcontroller 89c51 system is used to generate pulse-width modulation (PWM) voltage waveform for a three phase inverter [2]. In another previous work, Kareem (2004) presents a new speed control system in which a microcontroller for inverter control and the speed controller is designed by employing an IGBT-type power electronic switch. The range of inverter output frequency is from (350 to 400) Hz at 10 Hz frequency step [3]. On the other hand, Muhammad Hussein (2005) implements the design and construction of a voltage source inverter (VSI) system based on microcontroller (type 89c51). The inverter power switches are (MOSFET) controlled by pulses depending on sampled sinusoidal pulse width modulation (SPWM) technique with frequency ratio changing [4]. Senan M. Bashi (2005) investigates the performance of single-phase induction motor using microcontroller M68HC11E-9. The microcontroller senses the speed's feedback signal and consequently provides the pulse width variation signal that sets the gate voltage of the chopper, which in turn provides the required voltage for the desired speed [5]. In this work the device is used in medical applications to obtain high speed induction motor such as centrifugal device to separate solutions. So the frequency of the device must be higher than the supply frequency, i.e. 400Hz.

## System Simulation

The system is built with practical elements and tested with AC motor through controlling voltage source inverter with 200V DC. The proposed single-phase bridge inverter has four switches N-channel MOSFET, along with a digital clock to generate constant frequency as shown in figure (1)

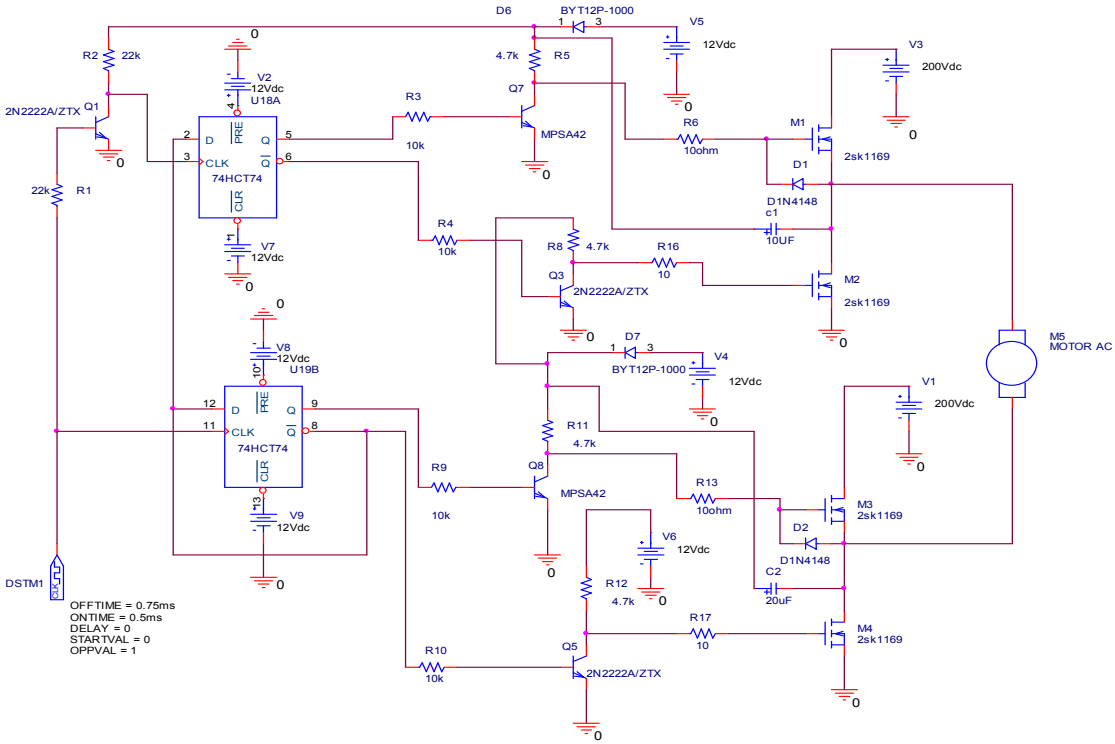



Fig. (1). The circuit diagram of quasi square operation.

## Controller Construction

As shown in figure (2), a 4-bit dip switch is used as a duty cycle selection switch. The duty cycle varies from 0% up to 60% at 5% resolution. The value of the desired duty cycle should be matched with a dip switch code as shown in table (1). Two push button unlatched switches (PB) are used. The output of the microcontroller is a train of pulses with desired duty cycle taken from P.3.4. These pulses are inverted by using TTL logic IC 74LSO4 and have been fed to the opto coupler 3N35.

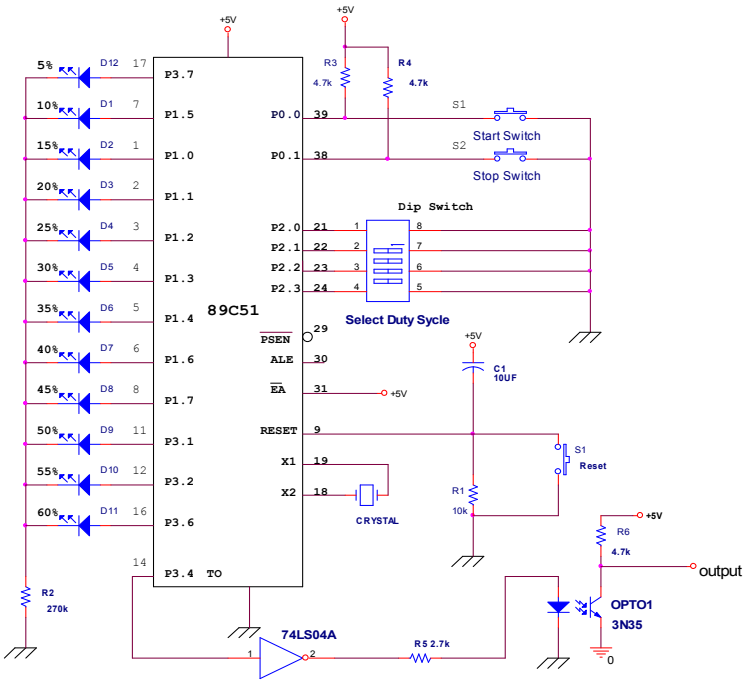



Table (1)

| Dip Switch Code | Duty Cycle |
|---|---|
| 0000 | 0% |
| 0001 | 5% |
| 0010 | 10% |
| 0011 | 15% |
| 0100 | 20% |
| 0101 | 25% |
| 0110 | 30% |
| 0111 | 35% |
| 1000 | 40% |
| 1001 | 45% |
| 1010 | 50% |
| 1011 | 55% |
| 1100 | 60% |

Fig. (2) Schematic diagram for PWM controller

## PWM Programming

Two internal interrupt signals are generated from two timers and this causes the program to jump to two interrupt service routines (ISR) to control the generation of PWM pulses. The value of the duty cycle determines generating of PWM signals. Timer 0 will control the uniform cycle time. Timer 1 will control the on time of PWM pulses. Figure (3) shows the sequences of interrupt signals.

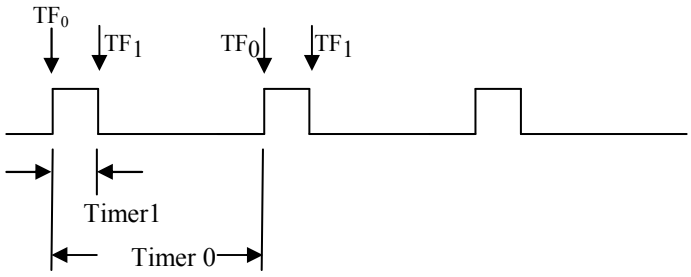



Fig. (3) Timing of interrupts.

The main program initializes the register bank, stack pointer, timer mode register, timers and enables the configuration of interrupt system. Moreover, it reads the status of start and stop push buttons. The flow chart of main program is shown in figure (4).

As shown in the flow chart, it is clear that the main program calls two subroutines. Read duty-cycle (READ DT-CYCL) and on time calculation (ON-TIME CALC). The first routine checks the desired duty cycle by reading the dip switch status and the second routine calculates the ON-TIME depending on the selected duty cycle

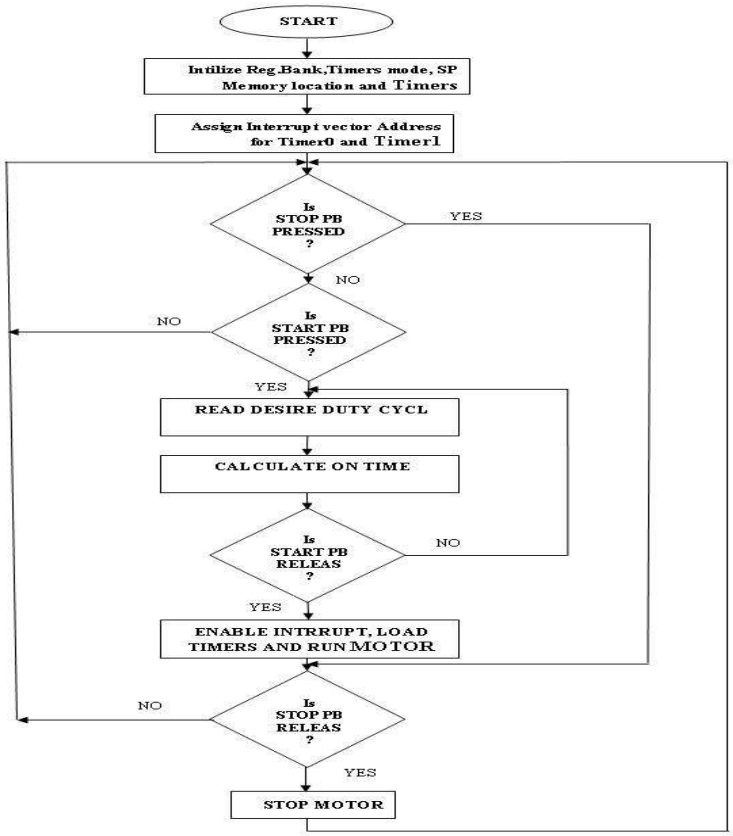



Fig. (4) Flow chart of main program.

## Interrupt Service Routine

Initially Timer 0 is loaded with time period of 2500 $\mu S$ , while Timer 1 is loaded with on time, which is calculated according to the selected duty cycle through the execution of the main program. When Timer 1 counts up to zero, internal interrupt signal, $TF_1$ will be high and causes the main program to jump and execute the interrupt service routine, $T_1$-ISR. The output of p3.4 will be low by this routine and disable Timer 1 interrupt, and turn it off, while Timer 0 is still counting up. When Timer 0 reaches zero, internal interrupt signal, $TF_0$ will be high and causes the main program to jump and execute T0-ISR. This routine will re-initialize the two timers, the output of p3.4 will be high, turn on two timers and enable both interrupts $T_0$ and $T_1$. The flow chart of the two interrupt service routines is shown in Figure (5)

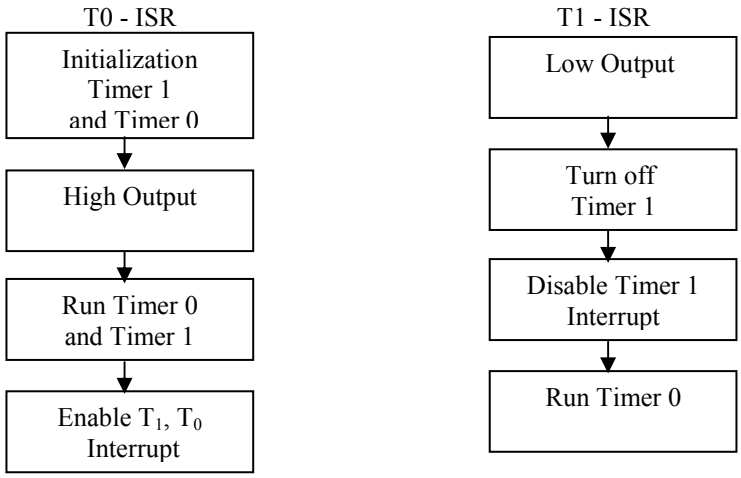



**Fig. (5)Flow chart of interrupts**

## Read Duty-Cycle

This routine continuously checks the status of a 4-bit dip switch to determine any variation in the desired duty cycle. Each of the 12 codes formed by 4-bit dip switch has a counterpart of a desired duty cycle as shown in table (1). The routine is based on lookup table technique, the duty cycle is stored in (ROM) whose starting address is assigned as duty cycle table (DCYCL_TABL), the range of duty cycle is from 0%-60% at 5% resolution. Initially, the routine is used to clear p1 and p3, and then loads the DATA POINTER register with the starting address of the DCYCL_TABL. The desired duty cycle is selected according to the switch code, the value of the code is added to the starting table address to get the desired duty cycle. For each selection of duty cycle, a proper LED is turned on. If the enter code is out of range, i.e. 13-15, an error is indicated by flashing all LEDs. The flow chart of the routine is shown in Figure (6).

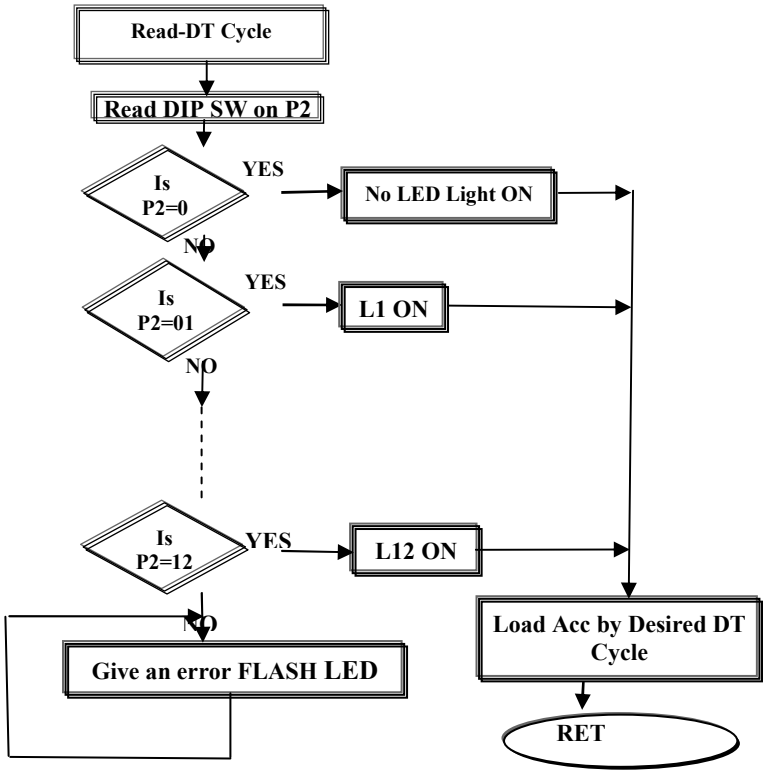



Fig. (6 ) Flow chart of the duty cycle selection.

## On Time Routine

The ON_TIME is calculated simply by:
ON_TIME = DUTY CYCLE * PERIOD / 100
So the routine has just to divide the period, which is constant, over 100 and then multiply the result of the division by the calculated duty cycle of the previous routine. This technique allows avoiding fixed arithmetic point. The negative value of the result has to be computed and loaded in Timer 1. The flow chart of this routine is shown in Figure (7).

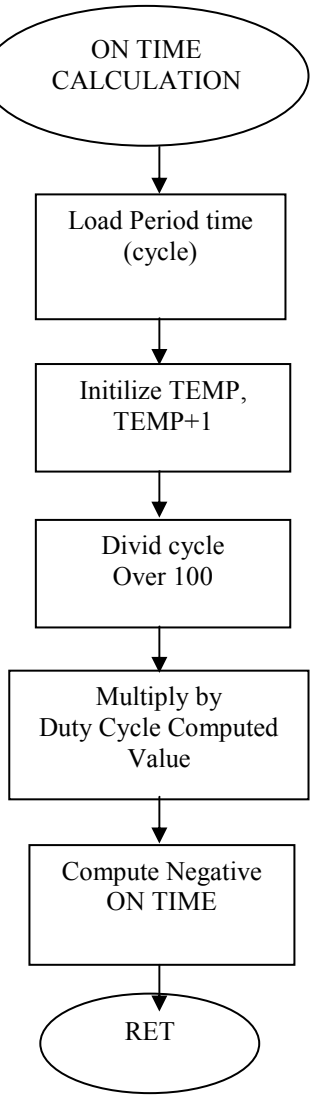



Fig.(7) Flow chart of ON Time calculation routine

## Power Stage and Gate Drives Circuit

The first step in designing the power stage is choosing the power semiconductor devices. The inverter consists of four main switches. A high speed power switching, 20A, 450V, MOSFET type 2SK1169 is chosen as the main switching device for the inverter. To avoid short circuit, each MOSFET is connected to a diode 70mA, 100V, DIN448 type,

between the gate and source, in addition to connecting a diode, 300V, 1.5A, BYT12P-1000 type, through each DC power supply 12V. The four MOSFETs are fitted on a suitable heat sink in order to dissipate the results of conduction losses.

The gate drivers obtain the signal pulses from M74HC74-CMOS D Flip-Flop and amplify them to the level required for switching the power MOSFET. All interconnections are made on a printed circuit board (PCB)

## Simulation Result

The simulation is done for different duty cycles at 5% resolution and the following parameters Vdc = 200V, AC motor, T= 2.5 msec. Figure (8) illustrates the measured digital clock output pulse at 60% duty cycle. Figure (9) illustrates the control signals for lower and upper MOSFET at 60% duty cycle. Figure (10) shows the output voltage at 60% duty cycle and the frequency spectrum of the output voltage is shown in figure (11).

## Practical Result

Cycle of output wave shown Selected practical results obtained for single-phase inverter are used to evaluate the performance of the proposed system. For this purpose, practical system consisting of a PWM-VSI drive and 0.36HP induction motor has been used. The results presented here for 60% duty cycle are obtained from tests carried out on a 220V, 400Hz squirrel cage induction motor. The practical results are depicted in the illustrated diagrams:

The waveforms obtained practically, as shown in Figures (12) to (16) are measured by using a universal scope meter and are transferred to computer software system by which the waveforms can be plotted. Figure (12) shows the measured microcontroller output waveform at 60% duty cycle. Figures (13) and (14) show the PWM pulses used to control the lower and upper MOSFET of power circuit via drive. Figure (15) shows the measured output voltage at 60% duty cycle. On comparing the figures (12) to (15) with simulated circuit output waveforms (8) to (11), coincidence between the waveforms of the practical and simulated waveforms can be noticed. Figure (16) shows the measured output current waveform for the motor. The current increases with increasing duty cycle which leads in turn to an increase in Vrms and a decrease in off period, gradually the wave approaches sine by filterization within motor coils.

Switching angles ($\alpha_1, \alpha_2, \alpha_3, \alpha_4$) for a complete cycle of output wave shown in figure (17) are calculated by calculating (a) time, i.e. (on time) at various values of duty cycles from 25% - 60%. Matlap – program is used to calculate the values which are listed in the table (2).

**Table (2) 4-switching angles per cycle**

| | 25% Duty cycle | 30% Duty cycle | 35% Duty cycle | 40% Duty cycle | 45% Duty cycle | 50% Duty cycle | 55% Duty cycle | 60% Duty cycle |
|---|---|---|---|---|---|---|---|---|
| $\alpha_1$ | 0.4688 | 0.4375 | 0.4063 | 0.3750 | 0.3438 | 0.3125 | 0.2813 | 0.2500 |
| $\alpha_2$ | 0.7813 | 0.8125 | 0.8438 | 0.8750 | 0.9063 | 0.9375 | 0.9688 | 1.0000 |
| $\alpha_3$ | 1.7188 | 1.6875 | 1.6563 | 1.6250 | 1.5938 | 1.5625 | 1.5313 | 1.5000 |
| $\alpha_4$ | 2.0313 | 2.0625 | 2.0938 | 2.1250 | 2.1563 | 2.1875 | 2.2188 | 2.2500 |

Table (3) and figure (18) show the variation of the amplitude of output voltage for the fundamental wave and harmonics with the change in the duty cycle. By increasing duty cycle, harmonics amplitude reduces according to the fundamental wave, hence ($e_{orms}$) value of the total voltage increases. The table (4) show that ($V_{orms}$) changes by controlling on time and increases by increasing duty cycle. Figure (19) shows the variation of $V_{orms}$ with the duty cycle. Figure (20) shows the variation of speed with duty cycle. Figure (21) shows AC drive system and microcontroller circuit printed card board. Finally figure (22) shows system stage of microcontroller based-400Hz frequency converter

**Table (3) the variation of the amplitude of output voltage for fundamental wave and harmonics with the change in the duty cycle for inductive load**

| | 25% Duty cycle | 30% Duty cycle | 35% Duty cycle | 40% Duty cycle | 45% Duty cycle | 50% Duty cycle | 55% Duty cycle | 60% Duty cycle |
|---|---|---|---|---|---|---|---|---|
| $e_{orms}$ | 95.3187 | 105.7326 | 115.2363 | 123.2766 | 130.8144 | 138.5355 | 145.8485 | 152.2730 |
| $1^{st}$ Harmonic (v) | 97.4495 | 115.6077 | 133.8679 | 149.6783 | 165.3806 | 180.0633 | 193.6358 | 206.0145 |
| $3^{rd}$ Harmonic (v) | 78.4213 | 83.8376 | 84.5240 | 80.7282 | 72.3743 | 60.0211 | 44.3511 | 26.2302 |
| $5^{th}$ Harmonic (v) | 47.0528 | 36.0127 | 18.5990 | 0.0000 | 19.4899 | 36.0127 | 47.0528 | 50.9296 |
| $7^{th}$ Harmonic (v) | 13.9214 | 5.6908 | 24.3216 | 34.5978 | 35.3731 | 25.7233 | 8.4923 | 11.2451 |
| $9^{th}$ Harmonic (v) | 10.8277 | 25.2103 | 27.2258 | 16.6309 | 2.2199 | 20.0070 | 28.2070 | 22.8905 |

**Table (4) $Vo_{rms}$ at different duty cycle**

| | 25% Duty cycle | 30% Duty cycle | 35% Duty cycle | 40% Duty cycle | 45% Duty cycle | 50% Duty cycle | 55% Duty cycle | 60% Duty cycle |
|---|---|---|---|---|---|---|---|---|
| $Vo_{rms}$ | 100 | 109.54 | 118.32 | 126.5 | 137.84 | 141.42 | 148.32 | 154.92 |

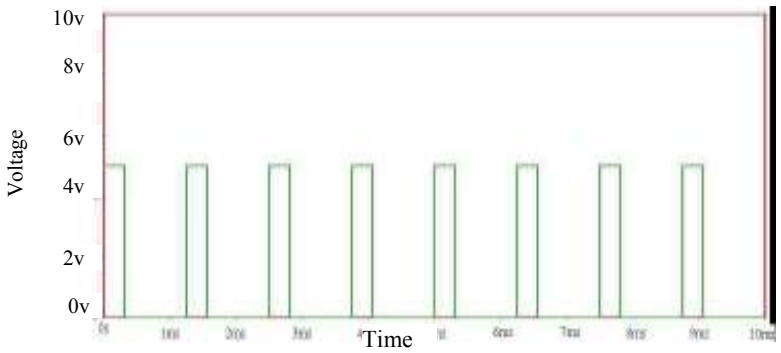
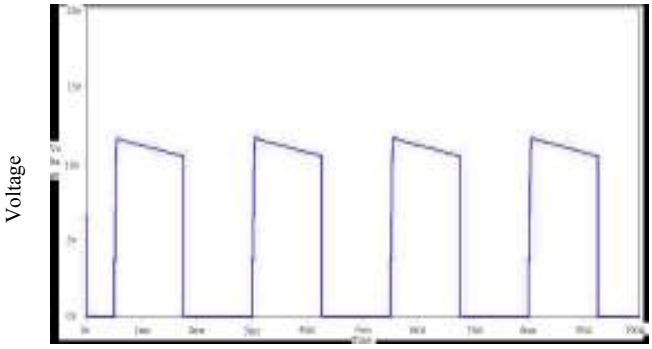
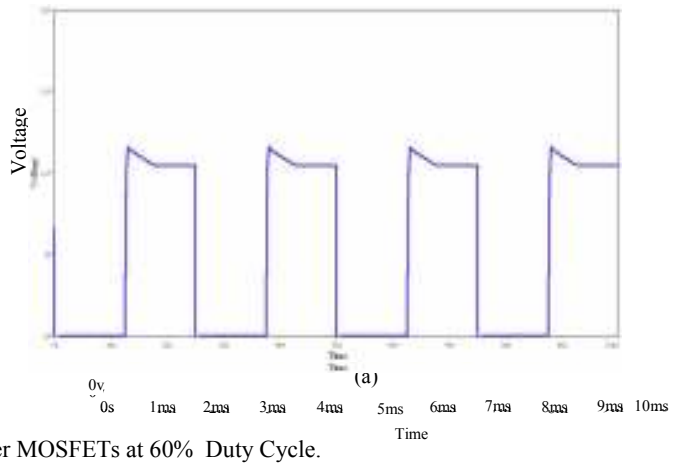



Fig. (8) The measured digital clock output pulse at 60% duty cycle.




(b)




(a)

Fig.(9) The control signal for lower and upper MOSFETs at 60% Duty Cycle.
(a) Control Signal for the lower MOSFT.
(b) Control Signal for the upper MOSFT.

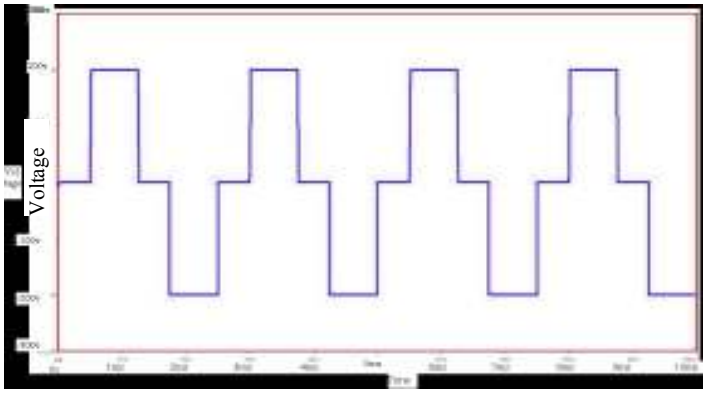



Fig. (10) Output voltage waveform at 60% Duty Cycle

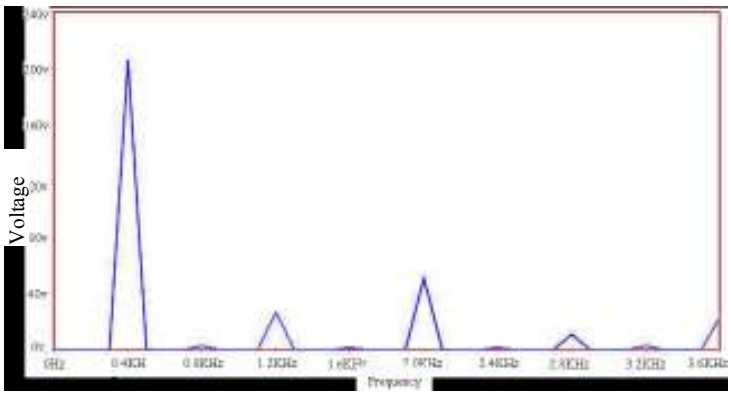



Fig. (11) Frequency spectrum of the output voltage waveform at 60% Duty Cycle

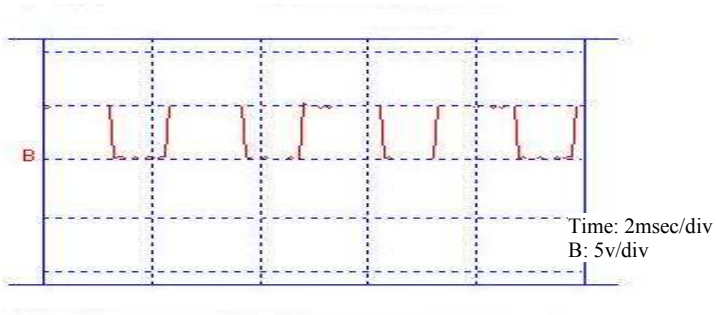



Fig.(12)The measured microcontroller output pulse at 60% Duty Cycle.

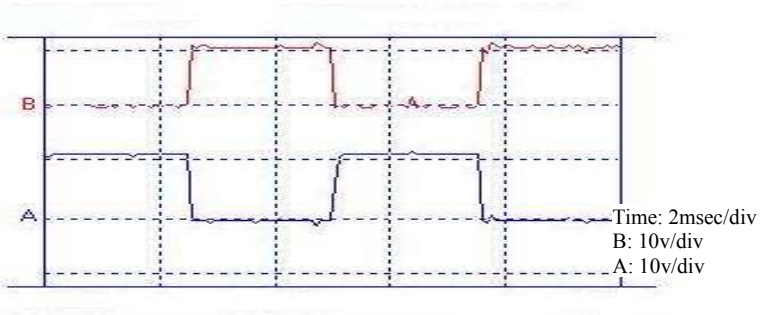



Fig. (13) Control PWM signal for the lower MOSFET at 60% Duty Cycle.

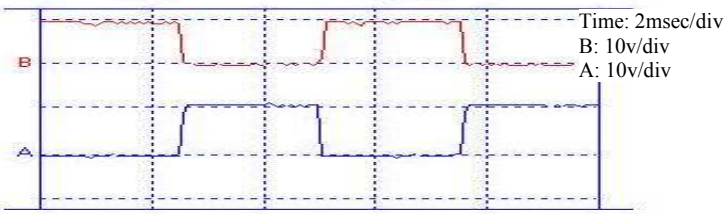



Fig. (14)Control PWM signal for the upper MOSFET at 60% Duty Cycle.

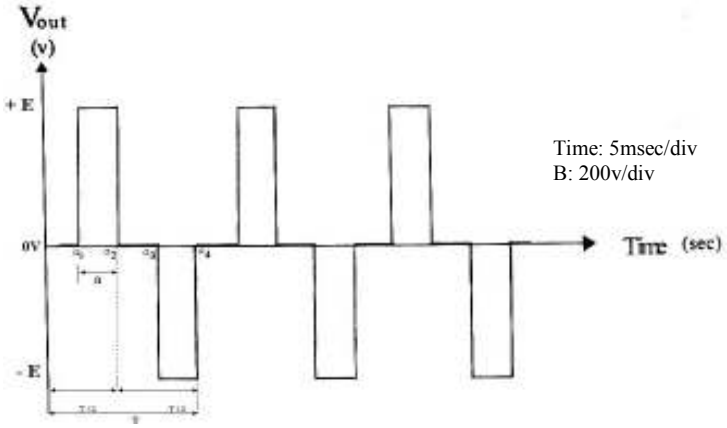



Fig.(15)The measured output voltage waveform of inverter at 60% Duty Cycle.

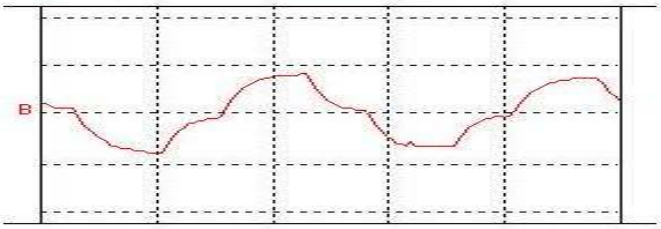



Fig. (16)The measured output current waveform to the motor at 60% Duty Cycle.

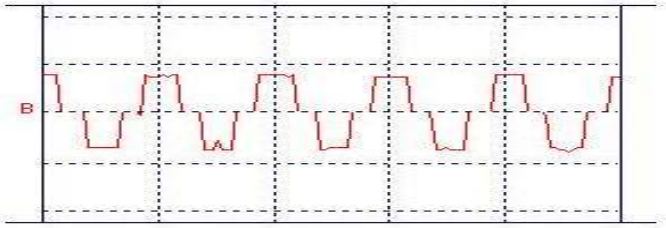



Fig. (17) Output voltage waveform of inverter

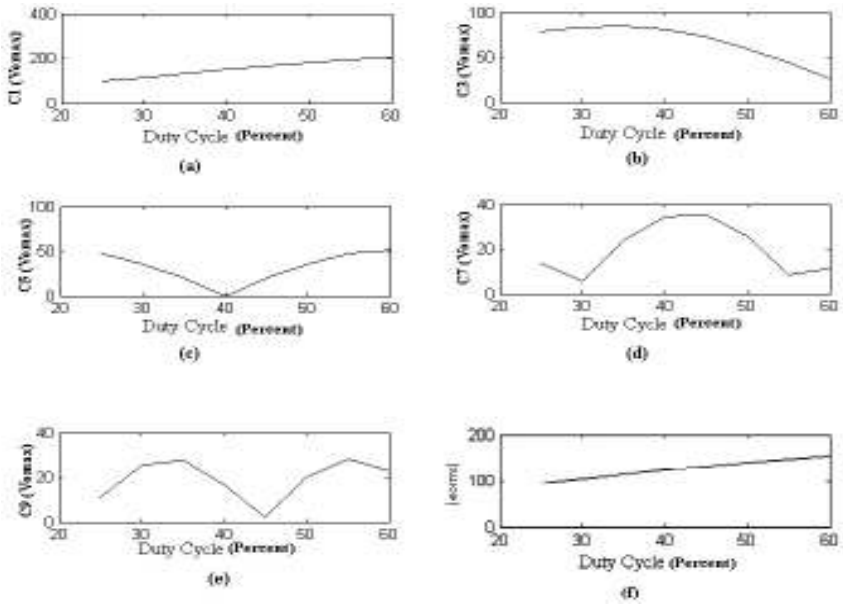



Fig. (18) Shows the variation of the amplitude of output voltage for fundamental wave and harmonics with the change in the duty cycle.

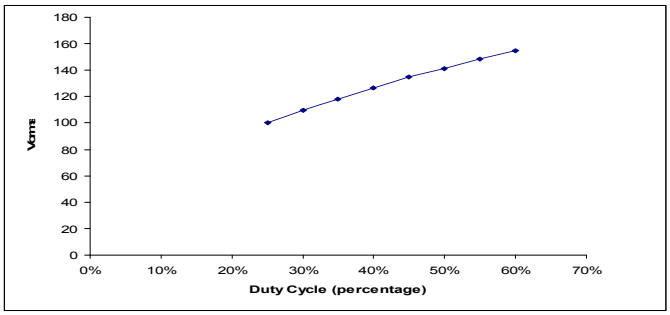



Fig. (19) Relationship between Vorms and Duty Cycle.

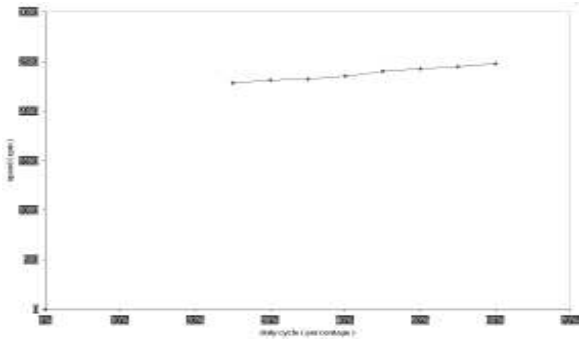


Fig. (20) Relationship between speed and Duty Cycle.

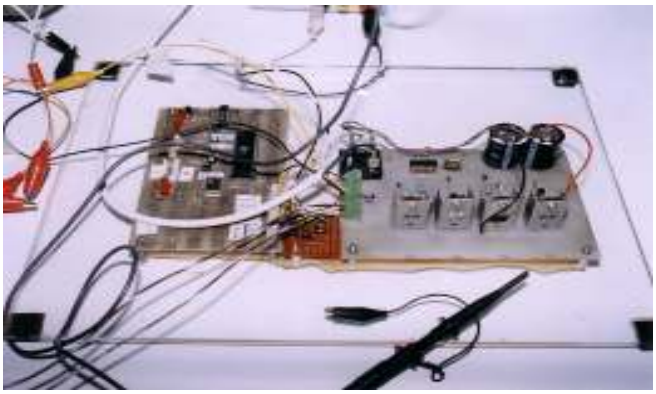


Fig. (21) AC drive and microcontroller circuit printed card board.

Fig. (22) System stage of the microcontroller based-400Hz frequency converter.

## Conclusions:

From the work carried out concise conclusions have been reached regarding the use of single-phase control voltage source inverter. a microcontroller 89c51 has been used to generate a train of pulses with different cycles at 400 Hz frequency. The duty cycle can be varied from 0% up to 60% at 5% resolution. Two timers and two interrupt service routines (ISR) are used to control the generation of PWM pulses. Each of the 12-codes formed by 4-bit dip switch has a counter part of a desired duty cycle. The routine is based on lookup table technique. Flexibility is achieved by software implementation. The advantage of high switching speed improves the PWM pattern by minimizing the voltage and current harmonics. A gate drive with fast response and low power loss has been designed.

**References:**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