BICMOS RF CIRCUIT DESIGN LNA[+]

Odai A. Wadea [*]

Abstract:

This paper is concerned with the optimal design and simulation of Low Noise Amplifier for mobile communications operating at 1.5 GHz, 1.5 V and 0.25 μm channel length. The minimization of noise figure and required chip area for fabrication are the most important parameters to be investigated, therefore the optimization technique applied in this paper is to obtain the optimum structure parameters design values and to provide the minimum noise factor together. A modified new structure is used to minimize the chip area that is required for the fabrication of the amplifier on single chip. Electronic workbench (EWB) is used to simulate the designed structures to obtain the best results in such simulation.

المستخلص:

هذا البحث يقدم تصميم وتمثيل لدائرة مكبر اشارة قليل الضوضاء للاستخدام في دوائر الاتصالات الخلوية التي تعمل ضمن تردد 1.5 GHz ، 1.5 v . تقليل الضوضاء والحجم المطلوب للتصميم هي اهم العوامل الواجب تحقيقها للحصول على افضل دائرة مكبر اشارة لذلك فان التقنيات الموضحة في هذا البحث تعطي افضل النتائج لتحقيق هذا الهدف من حيث قيمة الضوضاء وحجم الدائرة. لغرض تمثيل الدائرة تم استخدام برنامج Electronic Work Bench والحصول على النتائج والمخططات من هذا النظام .

Keywords:

Very Large Scale Integration (VLSI), Radio Frequency Integrated Circuit (RFIC), Complementary Metal Oxide Semiconductor (CMOS), Surface Mount Device (SMD), and Signal to Noise Ratio (SNR), Low Noise Amplifier (LNA) .

Symbols:

γ : coefficient of channel thermal noise , δ:Coefficient of gate noise, $\mu_{ef.f:}$ is the field electron mobility ,ε_{sat}: velocity saturation field strength , B: Frequency band width , C: Correlation coefficient , $C_{a,max}$: Maximum capacitance available from the array , C_{gs}: Gate – source capacitance , C_{ox}: Oxide capacitance , C_p: Parasitic drain capacitance , $C_{v,min}$: Minimum varacter capacitance , F : Noise factor , G_a: Power gain, g_{do}: Zero bias drain conductance , $g_{g:}$: Shunt conductance , g_m: device transconductance , G_m: Transconductance , I: DC current , i^2_g: Shunt noise current , $i^2_{g,c}$: The portion of the total gate that is correlated with the drain noise , $i^2_{g,u}$: The

---

[+] Received on 17/4/2008, Accepted on 10/8/2009

[*] Assist Teacher/ Technical College/ Baghdad

portion that is uncorrelated with the drain noise , I_d: Drain current , i_d^2: Channel noise , i_n^2: Main square values of shot noise, K: Boltzman's constant , L: Channel length, L_g: Gate inductance , L_S: Source inductance , n: no. of gate fingers used to lay out the device. NF : Noise figure , P_D: Power dissipation , $P_{no,i}$: Available noise power at the output due to internal noise source, P_O: Is constant determined solely by physical technological parameters (v_{sat} and ε_{sat}), q: Electron charge , Q_{in}: is the effective Q of the amplifier input circuit, R_g: Gate resistance, r_g: Constant resistive term , R_s: Source resistance , R_{sh} : Shunt resistance , $S_{\delta rc}$: Output noise power , $S_{o,\delta rc}$: Output noise power due to the source , $S_{o,Rl,Rg}$: Output noise power due to R_l and R_g, T: Temperature in Kelvin , V_{DD}: DC voltage , V_g^2: White noise source , V_{gs}: Gate – source voltage , V_{sat} : saturation velocity, V_T: Threshold voltage , W: Channel width , Z_{in}: Input impedance , ΔF: Band width frequency

Introduction:

The ever increasing demand of low cost wireless transceivers has created the interest of integrating the whole radio frequency (RF) front end and baseband circuits in a single chip. At the same time, CMOS technologies, with the continuous scaling down of their feature size, have become a cost – effective competitor in RF integrated circuit (RFIC) design at the low to medium of GHz frequency band. The huge VLSI mass market makes CMOS even more attractive for RFIC applications to reduce the chip area as long as the single chip solution is considered. As the first active stage of a RF receiver, the LNA should meet at one time several specifications. It must provide enough gain to suppress the noise of subsequent stages and introduce as little noise as possible. Besides, linearity is always required all through the module; and input matching is particularly important, if a filter proceeds [1].The telecommunications industry today is undergoing changes. The major industry trends, particularly in cellular telephone, are equipment designed for higher operating frequencies and the use of miniature surface mount devices (SMD). The trends of miniaturization and the utilization of higher operating frequencies dictate the introduction of modifications to the physical and electrical characteristics of the individual components used in circuit's [2].The growing market of mobile wireless communications has increased the demand for low cost RF low noise amplifiers (LNA). The noise performance of these amplifiers must be low and the linearity requirements are severe in order to meet the dynamic range specifications. On the other hand, the power consumption must be as low as possible to save batteries.

Optimal Design of LNA:

In low noise amplifier design, determination of the minimum noise factor is a common and well-understood procedure. Typically, a small signal model of the amplifier is assumed a priori, an expression for NF is formed, and differentiation leads to the unique conditions for optimized noise performance. Noise factor (NF) is defined as [3]:

$$\mathrm{NF} = \frac{\text{total output noise}}{\text{total output noise due to the source}}$$
(1)

The transconductance of the input stage is given by [1] :

$$\mathrm{G_m} = \frac{\mathrm{w_T}}{\mathrm{w_o.R_S.(1+\frac{w_T.L_S}{R_S})}} = \frac{\mathrm{w_T}}{\mathrm{2w_o.R_S}} \qquad (2)$$

Where $\mathrm{R_S = W_T \,.\, L_S}$

Output noise power density due to the 50 Ωinput resistances is given by [1]:

$$\mathrm{S_{o,\delta rc}\,(w_o) = S_{orc}(w_o).G^2_{m,eff}} = \frac{\mathrm{4.K.T.w_T^2}}{\mathrm{w_o^2.R_S.(1+\frac{w_T.L_S}{R_S})^2}} \qquad (3)$$

Similarly, output noise power density due to the parasitic resistance and gate resistance is given by [1] :

$$\mathrm{S_{o,\,Rl,\,Rg}\,(w_o)} = \frac{4.K.T.(R_l + R_g)w_T^2}{w_o^2 R_S^2.(1+\frac{w_T^2.L_S}{R_S})^2} \qquad (4)$$

The channel current noise of the CMOS transistor is given by [1] :

$$\mathrm{S_{o,\,id}\,(w_o)} = \frac{\frac{\overline{\mathrm{i_d^2}}}{\Delta \mathrm{f}}}{\left(1+\frac{\mathrm{w_T.L_S}}{\mathrm{R_S}}\right)^2} = \frac{\mathrm{4.\,K\,.\,T\,.\,\gamma\,.\,g_{do}}}{\left(1+\frac{\mathrm{w_T.L_S}}{\mathrm{R_S}}\right)^2} \qquad (5)$$

By substituting (3),(4) and (5) in (1) we get the expression of noise factor:

$$\mathrm{NF} = 1+\frac{R_l}{R_S}+\frac{R_g}{R_S}+\gamma.g_{do}.R_S.\left(\frac{w_o}{w_T}\right)^2 \qquad (6)$$

A / To find optimum power density, we fix the value of the transconductance, $\mathrm{G_m}$; assign a constant value to ρ is:

$$\mathrm{G_m} = \frac{3\,\upsilon_{\mathrm{sat}}}{2\,\mathrm{w_o R_s L}}\frac{\rho(1+\frac{\rho}{2})}{(1+\rho)^2} \qquad (7)$$

Where $\rho = \frac{V_{od}}{L\varepsilon_{sat}}$

Once ρ is determined, we can minimize the NF by taking:

$$\frac{\partial N\mathrm{F}}{\partial\,\mathrm{P_D}} = 0 \qquad (8)$$

Which, after some algebraic manipulations, result is

$$P_{D,opt} = P_o \frac{\rho^2}{1+\rho}\left[\frac{1}{\sqrt{1+\frac{5\gamma}{\delta\alpha^2}}}\right] \qquad (9)$$

B / a second method of optimization, fixes the power dissipation and adjusts ρ to find the minimum noise factor. The expression (6) is minimized for a fixed P_D when

$$\frac{\partial N\mathrm{F}}{\partial \rho} = 0 \qquad (10)$$

$$\rho_{opt}^2 = \frac{V_{dd} W . C_{ox} v_s V_{od}^2\, 2 w_O R_S}{(V_{od} + L\varepsilon_s)3. V_{dd} . v_s \varepsilon_s} |C| \sqrt{\frac{5\gamma}{\delta}} \left[1 + \sqrt{1 + \frac{3}{|C|^2}\left(1 + \frac{\delta}{5\gamma}\right)}\right] \qquad (11)$$

By using (9) and (11) and long channel CMOS transistor with some algebra and summing all factors we get total minimum noise factor[1].

$$F_{\min Gm,\rho} = 1 + 1.35675\left(\frac{w_o}{W_T}\right) \qquad (12)$$

The value of 1.35675 is only valid for long channel devices; **where $\gamma = 0.7$, $\delta = 4/3$, $\alpha = 1$, $C_{ox} = 10^{-3}$, $R_s = 50$ and L= 0.25 μm [1]** ; it may be three or four times larger in the presence of high electric fields. There is another parameter that must be found to get on minimum chip area as possible, to find the minimum channel width we use the relations and with some algebra we find the minimum width as:

$$W_{opt} = \frac{3}{2 w_O R_S \left(\sqrt{1 + \frac{5\gamma}{\delta\alpha^2}}\right) C_{ox} . L} \qquad (13)$$

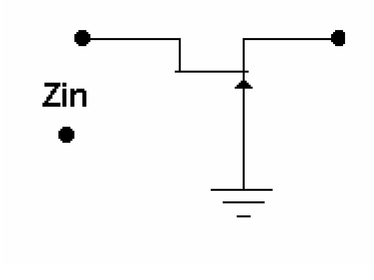
For long channel W_{opt} = 67 μm, this value is equal approximately to the width of firs technique, but the difference is the first one is not practical case while the second is practical.

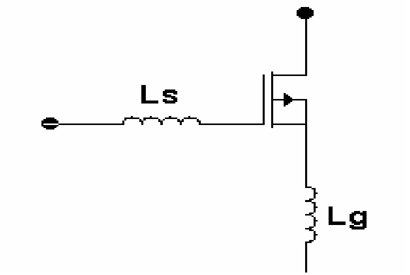
Fully integrated LNA design:

In the design of LNA there are several common goals [4], Including minimizing the noise figure of the amplifier, providing gain with sufficient linearity and providing a stable 50 Ω input impedance to terminate an unknown length of transmission line, which delivers signal from the antenna to the amplifier.

1 Input matching:

A good input match is even more critical when a preselect filter proceeds the LNA, because such filters are often sensitive to the quality of their terminating impedance. With these goals in mind we will first focus on the requirement of providing stable input impedance. To present known resistive impedance to the external word, a number of circuit topologies as shown in fig (1) [5].





(a) (b)

Fig (1) Types of input matching

The noise figure of fig (1-a) would be high for high frequencies due to the gate current noise of the transistor. The chip area of transistor = W.L, Where, W= width channel device and L= length channel device.

The second architecture employs inductive source or emitter degeneration as shown in fig (1-b) to generate a real term in the input impedance, with such an inductive, a real term in the input impedance can be generated without the need of real resistance, which degrades the noise performance.

1.1 Inductive source degeneration:

This architecture generates a real term in the input impedance, tuning of the amplifier input becomes necessary making this a narrow band approach. The proliferation of this architecture is not accident; it offers the possibility of achieving the best noise performance of any architecture. For an inductive degenerated LNA, the input impedance is given by [6]:

$$Z_{in} = S\left(L_S + L_g\right) + \frac{1}{SC_{gs}} + W_T L_S \tag{14}$$

Input matching requires that at the resonance frequency of the circuit, the impedance of the input stage is purely real and should be equal to 50Ω. It follows that:

Real part:

$$\mathrm{W_T.L_S = Z_{in} = 50\ \Omega \qquad \therefore\ L_S = \frac{50}{W_T}} \tag{15}$$

A simple Matlab program is written to evaluate the value of L_S, where is calculated to be equal, $L_S = 2.0833 \times 10^{-10}$ Henry, where $W_T =$ 2.4000e+011

Imaginary part = 0 (because of resonance):

$$\mathrm{W_O\left(L_S + L_g\right) = \frac{1}{W_O C_{gS}}}$$

$$\mathrm{\therefore L_g = \frac{1}{W_O^2 . C_{gS}} - L_S = 9.8924 \times 10^{-9}\ H} \tag{16}$$

From (16) we see that L_g depends on the magnitude of L_s to provide the matching. The magnitude of L_s and L_g limit the area of the circuit as clear below.
The chip area required to fabricate inductors can be founde using [7]:

$$A = \frac{L_x . l}{\mu . n^2} \tag{17}$$

$$L_x = \frac{d^2 n^2}{1 + 0.45d}$$

Where, L_x= inductance (Henry), l = length of inductor (meter), $\mu = 4\pi \times 10^{-7}$, n= number of turns, A = inductor chip area and d= coil diameter [8].

$A_{Ls} = 1.38 \quad 10^{-7}$ m^2 , $A_{Lg} = 7.7874 \times 10^{-5}$ m^2

The Chip area required to fabricate MOS transistor = (W×L) (18)

Where, W= transistor width (meter) and L= transistor channel length (meter)

So the total chip area = $A_{transistor} + A_{Ls} + A_{Lg}$

For width equal 67μm and length equal 0.25μm and with some algebra

$A_{transistor} = 1.67 \times 10^{-9}$ m^2

$A_{total} = 78 \times 10^{-6}$ m^2

To find the value of input impedance of the circuit, we use the Y- parameter. The input impedance is shown as below

$$Z_i = \frac{1}{Y_i - \frac{Y_r . Y_F . Z_L}{1 + Y_O . Z_L}} \tag{19}$$

Where. Z_L = load impedance (50Ω), and the required input impedance is (Z_{in}=7.5516 – j12.6215) Ω , A simple L impedance transformation network is used to transform the 50 Ω into this value. The final input impedance circuit is shown in fig (2)

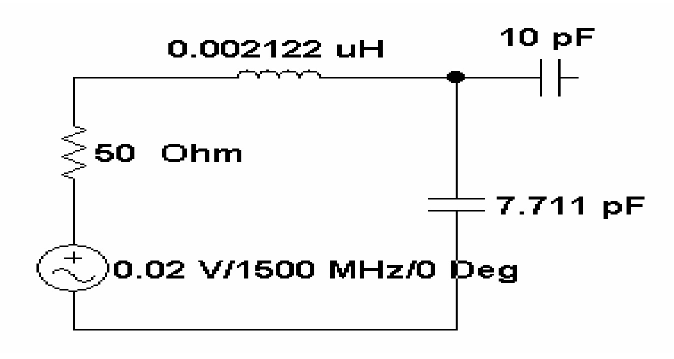


Fig (2) the input matching network

The required output impedance is

$$Z_O = \frac{1}{Y_O - \frac{Y_r . Y_F . Z_S}{1 + Y_i . Z_S}} \tag{20}$$

Where Z_S = source impedance (50Ω). A simple Mat lab program is written to evaluate the vale of Z_o, So (Z_o=10.2323 – j12.5813). The final output impedance circuit is shown in fig (3)

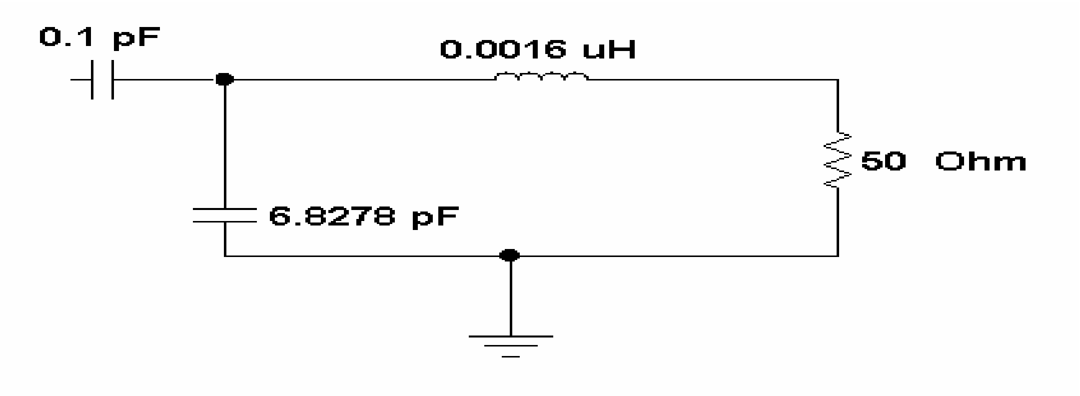


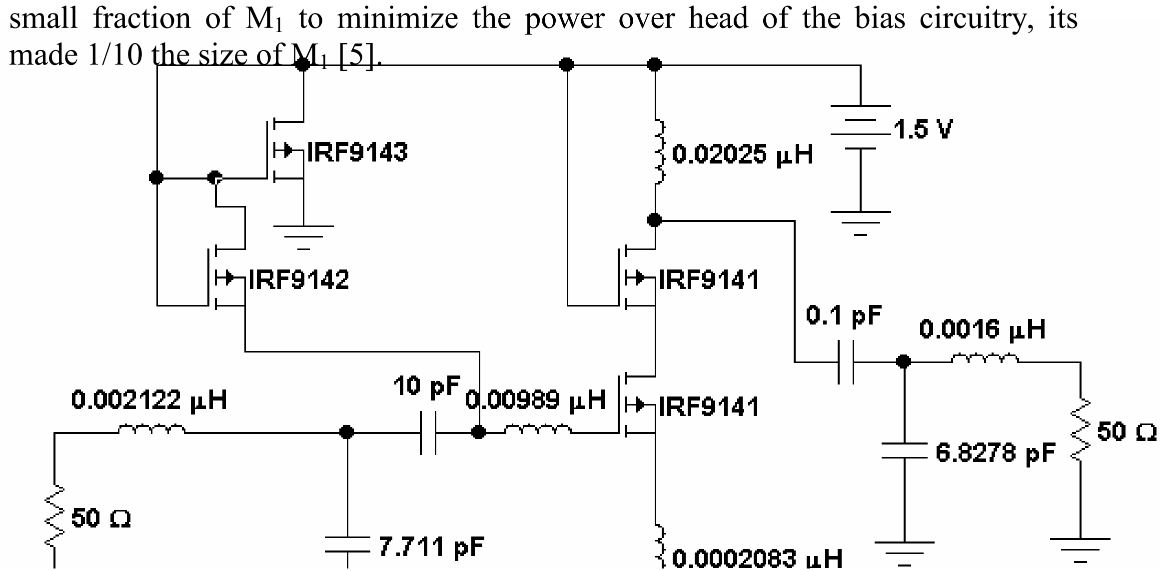
Fig (3) the output matching network

The simulation design's shown in figure (4) a 10pf DC blocking capacitor is chosen in input, since it is in series with the gate to source capacitance, it doesn't effect the overall input capacitor, The inductively source degenerated cascode structure is chosen for its superior noise and reverse isolation, The cascoding transistor is chosen to have the same width as the main device. This choice is somewhat arbitrary and thus not necessarily ideal.

Two considerations have constrained the size of the cascading transistor:

1- The gate – drain capacitance can reduce the impedance looking into the gate and the drain of M_2 considerably.
2- Degrading both the noise performance and input match.

A current mirror circuit provides a constant current, which, is obtained from an output current which, is reflection or mirror of a constant current developed on one side of the circuit. Transistor M_1 forms a current mirror with M_2, and its width is a small fraction of M_1 to minimize the power over head of the bias circuitry, its made 1/10 the size of M_1 [5].



M2

M1

Fig (4) final circuit

A 0.1 pf DC blocking capacitor is chosen in output and its value make noise in minimum value. As shown in figure (5) the noise figure (NF) reaches its minimum value of 0.01062 dB at the frequency of 1.5 GHz ,from the simulation circuit we found the Gain of the LNA reaches its maximum value of 126 db at frequency of 1.5 GHz. So the design can also provide a reasonable gain at the resonance frequency.

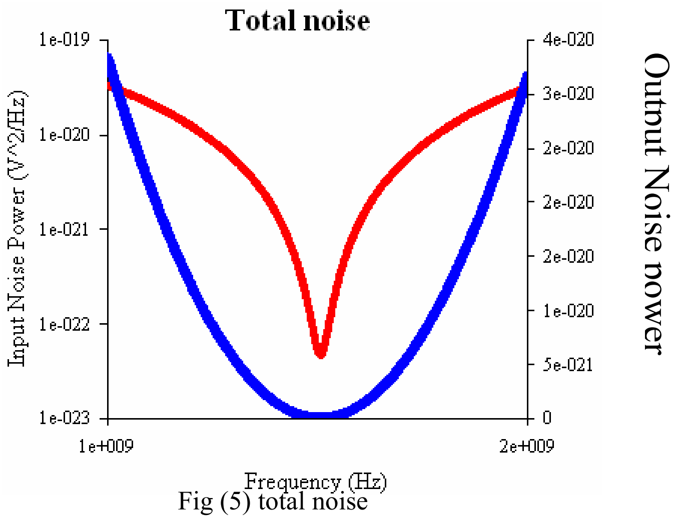


Fig (5) total noise

1.2 Common gate design:

The previous circuit used inductive source input matching, but there is another topology called common gate for common gate matching as shown in fig (6). The input impedance is given by [9]:

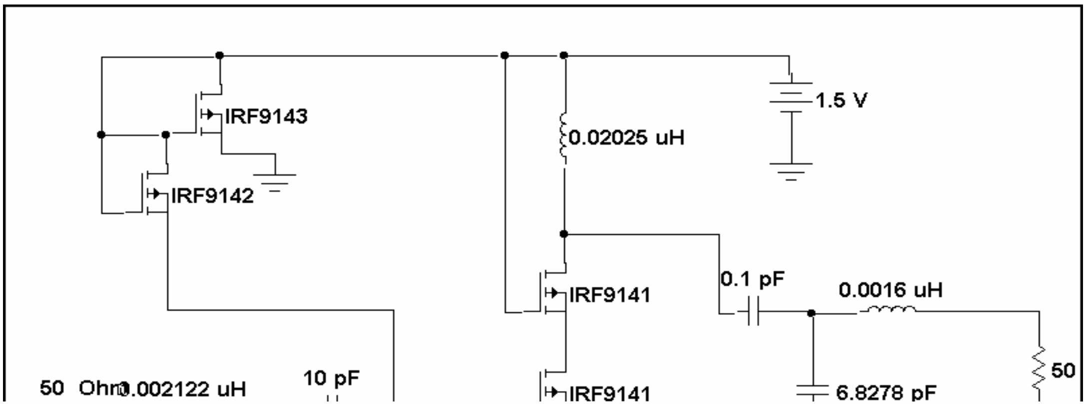


Fig (6) LNA with common gate input matching

Total chip area $A_T = W_1.L_1 + W_2.L_2$ + area of all inductors. The gain of this circuit is large and the noise is large too, we can reduce the noise of common gate circuit by using voltage series feedback. As shown in fig (7) the noise figure (NF) reaches its minimum value. Table (1) presents a comparison between inductor matching technique and common gate one. It can be shown from table that the noise figure increases when using common gate matching, however a significant saving in chip area is obtained.

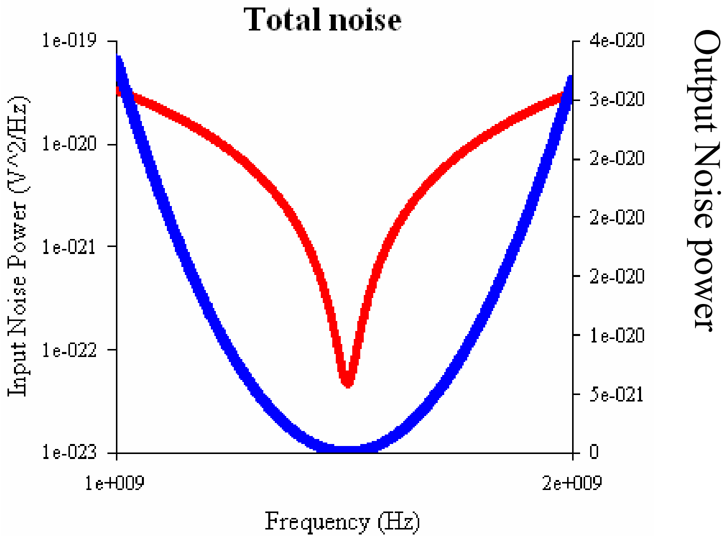


Fig (7) Total noise

Table (1) Comparison between inductors matching and common gate matching CMOS transistor

Inductors matching	Common gate matching
Low noise figure (NF = 0.01062 db)	High noise figure (NF = 0.25 db)

Large chip area A_{Ls} = 1.3816 e-7 m^2 A_{Lg} = 7.7874 e-5 m^2 $A_{trasistor}$ = 1.67185 e-17 m^2 A_{Ld} = 4.6616e-005 m^2 A_{total} = 125 µm^2	Small chip area A_{Ls} = 1.3816 e-7 m^2 A_{trans} = 1.67185 e-17 m^2 A_{Ld} = 4.6616e-005 m^2 A_{total} = 46 µm^2
Gain A_v = 126 dB	Gain A_v = 190 dB
Power dissipation 1.2 mW	Power dissipation 1.2 mW
Phase noise = 36.8 dB	Phase noise = 36.8 dB

Bi CMOS design :

1. inductive source degeneration:

we can use bipolar transistor instead of CMOS transistor in cascode and current mirror connection because bipolar transistor achieve high gain and the noise change will be a very small value so we ignore this change. Fig (8) shows the final circuit diagram of this case, while fig (9) shows the resultant noise figure with frequency.

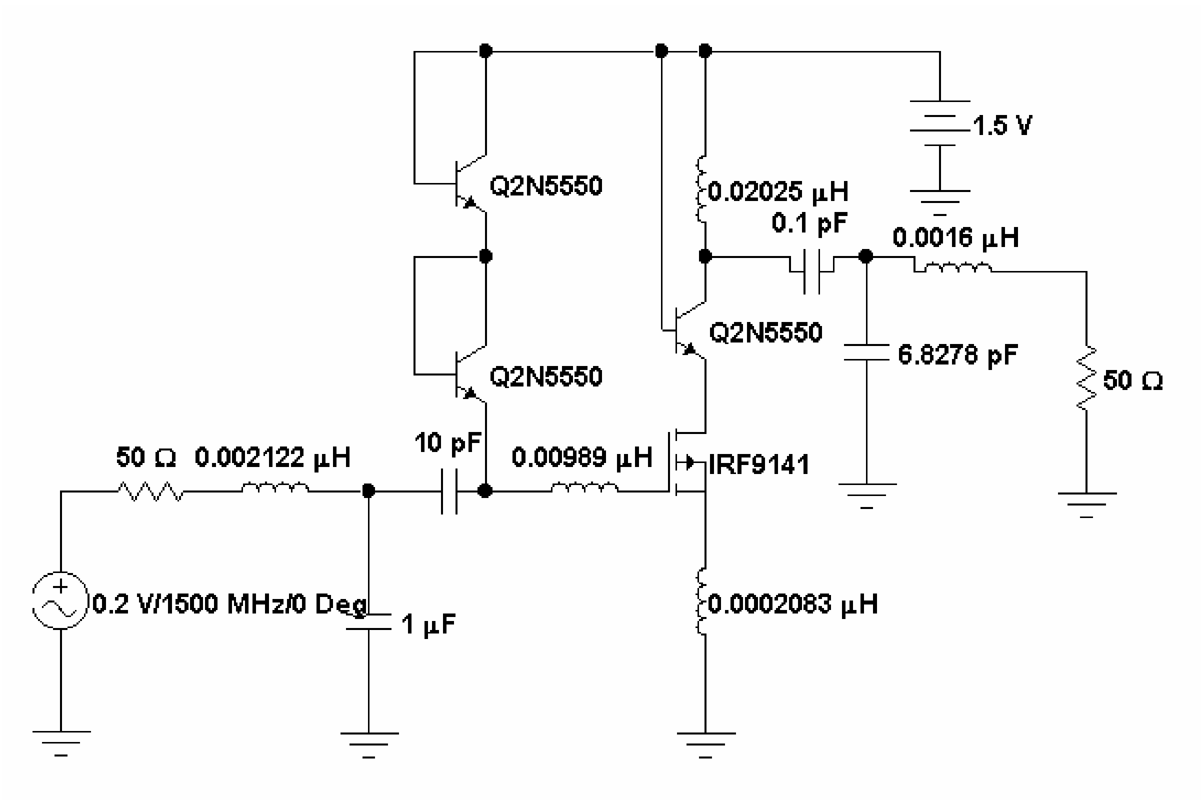


Fig (8)
LNA final circuit

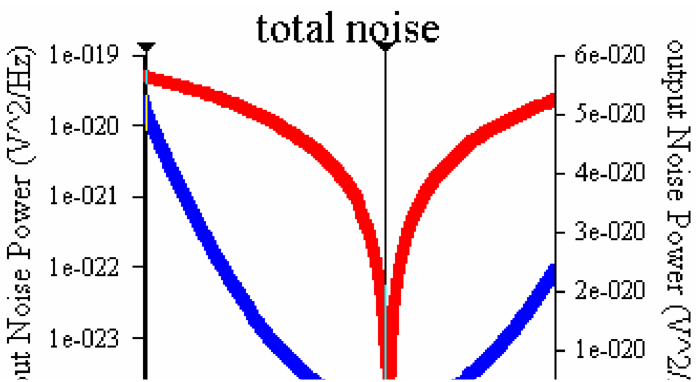


Fig (9) total noise

2. common gate design :

Fig (10) is illustrating of circuit design of this case. The resultant obtained for this case is shown in fig (11) for the noise frequency relations.

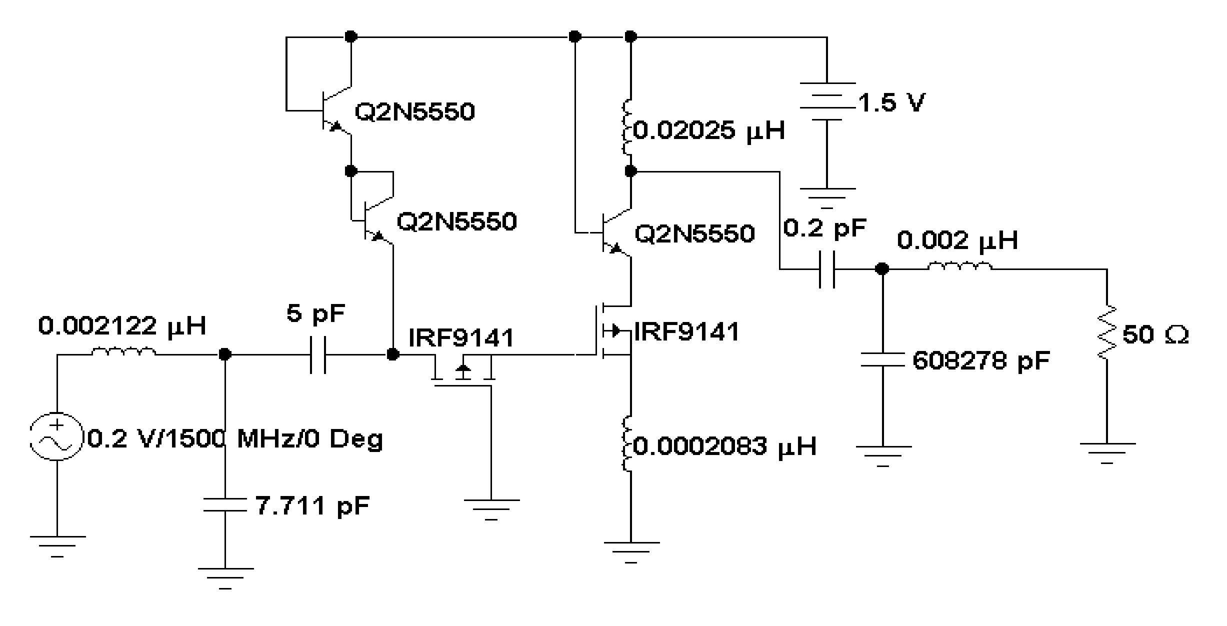


Fig (10) Common gate Bi CMOS circuit

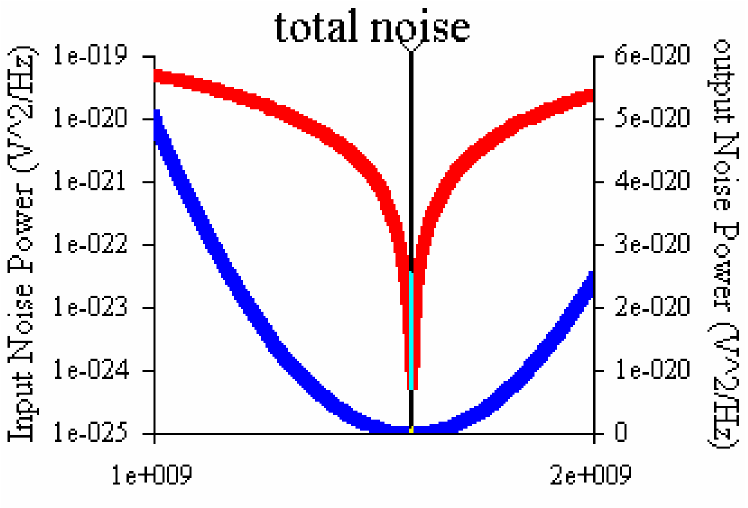


Fig (11) total noise

Also, the comparison of both matching technique is illustration in table (2) .

Table (2) Comparison between inductors matching and common gate matching Bi CMOS transistor

Inductors matching	Common gate matching
Low noise figure (NF = 0.01062 db)	High noise figure (NF = 0.25 db)
Large chip area A_{Ls} = 1.3816 e-7 m^2 A_{Lg} = 7.7874 e-5 m^2 $A_{trasistor}$ = 1.67185 e-17 m^2 A_{Ld} = 4.6616e-005 m^2 A_{total} = 125 μm^2	Small chip area A_{Ls} = 1.3816 e-7 m^2 A_{trans} = 1.67185 e-17 m^2 A_{Ld} = 4.6616e-005 m^2 A_{total} = 46 μm^2
Gain A_v = 268 dB	Gain A_v = 333 dB
Power dissipation 1.2 mW	Power dissipation 1.2 mW
Phase noise = 36.8 dB	Phase noise = 36.8 dB

Conclusions:

This paper is concerned with the optimal design of LNA for mobile communication. An optimization method is used to minimize the noise figure and reserving the other specification such as gain. Since LNA design is intended to be fabricated on single chip, a modified structure is developed to minimize the total chip area required for fabricator. The gain value of 268 dB, the area 125 μm^2, phase noise 36.8 dB and NF 0.01062 dB results have been obtained for the source degeneration matching, which is the best method for design low noise amplifier, was but high gain can be also be achieved by the common gate input matching which used to design the low noise amplifier.: where the gain vale of 333 dB, the area 64 μm^2, phase noise 36.8 dB and NF 0.25 dB have been obtained

Reference:

1. Ting Xie, Zhi-Heng Chen, Zhi–Gong Wang, "*A fully integrated 3.5 GHz 1.5v CMOS Low noise amplifier*" *Institute of RF & OE – ICs, Southeast University, and Nanjing, China 2001.*
2. Barry N. Breen, Chaim Goldberger and Leonid Talalaevsky, "*The accu-l multi-layer inductor for high frequency applications*", 2001.
3. Derek K. shaeffer, student Member, IEEE, and Thomas H.Lee, Member, IEEE, "*1.5 v, 1.5 GHz CMOS LNA*", J.solid-state circuit, Vol 32,PP 745 – 759, May 1997.
4. J.C. Rudell, J.J.ou, T.B.cho, G.chien, f. Briant, J. weldon, P.Gray, "*A 1.9 GHz wide band IF double conversion CMOS Receiver for cordless telephone applications*", IEEE journal of solid state circuit, vol. 32, no. 12, December 1997.
5. Vikas chandra. "*900 MHz RF CMOS Low noise amplifiers*" *Dept. of ECE, Carnegie Mellon University, Pittsburgh, pA 15231,2002.*
6. Cong Liu, Yinghua Li, "*Optimal design of CMOS LNA via geometric programming*". *EE227 final project march2001.*
7. Robert H. johns, "*Home brew your own inductors*", W3JIP, QST, Aug 1997, P35.
8. Nathan Sneed, "*A 2 GHz CMOS LC-Tuned VCO using Switched - capacitor to compensate for bond wire inductance variation*". University of California, Berkeley, December 2000.
9. T.H.Lee, Cambridge, "*The design of CMOS Radio frequency integrated circuit*", Cambridge University press, 1998, ch 11.