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Design and Implementation of a Low Losses Current-Fed Portable Induction Furnace

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Abstract: This research is concentrated on the practical design of a portable Induction Heating Furnace (IHF) composed of a Current-Fed Parallel Resonance Inverter (CFPRI) as a power supply of an Induction Coil (IC) and its specimen. The design is intended to reduce the losses in both the switches of the inverter and those due to non-sinusoidal currents in the conductors connecting the power supply components. The IC was connected in parallel to a suitable capacitor to form a tank load in this furnace. Detailed design steps for each implemented part are represented in this research. The implemented power supply tested practically on certain load. The practical results were compared with that obtained from the simulation for this system using the (Plecs) computer package. The practical results agreed with the simulation.

تصميم وتنفيذ فرن حثي محمول قليل الخسائر مغذى من مصدر تيار

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الخلاصة

يتركز هذا البحث على تصميم عملي لفرن تسخين حثي (IHF) محمول يتكون من عاكس رنين توازي يتغذى من مصدر تيار (CFPRI) يعمل كمجهز قدرة لملف حثي (IC) وعينته. تضمن التصميم تقليل كل من خسائر الأقلدة في مفاتيح العاكس وتلك الناتجة عن التيارات اللاجيبية في الموصلات التي تربط اجزاء المجهز. يربط الملف الحثي على التوازي مع المكثف المناسب لتشكيل حمل الخزان في هذا الفرن. تم في هذا البحث عرض التفاصيل للخطوات التصميمة لكل جزء تم تنفيذه. إن مصدر القدرة المنفذ تم إختباره عملياعلى حمل معين كما تمت مقارنة النتائج العملية مع تلك المستحصلة من محاكاة للمنظومة باستخدام حزمة حاسوبية تعرف بأسم (Plecs). إن النتائج العملية جاءت متوافقة مع نتائج المحاكاة.

الكلمات الدالة: فرن التسخين الحثي IHF، عاكس يتغذى من مصدر تيار CFI، عاكس ذاتي التنغيم،الدائرة المتكاملة لدارة إقفال الطور نوع (4046) (PLL IC 4046)، الدائرة المتكاملة (TCA785).

1.INTRODUCTION

Induction heating is a popular heat treatment technology in industrial and domestic products due to its higher efficiency, precise control, and lower emission characteristics than other heat treatment methods [1]. The most common power supply for induction heating is the CFPRI because the VFPRI switches suffer from high stresses [2-4], while low stress affects the CFPRI switches [5], reliable short-circuit, and overcurrent protection make it more suitable for high power applications. The purpose of this work is to design a reduced harmonic and switching losses power supply for a portable induction heating furnace (IHF). In this type of furnace, a long connector must exist between the IF power supply and the tank circuit load to afford flexibility in field applications. Then this connector must be specially designed to form a low inductance, low resistance, and low power loss since it carries a square wave current characterized by a high harmonic content. The main components of the IHF are shown in Fig.1. It is composed of a DC power source part as a three-phase FCFWR with its triggering circuit followed by an ($L\,C$) smoothing filter. The current fed to the H-bridge inverter forms the DC voltage source, passing through a choke coil to form a current source. This combination represents a current-fed parallel resonant inverter (CFPRI) [6]. The load is a parallel tank circuit, including the induction coil with its specimen and the suitable parallel tank capacitor. Due to the dependence of the induction coil equivalent circuit on the temperature variation during the heating process, changing the tank circuit resonance frequency, a self-tuned inverter was designed for this purpose using a feedback arrangement with a phase-locked loop (PLL) [7] tuning circuit. This work designs the triggering circuit of the FCFWR and the triggering and the PLL tuning circuits of the self-tuned H-bridge inverter. The implemented power supply showed approximately very close results to the simulation. The design seeks the reduction of the switching losses by obtaining the zero-phase shift between (v_{tank}) and (i_{tank}), which can be achieved when the inverter switching frequency corresponds to the resonance condition.

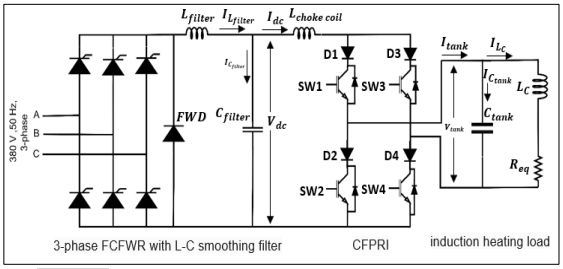

Fig. 1 The CFPRI for IHF Type LC Load.

2.CURRENT-FED PARALLEL-RESONANT INVERTER (CFPRI)

The idea of feeding the H-bridge inverter with a direct current source to form the CFPRI is to replace that known as a voltage-fed parallel resonant inverter (VFPRI). The output voltage of the CFPRI was of a sinusoidal waveform, while its current was a square wave. This feature leads to the following (Refer to Fig. 1):

$$\boldsymbol{V_{tank} = V_{C_{tank}}} \qquad \textbf{(1)}$$

$$\boldsymbol{I_{L_C} = Q \times I_{tank}} \qquad \textbf{(2)}$$

Where Q represents the quality factor of the tank circuit. Since I_{L_C} is an imaginary current, and I_{tank} is the real current, the inverter will only feed the real power, which means that the CFPRI is compatible with a high voltage low current DC source. On the contrary, the VFPRI is suitable for low voltage, high current DC sources. Fig. 1 depicts a diode in series with a switch because, if not used, the IGBT parallel diodes would cause the load-reactive current components to reach the DC source [8]. Current-source topologies provide low switching dv/dt and reliable short-circuit and overcurrent protection [9]. The following guidelines are necessary for the current-source inverter to function correctly: The top or bottom switches of the various legs cannot be

turned off simultaneously. Since a short circuit across the output voltage v_{tank} might result, each switch must have a diode connected in series unless the circuit will be damaged. In order to apply the theory practically, an overlapping time must be considered in the control signals of the top or bottom switches of the various legs. Due to the tank circuit load shown in Fig. 2, the equation describing its input impedance (Z_{in}) is [10]:

$$Z_{in} = R_{eq} + j\omega L_c + \frac{1}{j\omega C_{tank}} \quad (3)$$

$$Y_{in} = \frac{1}{R_{eq}+j\omega L_c} + j\omega C_{tank} \quad (4)$$

$$Y_{in} = \frac{R_{eq}-j\omega L_c}{R_{eq}^2+(\omega L_c)^2} + j\omega C_{tank} \quad (5)$$

$$Y_{in} = \frac{R_{eq}}{R_{eq}^2+(\omega L_c)^2} + \frac{-j\omega L_c}{R_{eq}^2+(\omega L_c)^2} + j\omega C_{tank} \quad (6)$$

Since, at resonance

$$\omega L_c = \omega C_{tank} \quad (7)$$

$$\frac{\omega L_c}{R_{eq}^2+(\omega L_c)^2} = \omega C_{tank} \quad (8)$$

$$R_{eq}^2 + (\omega L_c)^2 = \frac{L_c}{C_{tank}} \quad (9)$$

$$(\omega L_c)^2 = \frac{L_c}{C_{tank}} + R_{eq}^2 \quad (10)$$

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{L_c C_{tank}} + \left(\frac{R_{eq}}{L_c}\right)^2} \quad (11)$$

If $\frac{L_c}{C_{tank}} \gg R_{eq}^2$, the parallel resonance frequency may be simplified as:

$$f = \frac{1}{2\pi\sqrt{L_c C_{tank}}} \quad (12)$$

$$Q = \frac{reactive\ power}{real\ power} = \frac{I_{imag}}{I_{real}} \quad (13)$$

The relationship between the rms value of the fundamental component of the square wave output current of inverter (I_{tank}) at resonance condition as a function of the inputdirect current fed to the inverter (I_{dc}) is [11]:

$$I_{tank} = \frac{4}{\pi\sqrt{2}} I_{dc} \quad (14)$$

Since the real power dissipated in the equivalent resistance of the induction coil (P_{real}) due to tank circuit imaginary current passing in the induction coil (I_{L_C}) is:

$$P_{real} = I_{L_C}^2 R_{eq} = I_{tank} \cdot V_{tank} \cdot \cos\varphi \quad (15)$$

The following features apply to current-fed inverters (CFIs) [12]:

1- For the commutation process, overlap time is necessary; then the switching stages of the inverter are as follows [13]:
   - **a)** SW1 and SW4 were ON during the positive half cycle.
   - **b)** SW1, SW2, SW3, and SW4 were ON, during the overlap time.
   - **c)** SW2 and SW3 were ON during the negative half cycle.
   - **d)** SW1, SW2, SW3, and SW4 were ON, during the overlap time.

2- In the event of a short circuit, all semiconductors were required to conduct.

3- ZVS occurred at the resonance frequency.

4- ZCS occurred above the resonance frequency.

5- Transistors must be capable of handling high voltage.

Parasitic inductance (L_p), due to the parasitic inductances of the switches, diodes, and connectors, is a source of high voltage stress across the switches which might cause the degradation of semiconductors. The parasitic inductances also influence the switching process when the inverter's commutation is capacitive. Still, when L_p is considered, the voltage at the inductance's terminals opposes the voltage on the tank. Hence, commutating at capacitive switching offers a more dependable inverter operation when considering L_p. Capacitive switching is favored in CFPRI, even if the reverse recovery currents on diodes are still an issue. A detailed analysis is in references [8,14] about the quality factor (Q) effect on the suitable switching frequency for perfect ZCS and ZVS conditions. This analysis reveals that for a high (Q) tank circuit, the resonance frequency and the zero-phase shift frequency will be very close. It is preferable to choose the switching frequency in the capacitive region to avoid the severe effect of L_p on the switches' safety and reduce the switching losses during the heating process.

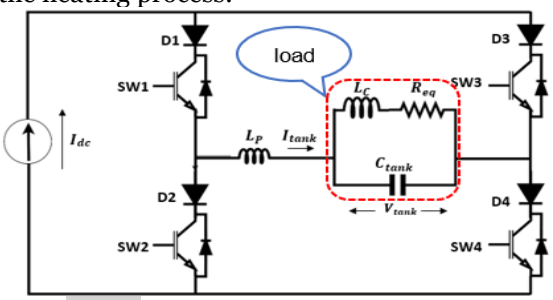

Fig. 2 CFPRI Considering Parasitic Inductances L_p.

3. THE PLECS SIMULATION AND RESULTS

In this study, the power supply of the IHF feeding linear specimen load is of a high-quality factor (Q). Fig.3 depicts the simulation circuit diagram for the IHF. The system was powered by a mains transformer of 1 MVA, i.e., 3-phase, 380 V, and 50 Hz, with secondary equivalent resistance and inductance of 612.5 μΩ and 12.5 μH, respectively. By passing its output voltage via an L-C smoothing low-pass filter with L_{filter} = 2.9 mH and C_{filter} = 13200 μF,

the FCFWR rectifies this AC voltage. In this design, a chock coil $L_{chock\ coil}$ = 50 mH acted as a current source, simulating a low-ripple variable DC voltage power source. According to Eq. (12), the tank circuit's induction coil L_c=3 µH, tank capacitor C_{tank} = 10 µF, and the resonance frequency (28.57 kHz) are required. To account for the loads, the equivalent load resistance (R_{eq}) was modified to (0.1Ω). For each case, three different applied terminal voltages were assessed by changing the FCFWR's triggering angle to ($42.74^{\circ}, 60^{\circ}$, and 75°). Fig. 3 displays the simulated circuit diagram created by the Plecs computer package. When (R_{eq} = 0.1 Ω) and ($\alpha = 42.74^{\circ}$) was the triggering angle, the system voltages were expressed as follows: Accordingly, Figs. 4-7. show the input voltage of phase A, the voltage across the chock coil, the DC voltage supplied to the inverter terminals, and the output voltage of the inverter. The cause of this disturbance in the input voltage occurred due to the non-sinusoidal input current feeding the controlled rectifier shown in Fig. 8. The four sharping edges (up and down) in the current waveform caused four disturbances in the voltage waveform since $\{v = L(di/dt)\}$. Figs. 8-19. Show the system currents and their harmonics for the input current of phase A, the direct current of the filter, the capacitor filter current, the input current fed to the inverter, the output current from the inverter feeding the tank circuit, and the induction coil current. These figures include all of the harmonics in each current according to the descriptions of load and triggering angles given below.

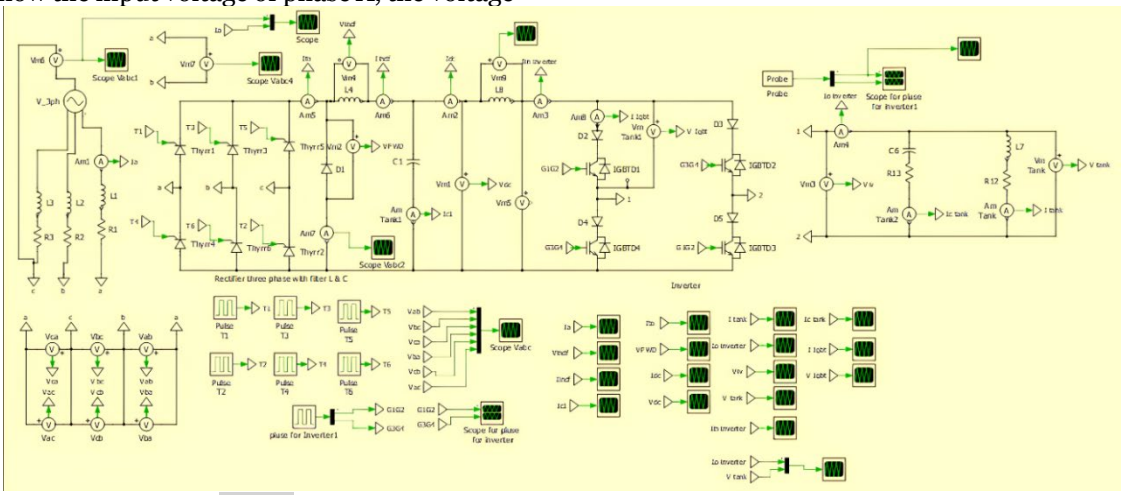

Fig. 3 Simulation Circuit of the IHF Using Plecs Software.

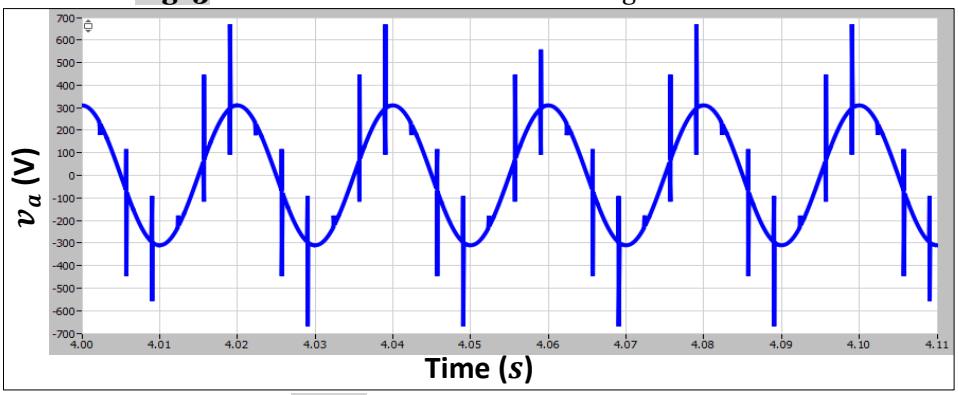

Fig. 4 Input Voltage Per Phase.

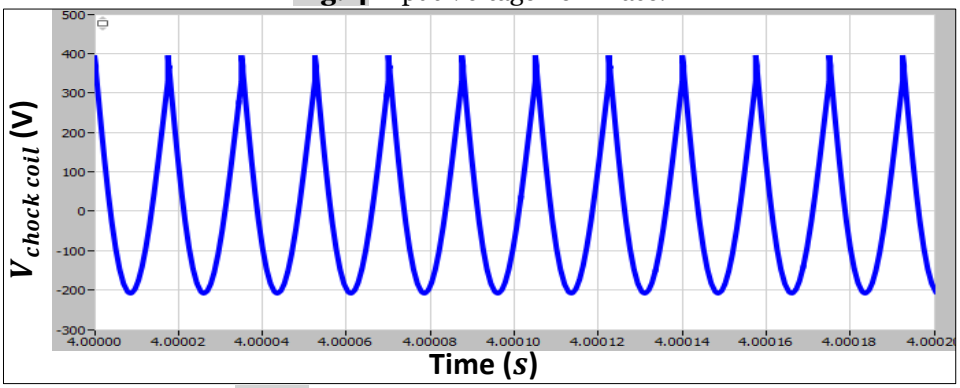

Fig. 5 The Voltage Across the Chock Coil.

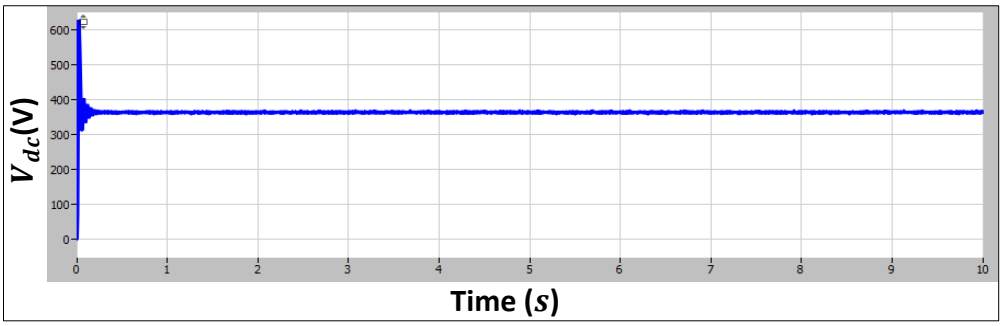

Fig. 6 The DC Voltage.

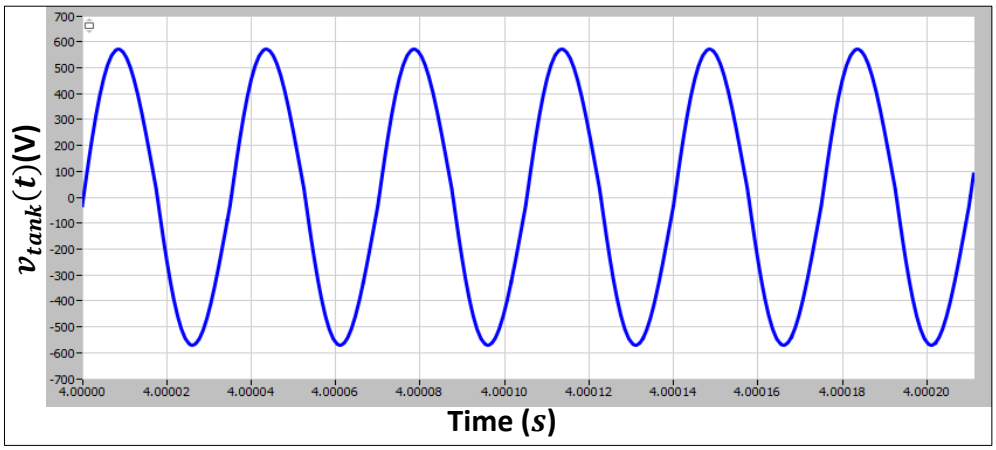

Fig. 7 The Inverter Output Voltage.

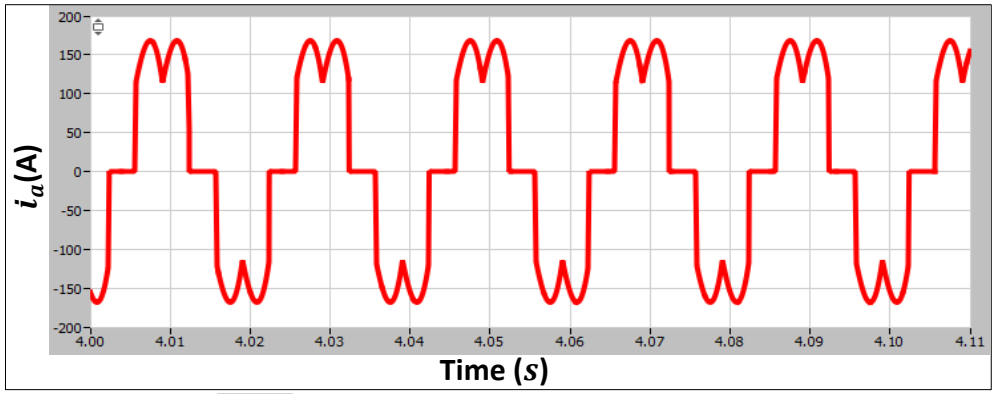

Fig. 8 An Input Current's Phase (A) Waveform.

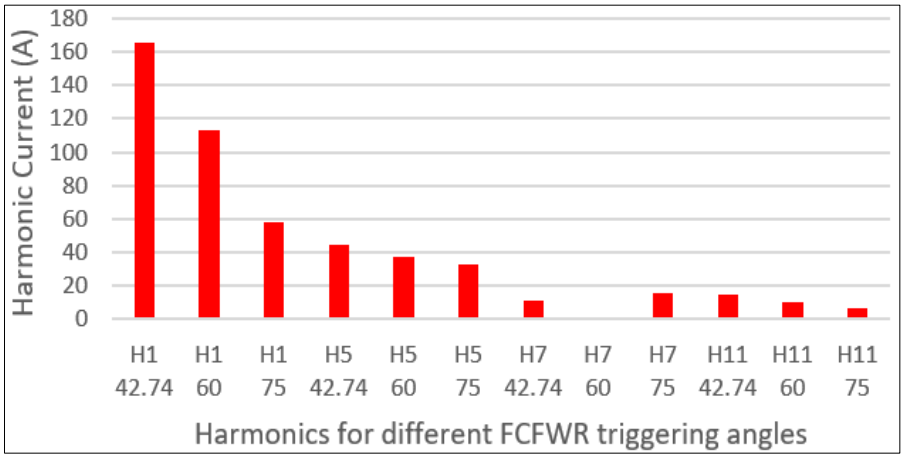

Fig. 9 The Harmonic Current of Phase (A) of 50 Hz, for Load Resistance $R_{eq} = 0.1\ \Omega$ at Different Triggering Angles $\alpha = 42.74^{\circ}, 60^{\circ}$, and 75°.

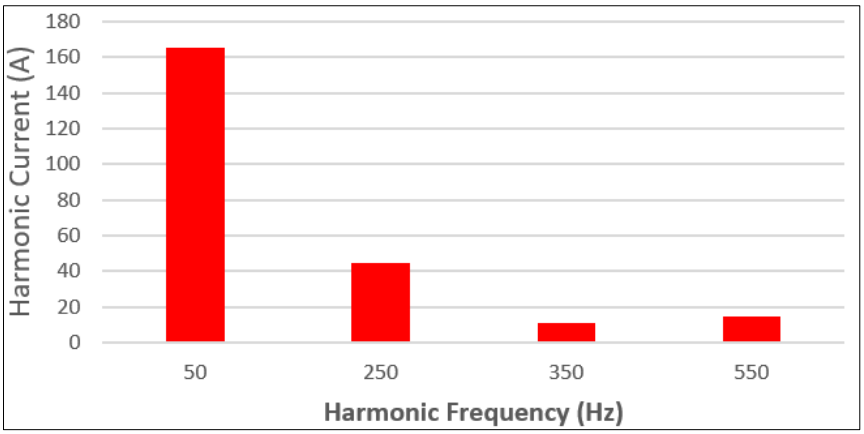

Fig. 10 The Phase (A) Harmonic Currents at $\alpha = 42.74^{\circ}$ and $R_{eq} = 0.1\ \Omega$.

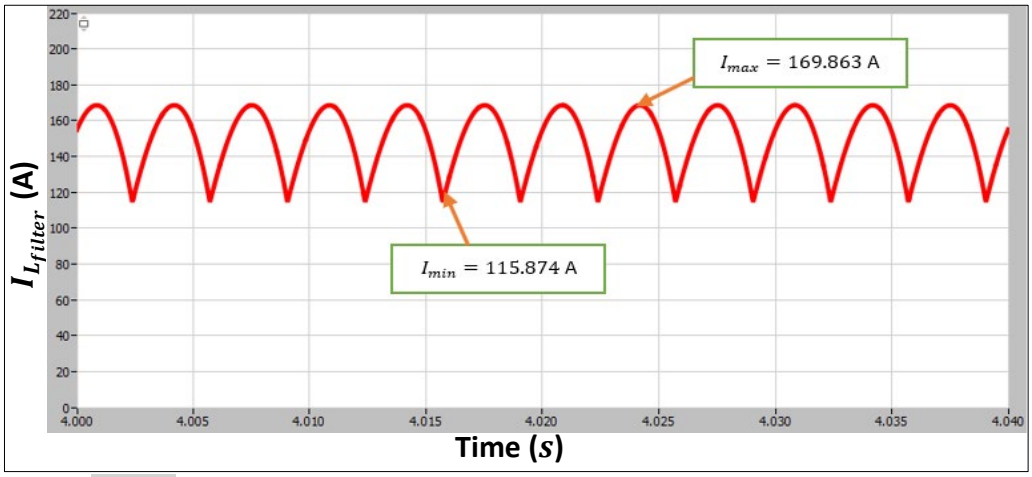

Fig. 11 Direct Current Passing Through L_{filter} of ($6f_s = 300$ Hz) Ripples.

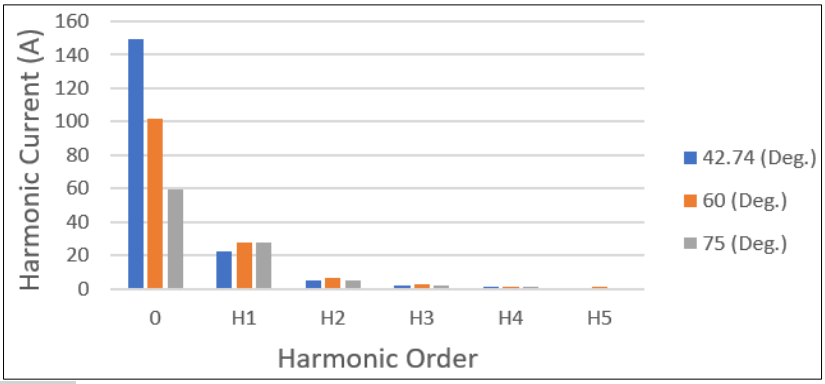

Fig. 12 When $R_c = 0.1\ \Omega$, the Direct Current Flowing in the Smoothing Coil has a Fundamental Frequency of (300 Hz) at $\alpha = 42.74^{\circ}, 60^{\circ}$, and 75°.

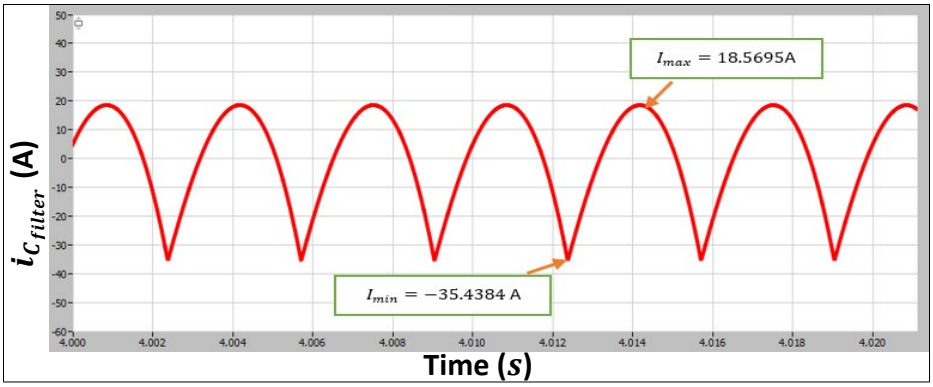

Fig. 13 The Current of the Filter Capacitor at (300 Hz).

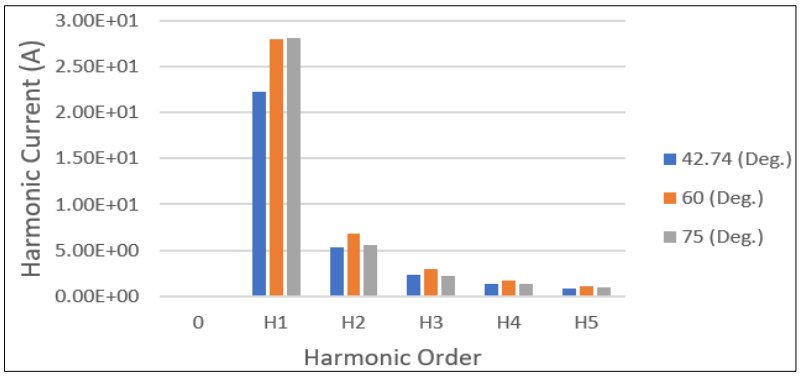

Fig. 14 The Harmonic Current of the Fundamental Frequency of (300 Hz) of the Current that Flows to the Capacitor Filter at $R_{eq} = 0.1\ \Omega$ and $\alpha = 42.74^{\circ}, 60^{\circ}$, and 75°.

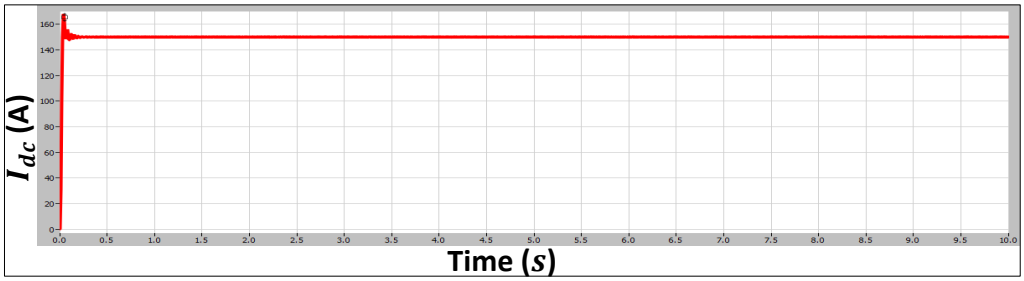

Fig. 15 The Waveform of the Inverter's Input Current.

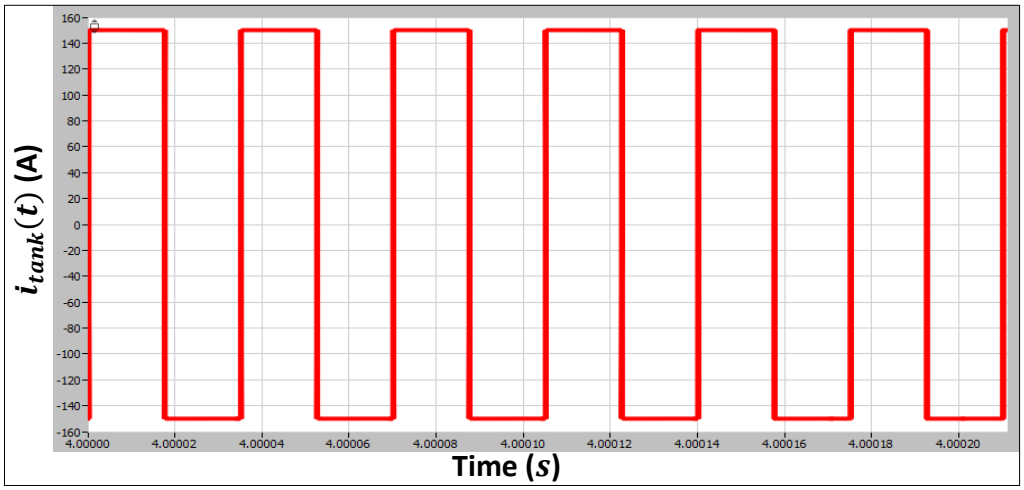

Fig. 16 The Inverter Output Current Waveform (f_r).

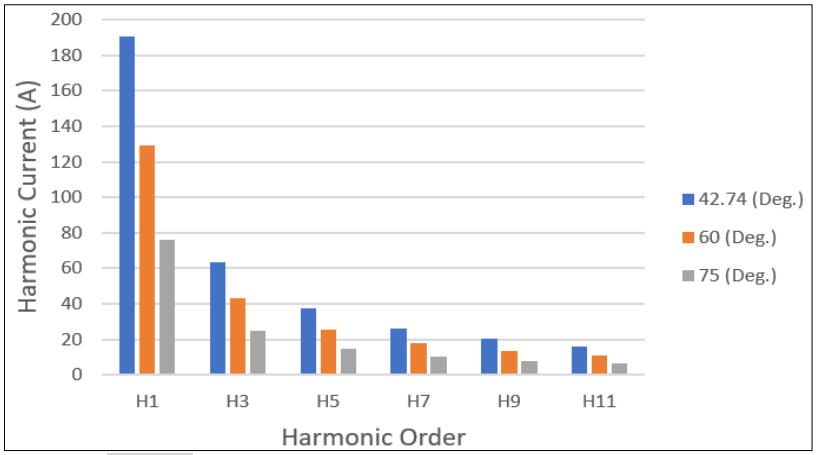

Fig. 17 The Harmonics Current of the Fundamental Frequency of (28570 Hz) of (i_{tank}) at $R_{eq} = 0.1\ \Omega$ and $\alpha = 42.74^{\circ}, 60^{\circ}$, and 75°.

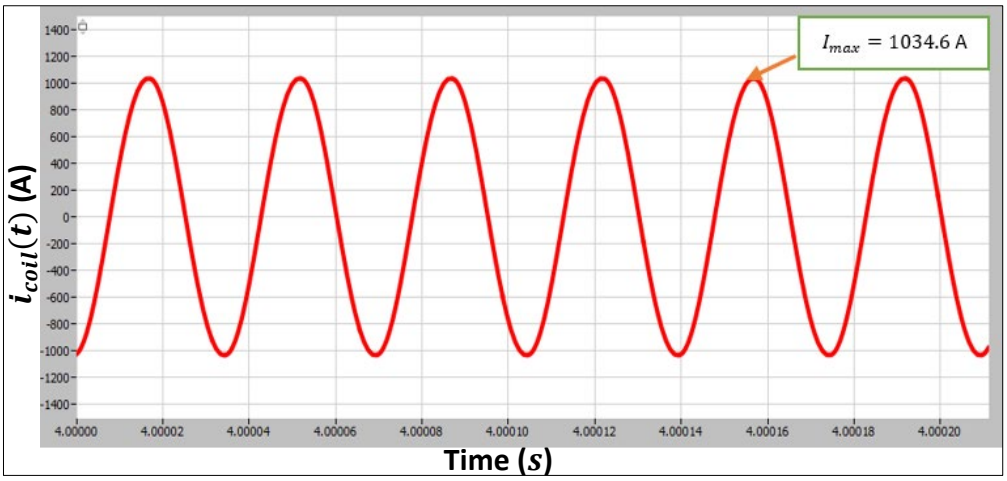

Fig. 18 The Current Flowing Through an Induction Coil at the Resonance Frequency (f_r).

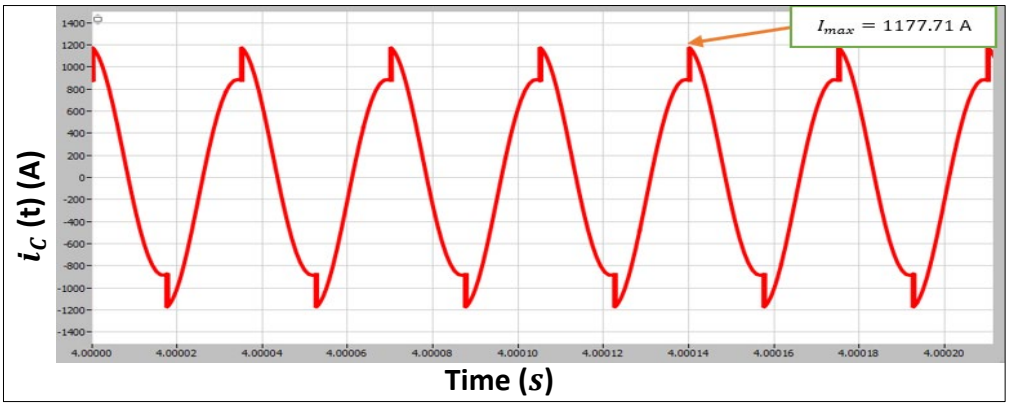

Fig. 19 The Capacitor Current at the Resonance Frequency (f_r).

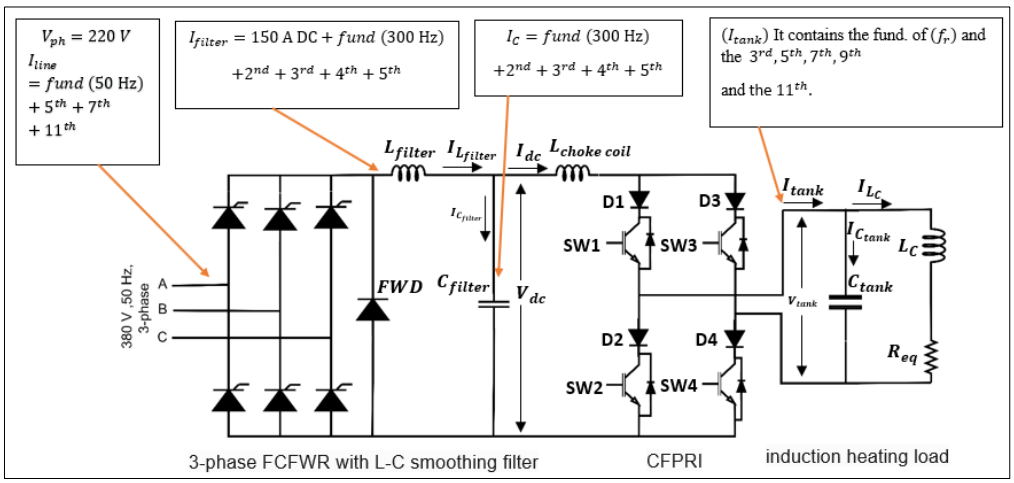

Fig. 20 The CFIHF Power Supply's Harmonics in Each Branch.

Due to the harmonic results abbreviated in Fig.20, the most severe contents of harmonics were that at the connector carrying the square wave current from the inverter feeding the *LC* tank circuit load. Hence, this connector must be designed to reduce the heat generation within it during the process and reduce the voltage drop across it due to its length in such furnaces. Also, its self-inductance must be as small as possible. Practically, it is noticed that when using a traditional copper connector between the inverter terminals and the tank load, this connector was subjected to a continuous increase in its temperature during the operation time, and it reached an unacceptable range of temperature. To reduce the drop in the applied voltage across its terminals and to avoid the continuous increase in its temperature, the same procedure adopted by the reference [15] was applied, as shown below:

(a) Determine the severest amplitude of the fundamental harmonic shown in the above

results to choose the most suitable Litz's wire gauge from the AWG table, considering that the frequency closest less than or equal to that of the fundamental frequency.

(b) From the data given in the AWG table of that chosen wire gauge, the rated power per meter length of that wire (P_r) can be calculated by applying the commonly used power equation ($P_r = I_r^2 R_W$), where (I_r) in (A) is the rated current of that gauge, and R_W is its resistance per unit length of that chosen wire.

(c) The chosen wire resistance with respect to each harmonic can be found by referring to Fig.21, which describes the harmonic effective area $\left(A_{nr_{eff}}\right)$, and applying the following equations consequently:

$$\delta_{nr} = 503\sqrt{\frac{\rho_{cu}}{n f_r \mu_{r_{cu}}}} \quad (16)$$

$$r_{nr_{int}} = r_{ext} - \delta_{nr} \quad (17)$$

$$A_{nr_{eff}} = \pi\left(r_{ext}^2 - r_{nr_{int}}^2\right) \quad (18)$$

$$R_{nr_{eff}} = \rho_{cu}\frac{l}{A_{nr_{eff}}} \quad (19)$$

l: Wire length in (m).

ρ_{cu}: Electrical resistivity of copper = $(17.2359244 \times 10^{-9})$in $(\Omega \cdot \mathrm{m})$.

r_{ext}: The radius of the chosen copper conductor $(r_{ext} = r_w)$ for the fundamental frequency. It was considered an external radius with respect to the other highest harmonics.

$r_{nr_{int}}$:The internal radius of the harmonic effective area (m).

f_{nr}: The frequency of the harmonic of order (n) (Hz).

$\mu_{r_{cu}}$: The copper relative permeability =(0.9793025) .

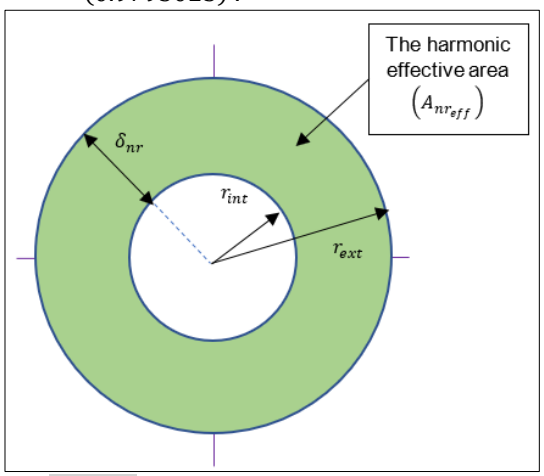

Fig. 21 The Harmonic Effective Area.

Due to the obtained spectrum of (i_{tank}), shown in Fig. 17, represents the highest load current value leading to dissipating 52 kW power in the specimen and requiring input DC power of 57 kW, with a system theoretical efficiency of about 91%. Since the fundamental frequency f_r = 28.570 kHz, the nearest compatible wire gauge was gauge number (20) due to the AWG with the following data, as shown in Table 1.

Table 1 Litz's Wire Gauge (20) Bata Due to AWG [16].

Gauge No.	f_{20} (kHz)	d_{20} (mm)	R_{20} ($\Omega \cdot \mathrm{m}^{-1}$)	$I_{rated_{20}}$ (A)	$P_{r_{20}}$ (W)
20	27	0.8128	0.033292	11	4

To calculate the ability of the rated power dissipated along the unit length of Litz's wire of gauge (20) $\left(P_{r_{20}}\right)$, the following formula can be used:

$$P_{r_{20}} = I_{rated_{20}}^2 \times R_{20} \quad (20)$$

$$\therefore P_{r_{20}} = (11)^2 \times 0.033292 = 4.028332 \text{ W}$$

Then using Eqs. (16)–(19) to calculate the $R_{nr_{eff}}$ for each harmonic in Ohm per unit length of the connector using Litz's wire of gauge (20). To calculate the total drop in voltage per unit connector length for each harmonic current $\left(V_{nr_{drop}}\right)$, the following formula can be used:

$$V_{nr_{drop}} = I_{nr_{rms}} \times R_{nr_{eff}} \quad (21)$$

Also, the power dissipated due to the harmonic current in the unit length of the connector can be calculated from

$$P_{nr_{loss}} = I_{nr_{rms}}^2 \times R_{nr_{eff}} \quad (22)$$

These data are represented in Table 2.

The total drop in the voltage along the unit length of the conductor due to the total harmonics ($V_{Tnrdrop}$) is:

$$V_{Tnr_{drop}} = \sum_{n=1}^{n=11} V_{nr_{drop}} \quad (23)$$

$$\therefore V_{Tnr_{drop}} = 16.663 \text{ V} \cdot \mathrm{m}^{-1}$$

Similarly, the total dissipated power due to harmonic currents per unit length of the conductor $\left(P_{Tnr_{loss}}\right)$ will be:

$$P_{Tnr_{loss}} = \sum_{n=1}^{n=11} P_{nr_{loss}} \quad (24)$$

$$\therefore P_{Tnr_{loss}} = 893.692 \text{ W} \cdot \mathrm{m}^{-1}$$

Hence, the total number of Litz's wires of gauge (20) required for this connector (N_{20}) is:

$$N_{20} = \frac{P_{Tnr_{loss}}}{P_{r_{20}}} \quad (25)$$

$$\therefore N_{20} = \frac{893.692}{4.028332} = 221.851 \cong 222 \text{ Wires}$$

The designed cable will dissipate $P_{r_{20}}$ W per unit length and cause a drop in voltage for each meter of length $V_{drop_{20}}$ equals:

$$V_{drop_{20}} = \frac{V_{Tnr_{drop}}}{N_{20}} \quad (26)$$

$$\therefore V_{drop_{20}} = 0.0750\ \mathbf{V \cdot m^{-1}}$$

To reduce the parasitic inductance of this group of 222 Litz's wires, they must be divided into two groups of 111 wires, and every two wires of each group twisted together, such that the twisting of the first group must be in CW sense, while that of the other group must be in CCW sense. This arrangement will reduce the stray inductance of this connector drastically. Hence, the connector will be quite suitable when connected to the CFPRI induction heating furnace.

Table 2 Harmonics Data.

$I_{tank}(\mathrm{A})\ R = 0.1\Omega\ \alpha = 42.74^0, \mathrm{THD} = 48.5035\%$

n	f_{nr} (kHz)	$I_{nr_{max}}$ (A)	$I_{nr_{rms}}$ (A)	δ_{nr} (m)	$r_{nr_{int}}$ (m)	$A_{nr_{eff}}$ ($\mathrm{m^2}$)	$R_{nr_{eff}}$ ($\Omega \cdot \mathrm{m^{-1}}$)	$V_{nr_{drop}}$ ($\mathrm{V \cdot m^{-1}}$)	$P_{nr_{loss}}$ ($\mathrm{W \cdot m^{-1}}$)
1	28.570	190.374	134.615	3.948×10^{-4}	1.16×10^{-5}	5.184×10^{-7}	0.03324	4.474	602
3	85.710	63.1393	44.646	1.316×10^{-4}	$2.748 \times^{-4}$	$2.816 \times^{-7}$	0.06120	2.732	121.987
5	142.850	37.5031	26.540	7.896×10^{-5}	3.2744×10^{-4}	1.820×10^{-7}	0.09470	2.513	66.703
7	199.990	26.3853	18.657	5.640×10^{-5}	3.5×10^{-4}	1.340×10^{-7}	0.12862	2.399	44.770
9	257.130	20.1116	14.221	4.386×10^{-5}	3.6254×10^{-4}	1.059×10^{-7}	0.16275	2.314	32.914
11	314.270	16.0452	11.345	3.590×10^{-5}	3.705×10^{-4}	8.762×10^{-8}	0.19671	2.231	25.318

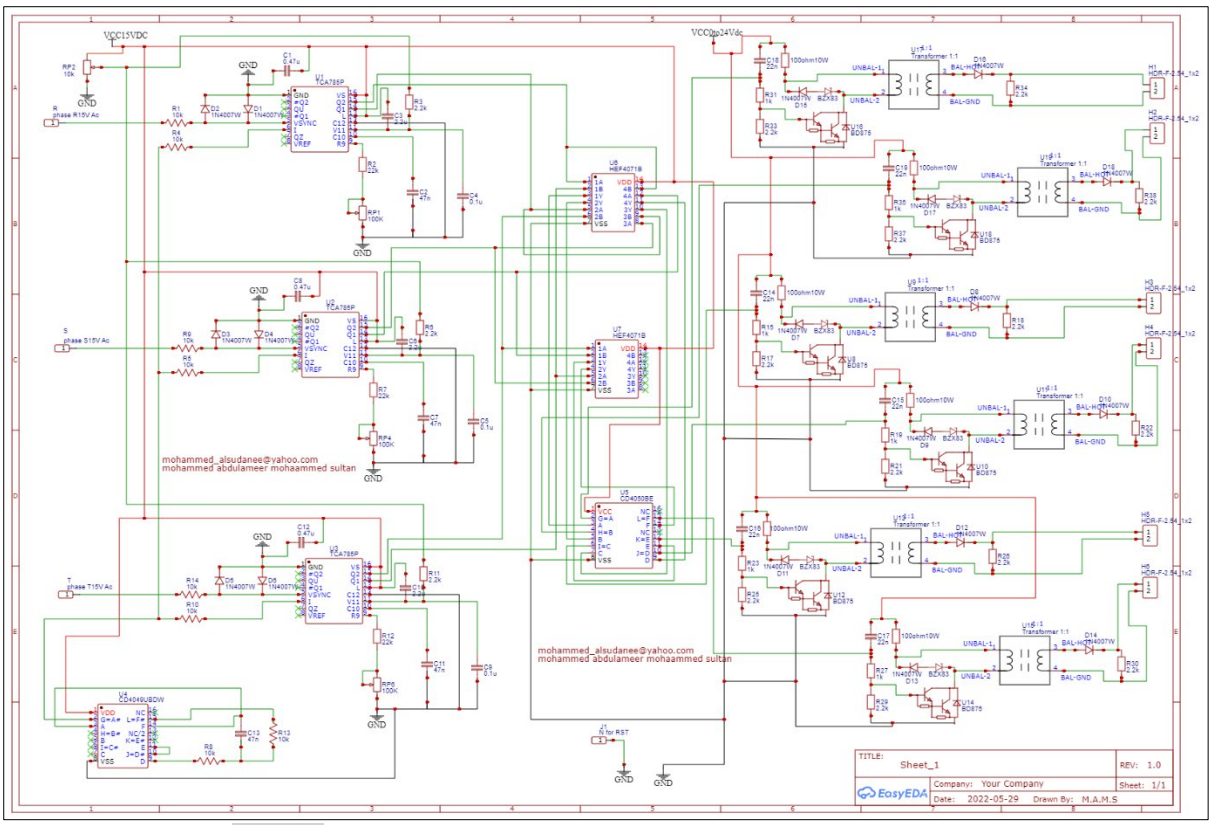

Fig. 22 Circuit Diagram of the Firing Unit for the 3-Ø FCFWR.

4. TRIGGERING CIRCUIT FOR THE 3-Ø FCFWR

The most important part of designing the FCFWR is the triggering circuit. The circuit diagram is shown in Fig. 22 using the integrated circuit (TCA785) [17]. Its data sheet is addressed in Appendix (A). The trigger angle can be changed from 0° to 120° by variable resistance to feed a variable DC voltage from 513 V to 0 V. The power circuit consists of six thyristor type SEMICRON (SKKT 132), see Appendix (B), and FWD type SEMICRON (SKKD 212), see Appendix (C), as shown in Fig.23 representing the implemented circuit.

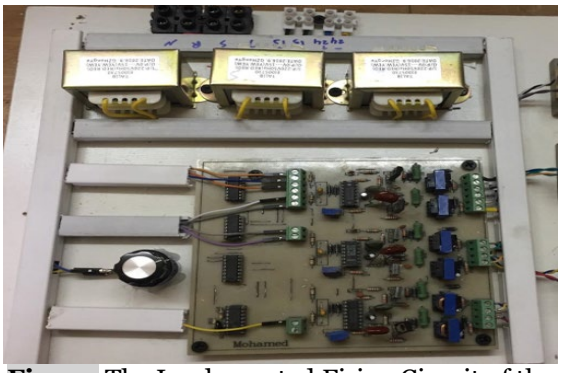

Fig. 23 The Implemented Firing Circuit of the FCFWR.

To get a smooth DC voltage, the rectified voltage was applied to an *LC* filter, as shown in Fig. 24. The filter was composed of a 2 mH coil designed by [18], but by reducing its airgap, its self-inductance reached a value 2.9 mH. The capacitor of 800 V and 13200 μF was used to obtain an acceptable smoothing of the output DC voltage in a high triggering angle.

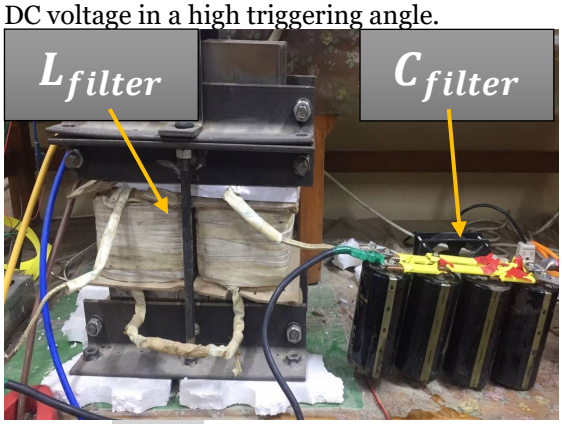

Fig. 24 Smoothing LC filter.

The LC filter represents a Low pass filter. The cutoff frequency due to Eq. (27) is 25.72 kHz.

$$f = \frac{1}{2\pi\sqrt{L_{filter}\, C_{filter}}} \qquad (27)$$

5.PULSE GENERATOR FOR H-BRIDGE INVERTER

PLL IC 4046 was used to generate gate pulses for the inverter; see Appendix (D). During the heating cycle, the induction heating load equivalent resistance and inductance effective characteristics changed [19-22]. So, to keep the inverter's power factor close to unity, it becomes essential to synchronize the operating frequency with that of the tank circuit. A crucial component of the inverter's functioning for this purpose is the phase-locked loop (PLL) [6] control circuit, as seen in Fig. 25. The former's job is to maintain a zero cross-current switching mode regardless of load changes, which suggests that the switching frequency of the IGBT must be changed, based on the resonance frequency of the inverter load circuit while it is in operation. A resonant frequency tracking control circuit developed around the CMOS PLL [23-25] chip MC14046B achieved the needed performance using a phase shifter, two comparators, an integrator, and a low-pass filter. The IGBT's Driving Circuits and the water-cooled heat sink for IGBT, see Appendix (E).

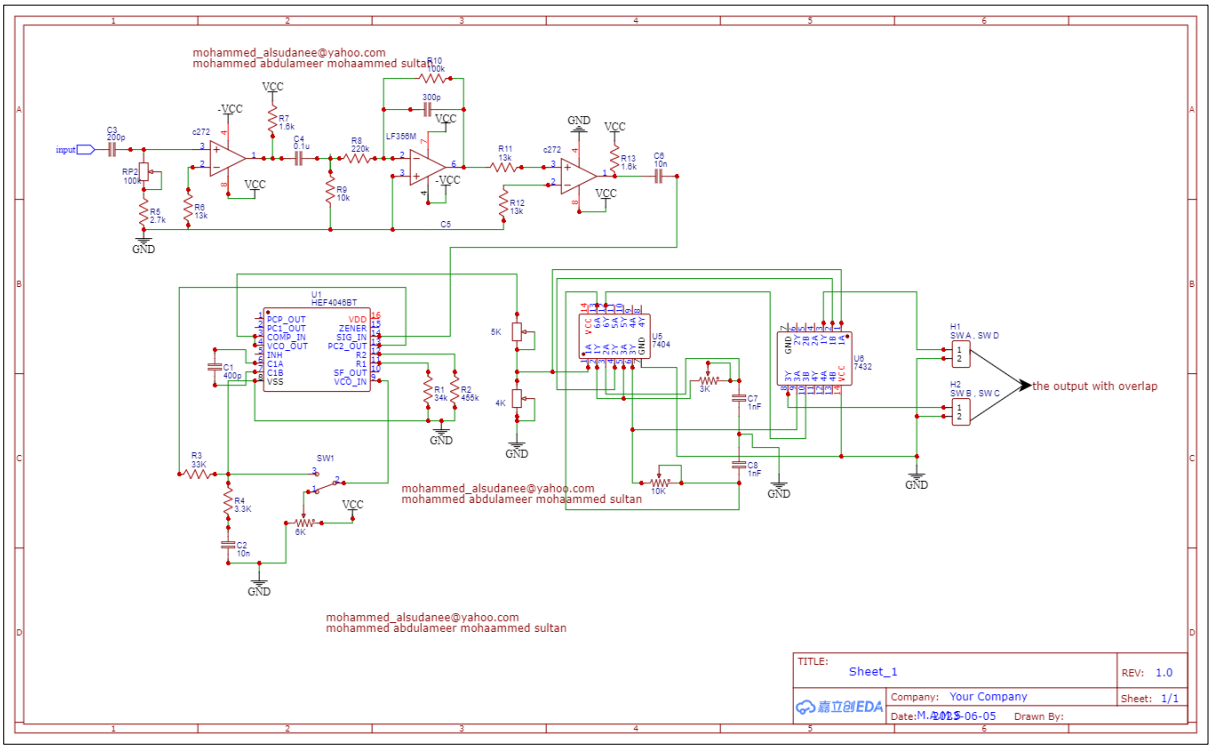

Fig. 25 Circuit Diagram PLL IC 4046.

6.PRACTICAL AND SIMULATION RESULTS

In this section, the practical results were compared with the corresponding simulation results. These findings were: The self-inductance of the induction coil L_C = 2.08 μH, parallel tank capacitor 40 μF, and the switching frequency $f_s = f_r$ = 17450 Hz. Fig. 26. represents measurements of the direct current and voltage fed to the inverter, while Figs. 27-29 represent the practical and simulation results of the inverter current, the capacitor voltage, and the IGBT voltage, respectively. Fig.30. shows the capacitive operation of the CFPRI.

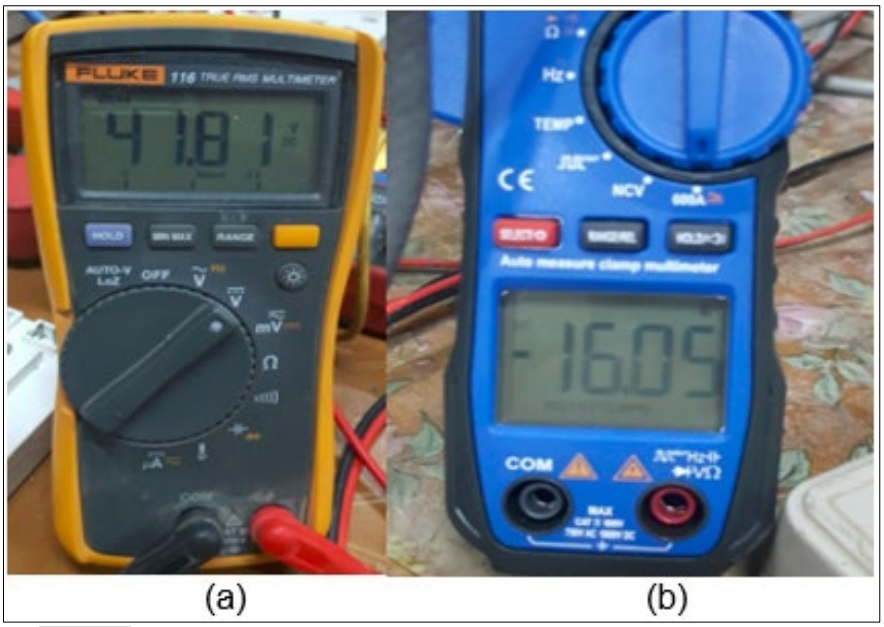

Fig. 26 Practical Measurement of (a) DC Voltage (b) Direct Current.

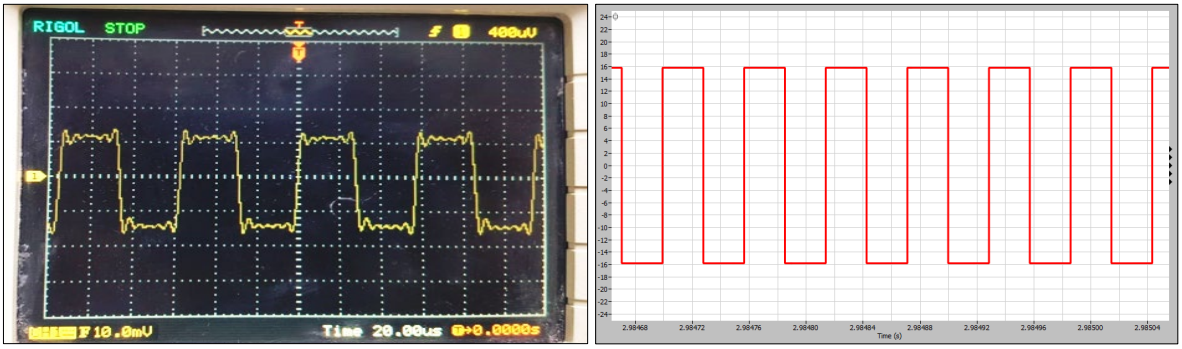

Fig. 27 (a) Experimental Inverter Current Waveform (10 A/div) (b) Simulation Waveform.

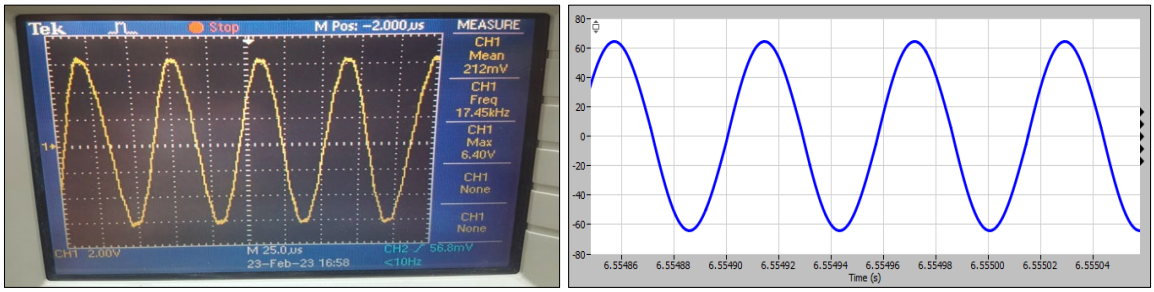

Fig. 28 Voltage Across the Capacitor (20 V/div) Waveform (a) Experimental (b) Simulation.

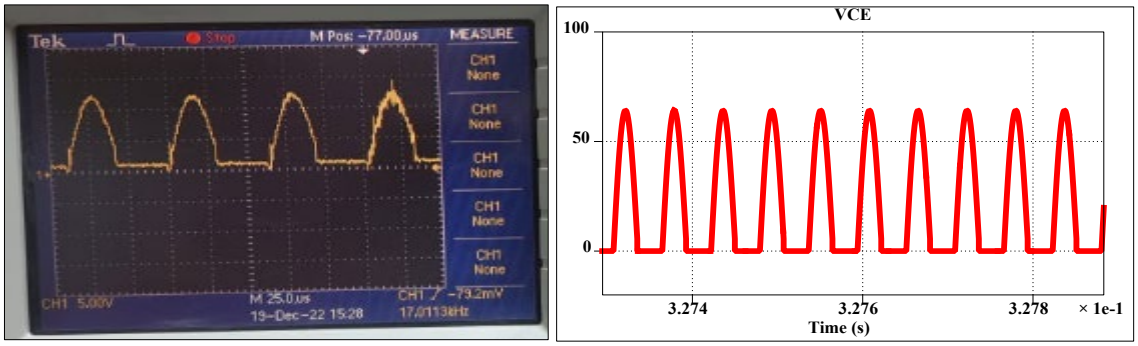

Fig. 29 V_{CE} at a Resonant Frequency in CFI Waveform (a) Experimental (b) Simulation.

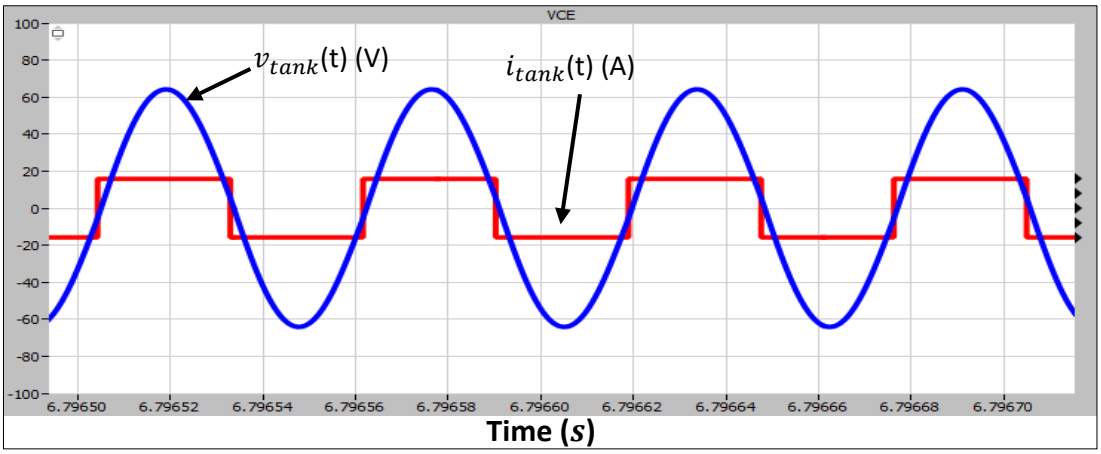

Fig. 30 The Capacitive Switching Case $\varphi = 5^{\circ}$ Leading.

From the result calculation, the power and R_{eq}:

$$I_{dc} = 16.05\ \text{A and}\ V_{dc} = 41.81\ \text{V}$$

$$p_{dc} = I_{dc} \times V_{dc} = 16.05 \times 41.81 = 671.0505\ \text{W}$$

$$I_{tank} = \frac{4I_{dc}}{\pi\sqrt{2}} = \frac{4 \times 16.05}{\pi\sqrt{2}} = 14.45\ \text{A}$$

$$V_{tank} = \frac{V_{tank(peak)}}{\sqrt{2}} = \frac{64}{\sqrt{2}} = 45.255\ \text{V}$$

$$P_{inv} = I_{tank} \times V_{tank} \times \cos 5^{\circ} = 651.446\ \text{W}$$

$$I_{L_C} = \frac{V_{tank}}{X_l} = 198.4724735\ \text{A}$$

$$R_{eq} = \frac{P_{in}}{I_{L_C}^2} = \frac{651.446}{198.4724735^2} = 0.01654\ \Omega$$

$$Q = \frac{I_{L_C}}{I_{tank}} = \frac{198.4724735}{14.45} = 13.735$$

Also, the efficiency [26] is:

$$\eta\% = \frac{p_{out}}{p_{in}} \times 100\% = \frac{P_{inv}}{P_{DC}} \times 100\% = \frac{651.446}{671.0505} \times 100 = 97.078\%$$

Fig. 31 depicts the induction coil with its hollow copper tube, which reached a temperature of 417 ℃.

Fig. 31 The Induction Coil During the Practical Test of the Designed CFPRI.

7.CONCLUSION

- Since the FCFWR was supplied from an efficient transformer of 1MVA, then this explains the undistorted input voltage from the mains despite the highly distorted current per phase due to the switching effects. Hence, the operation of this furnace in this lab negligibly affected other loads.
- Since the tank circuit quality factor was 13.735, i is considered a high-quality factor, and the switching frequency will be the resonance frequency of the tank circuit despite a capacitive operation shown in Fig. 15.
- The practical work declares the importance of the design steps of the connector delivering the power from the inverter to the load to protect the inverter switches and increase the system efficiency.
- The current-fed inverter operation in induction heating is preferable to the voltage-fed inverter in a high-power application. However, it must be loaded in the capacitive mode of operation.

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Appendix (A)
Datasheet of TCA785

SIEMENS

Phase Control IC

TCA 785

Bipolar IC

Features

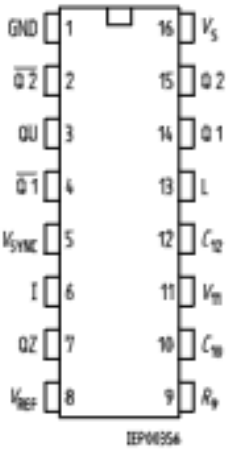
- Reliable recognition of zero passage
- Large application scope
- May be used as zero point switch
- LSL compatible
- Three-phase operation possible (3 ICs)
- Output current 250 mA
- Large ramp current range
- Wide temperature range

P-DIP-16-1

Type	Ordering Code	Package
TCA 785	Q67000-A2321	P-DIP-16-1

This phase control IC is intended to control thyristors, triacs, and transistors. The trigger pulses can be shifted within a phase angle between 0 ° and 180 °. Typical applications include converter circuits, AC controllers and three-phase current controllers.

This IC replaces the previous types TCA 780 and TCA 780 D.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	$\overline{Q2}$	Output 2 inverted
3	Q U	Output U
4	$\overline{Q2}$	Output 1 inverted
5	V_{SYNC}	Synchronous voltage
6	I	Inhibit
7	Q Z	Output Z
8	V_{REF}	Stabilized voltage
9	R_9	Ramp resistance
10	C_{10}	Ramp capacitance
11	V_{11}	Control voltage
12	C_{12}	Pulse extension
13	L	Long pulse
14	Q 1	Output 1
15	Q 2	Output 2
16	V_S	Supply voltage

Semiconductor Group 1 09.94

Appendix (B)
Datasheet of SEMICRON thyristor type (SKKT 132)

SKKT 132, SKKH 132

SEMIPACK® 2

Thyristor / Diode Modules

SKKT 132
SKKH 132

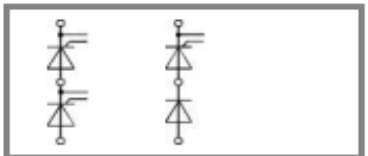
Features

- Heat transfer through aluminium oxide ceramic isolated metal baseplate
- Hard soldered joints for high reliability
- UL recognized, file no. E 63532

Typical Applications*

- DC motor control (e. g. for machine tools)
- Temperature control (e. g. for ovens, chemical processes)
- Professional light dimming (studios, theaters)

1) See the assembly instructions



SKKT SKKH

V_{RSM} V	V_{RRM}, V_{DRM} V	I_{TRMS} = 220 A (maximum value for continuous operation) I_{TAV} = 130 A (sin. 180; T_c = 87 °C)	
900	800	SKKT 132/08E	SKKH 132/08E
1300	1200	SKKT 132/12E	SKKH 132/12E
1500	1400	SKKT 132/14E	SKKH 132/14E
1700	1600	SKKT 132/16E	SKKH 132/16E
1900	1800	SKKT 132/18E	SKKH 132/18E

Symbol	Conditions	Values	Units
I_{TAV}	sin. 180; T_c = 85 (100) °C;	137 (96)	A
I_D	P3/180; T_a = 45 °C; B2 / B6	77 / 100	A
	P3/180F; T_a = 35 °C; B2 / B6	170 /200	A
I_{RMS}	P3/180F; T_a = 35 °C; W1 / W3	240 / 3 * 163	A
I_{TSM}	T_{vj} = 25 °C; 10 ms	4700	A
	T_{vj} = 125 °C; 10 ms	4000	A
i^2t	T_{vj} = 25 °C; 8,3 ... 10 ms	110000	A^2s
	T_{vj} = 125 °C; 8,3 ... 10 ms	80000	A^2s
V_T	T_{vj} = 25 °C; I_T = 500 A	max. 1,8	V
$V_{T(TO)}$	T_{vj} = 125 °C	max. 1	V
r_T	T_{vj} = 125 °C	max. 1,6	mΩ
I_{DD}; I_{RD}	T_{vj} = 125 °C; V_{RD} = V_{RRM}; V_{DD} = V_{DRM}	max. 40	mA
t_{gd}	T_{vj} = 25 °C; I_G = 1 A; di_G/dt = 1 A/µs	1	µs
t_{gr}	V_D = 0,67 * V_{DRM}	2	µs
$(di/dt)_{cr}$	T_{vj} = 125 °C	max. 200	A/µs
$(dv/dt)_{cr}$	T_{vj} = 125 °C	max. 1000	V/µs
t_q	T_{vj} = 125 °C ,	50 ... 150	µs
I_H	T_{vj} = 25 °C; typ. / max.	150 / 400	mA
I_L	T_{vj} = 25 °C; R_G = 33 Ω; typ. / max.	300 / 1000	mA
V_{GT}	T_{vj} = 25 °C; d.c.	min. 2	V
I_{GT}	T_{vj} = 25 °C; d.c.	min. 150	mA
V_{GD}	T_{vj} = 125 °C; d.c.	max. 0,25	V
I_{GD}	T_{vj} = 125 °C; d.c.	max. 10	mA
$R_{th(j-c)}$	cont.; per thyristor / per module	0,18 / 0,09	K/W
$R_{th(j-c)}$	sin. 180; per thyristor / per module	0,19 / 0,095	K/W
$R_{th(j-c)}$	rec. 120; per thyristor / per module	0,21 / 0,105	K/W
$R_{th(c-s)}$	per thyristor / per module	0,1 / 0,05	K/W
T_{vj}		- 40 ... + 125	°C
T_{stg}		- 40 ... + 125	°C
V_{isol}	a. c. 50 Hz; r.m.s.; 1 s / 1 min.	3600 / 3000	V~
M_s	to heatsink	5 ± 15 %[1)]	Nm
M_t	to terminal	5 ± 15 %	Nm
a		5 * 9,81	m/s^2
m	approx.	165	g
Case	SKKT	A 21	
	SKKH	A 22	

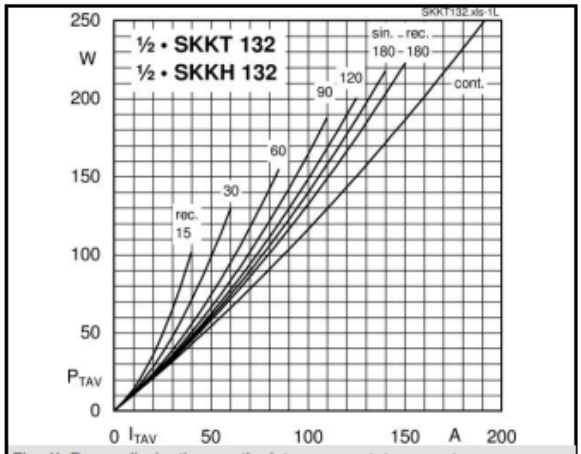


Fig. 1L Power dissipation per thyristor vs. on-state current

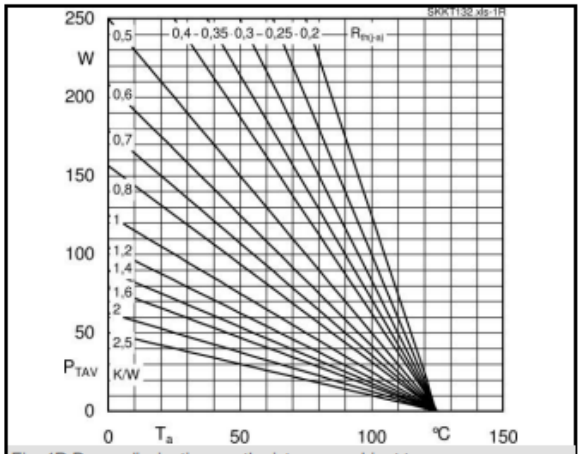


Fig. 1R Power dissipation per thyristor vs. ambient temp.

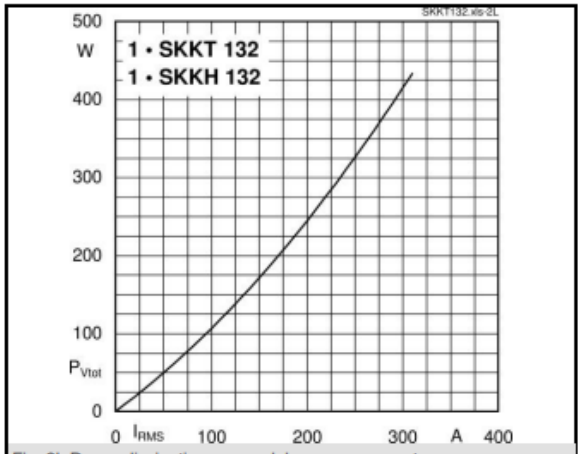


Fig. 2L Power dissipation per module vs. rms current

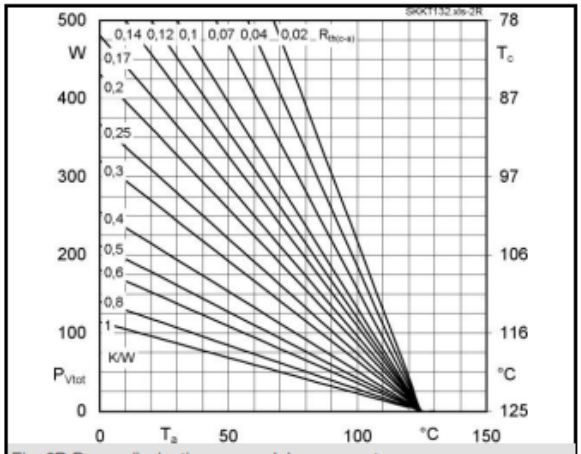


Fig. 2R Power dissipation per module vs. case temp.

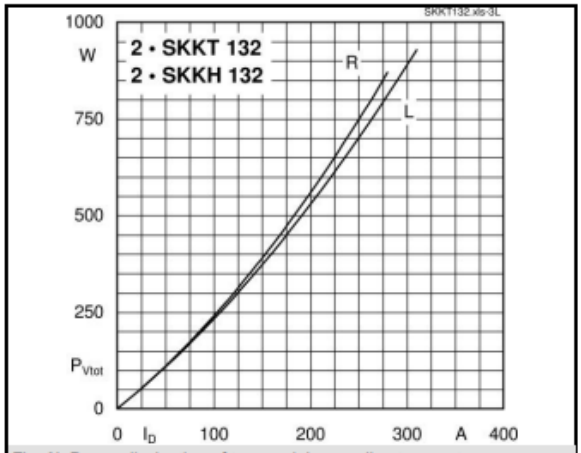


Fig. 3L Power dissipation of two modules vs. direct current

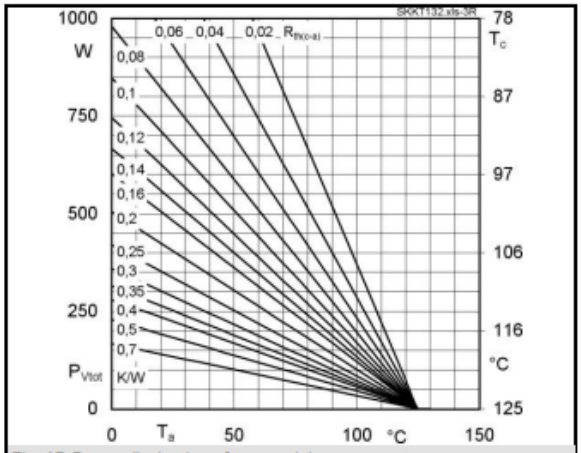


Fig. 3R Power dissipation of two modules vs. case temp.

SKKT 132, SKKH 132

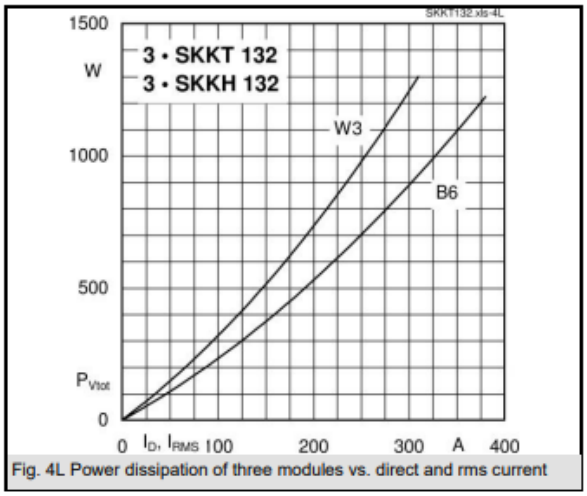


Fig. 4L Power dissipation of three modules vs. direct and rms current

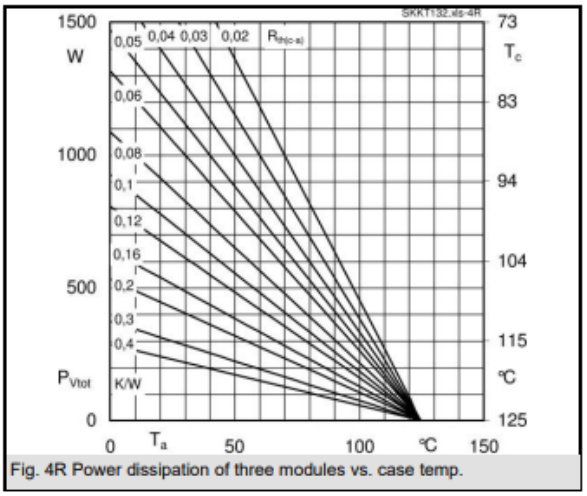


Fig. 4R Power dissipation of three modules vs. case temp.

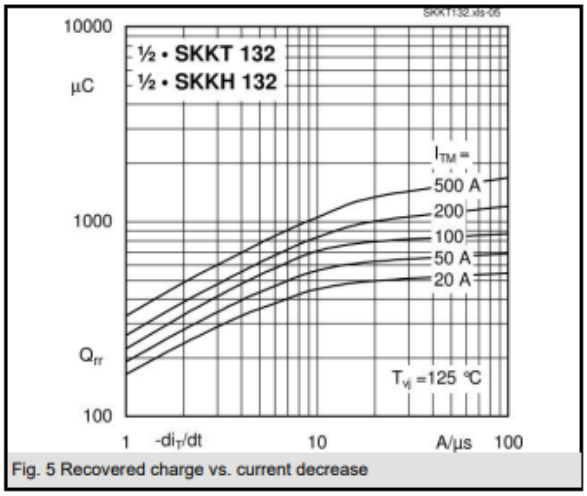


Fig. 5 Recovered charge vs. current decrease

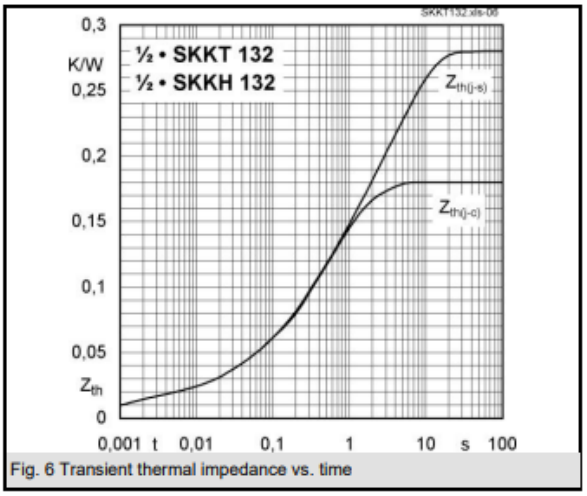


Fig. 6 Transient thermal impedance vs. time

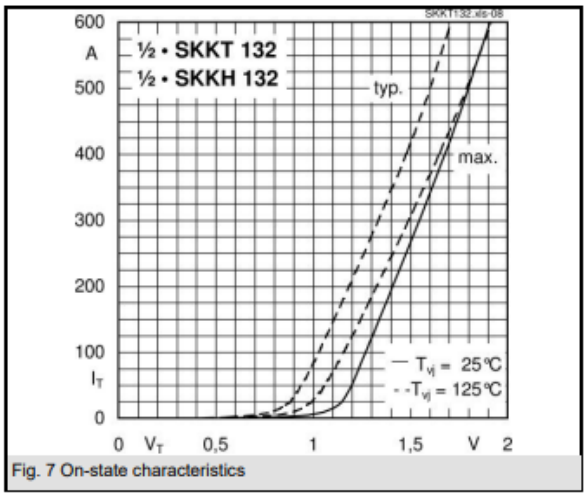


Fig. 7 On-state characteristics

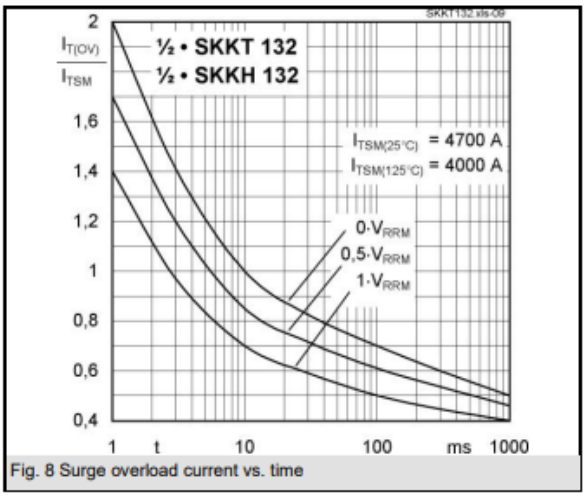


Fig. 8 Surge overload current vs. time

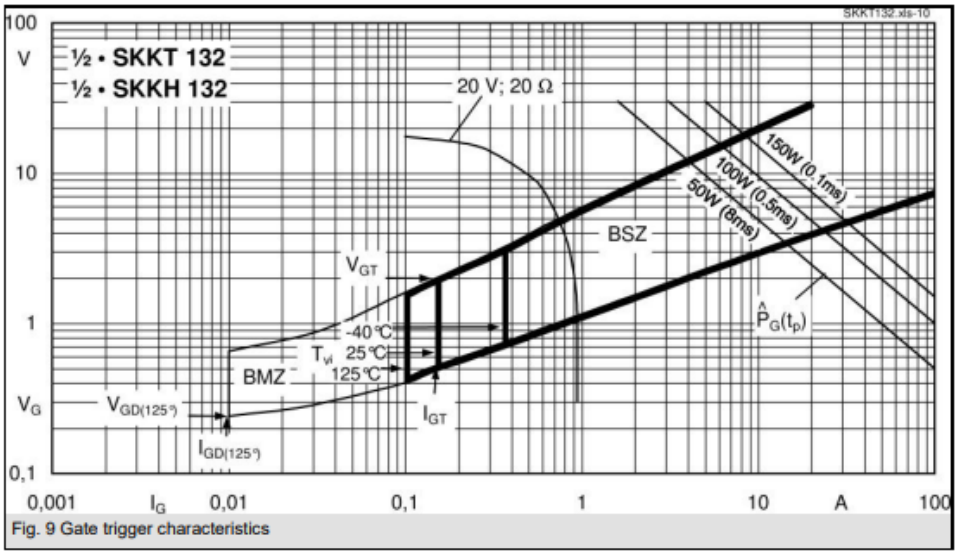
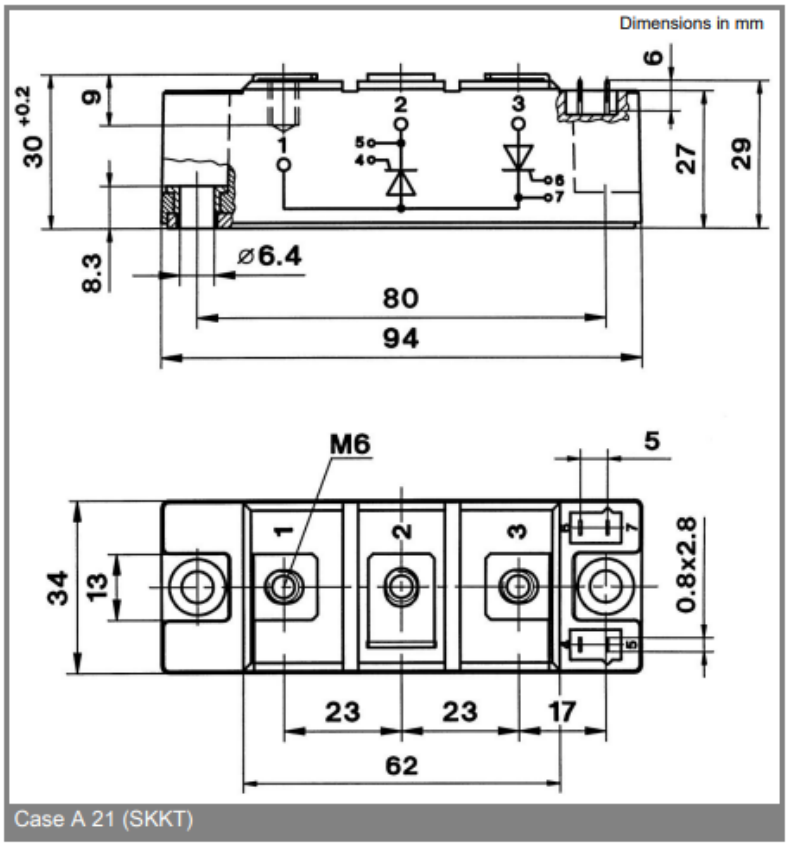
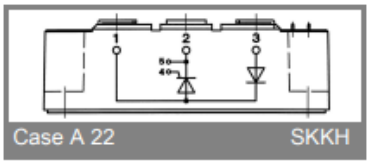


Fig. 9 Gate trigger characteristics



Case A 21 (SKKT)


Case A 22 SKKH

* The specifications of our components may not be considered as an assurance of component characteristics. Components have to be tested for the respective application. Adjustments may be necessary. The use of SEMIKRON

Appendix (C)
Datasheet of SEMICRON FWD type (SKKD 212)

SKKD 212 ...

SEMIPACK® 2

Rectifier Diode Modules

SKKD 212

Features

- Heat transfer through aluminium oxide ceramic isolated metal baseplate
- Hard soldered joints for high reliability

Typical Applications*

- Non-controllable rectifiers for AC/AC converters
- Line rectifiers for transistorized AC motor controllers
- Field supply for DC motors

V_{RSM} V	V_{RRM} V	I_{FRMS} = 340 A (maximum value for continuous operation) I_{FAV} = 212 A (sin. 180; T_c = 85 °C)
1300	1200	SKKD 212/12
1700	1600	SKKD 212/16
1900	1800	SKKD 212/18

Symbol	Conditions	Values	Units
I_{FAV}	sin. 180; T_c = 85 (100) °C	212 (165)	A
I_{FSM}	T_{vj} = 25 °C; 10 ms	6600	A
	T_{vj} = 125 °C; 10 ms	5500	A
i^2t	T_{vj} = 25 °C; 8,3 ... 10 ms	217800	A^2s
	T_{vj} = 125 °C; 8,3 ... 10 ms	151250	A^2s
V_F	T_{vj} = 25 °C; I_F = 500 A	max. 1,4	V
$V_{(TO)}$	T_{vj} = 135 °C	max. 0,75	V
r_T	T_{vj} = 135 °C	max. 1,05	mΩ
I_{RD}	T_{vj} = 135 °C; V_{RD} = V_{RRM}	max. 9	mA
$R_{th(j-c)}$	per diode / per module	0,18 / 0,09	K/W
$R_{th(c-s)}$	per diode / per module	0,1 / 0,05	K/W
T_{vj}		- 40 ... + 135	°C
T_{stg}		- 40 ... + 135	°C
V_{isol}	a. c. 50 Hz; r.m.s.; 1 s / 1 min.	3600 / 3000	V~
M_s	to heatsink	5 ± 15 %	Nm
M_t	to terminals	5 ± 15 %	Nm
a		5 * 9,81	m/s²
m	approx.	165	g
Case	SKKD	A 23	

SKKD

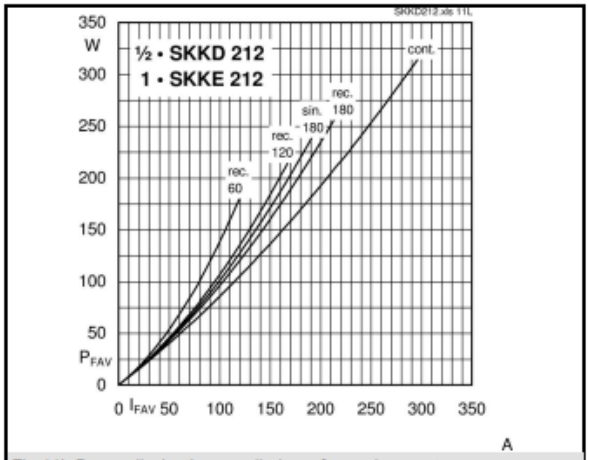


Fig.11L Power dissipation per diode vs.forward current

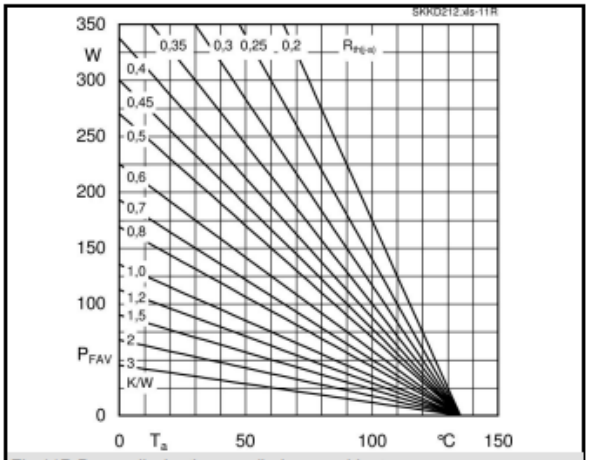


Fig.11R Power dissipation per diode vs.ambient

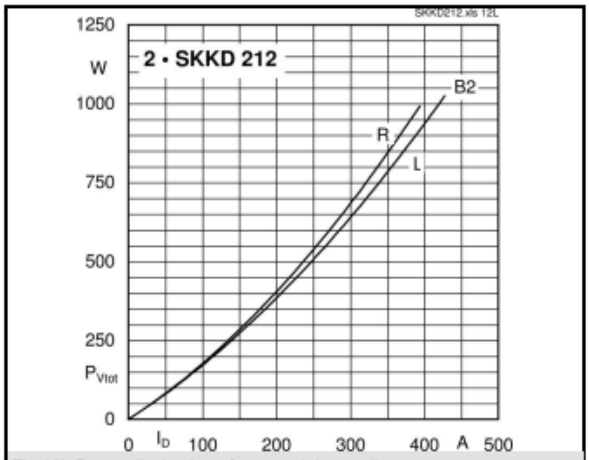


Fig.12L Power dissipation of two modules vs.direct

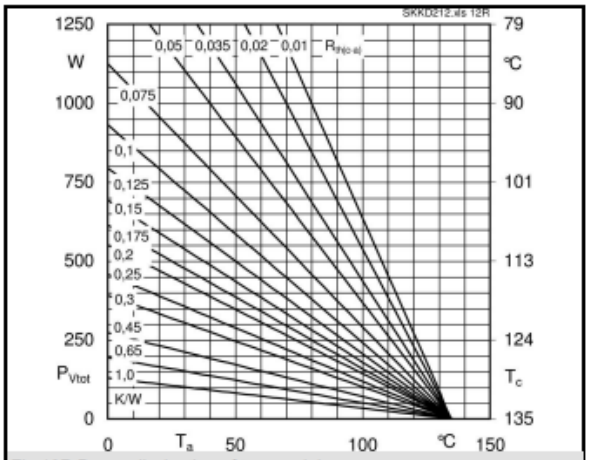


Fig.12R Power dissipation of two modules vs.case

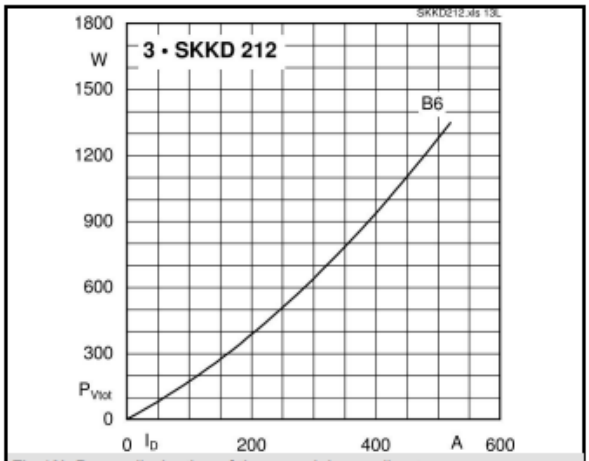


Fig.13L Power dissipation of three modules vs.direct

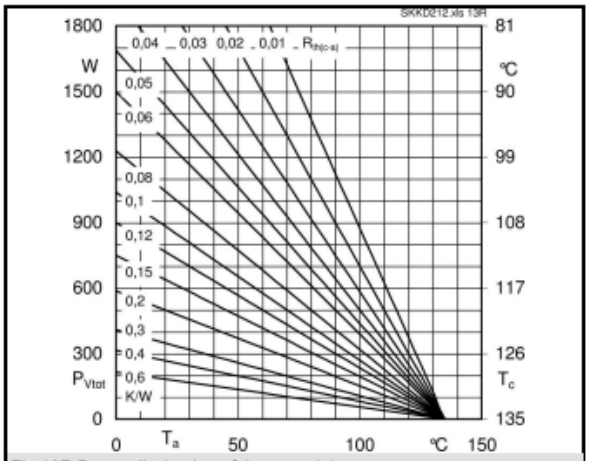


Fig.13R Power dissipation of three modules vs.case

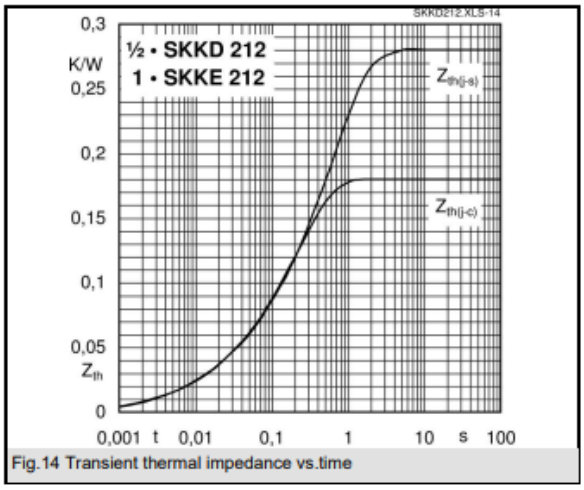


Fig.14 Transient thermal impedance vs.time

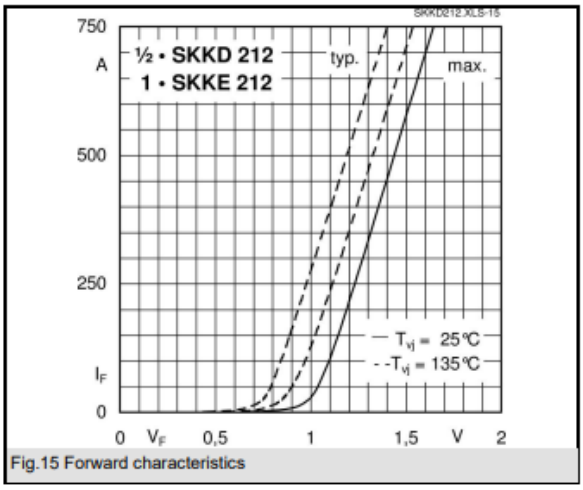


Fig.15 Forward characteristics

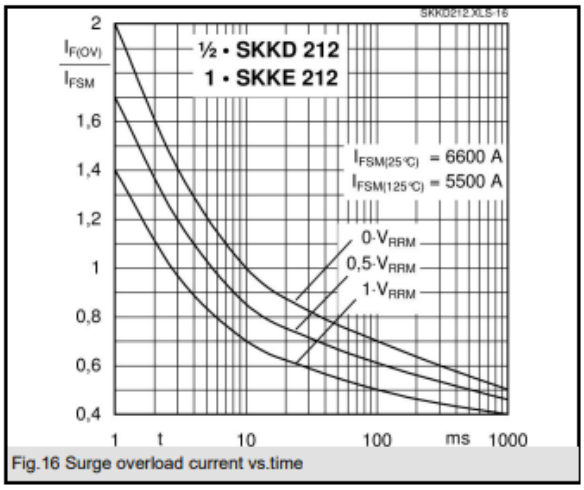


Fig.16 Surge overload current vs.time

Appendix (D)
Datasheet of a phase-locked loop (PLL) IC 4046

CMOS High Voltage Logic – CD4046B

CMOS Micropower Phase Locked Loop (PLL) in bare die form

Rev 1.0
21/09/18

Description

The CD4046B phase locked loop consists of two phase comparators, a voltage-controlled oscillator (VCO), source follower and zener diode. The comparators have a common signal input amplifier and common comparator input. The zener diode is used for power supply regulation if required. Applications include FM and FSK modulation / demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

Features:

- Choice of two Phase Comparators:
  - Exclusive Or Gate, duty cycle limited
  - Rising edge switching, duty cycle unlimited
- Buffered outputs compatible with MHTL and Low power TTL
- VCO inhibit control for ON-OFF keying and ultra-low standby power consumption
- Source-follower output of VCO control input
- Integrated zener diode to assist supply regulation
- Supply voltage range: 3V to 18V
- Symmetrical output characteristics

Ordering Information

The following part suffixes apply:

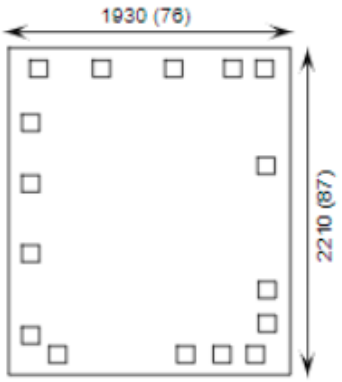
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 635µm(25 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1930 x 2210 76 x 87	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	635 (±20) 25 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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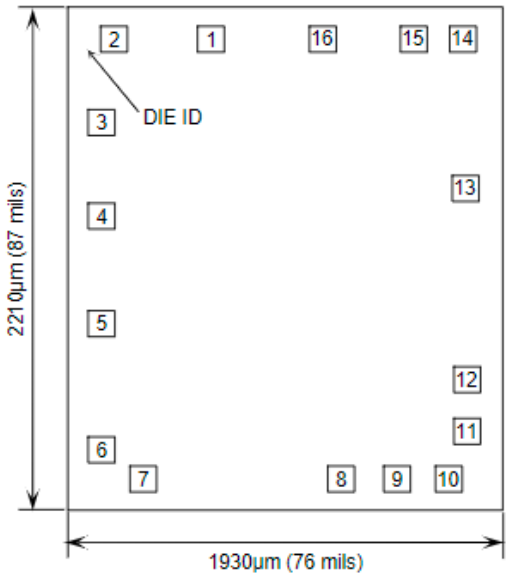
CMOS High Voltage Logic – CD4046B

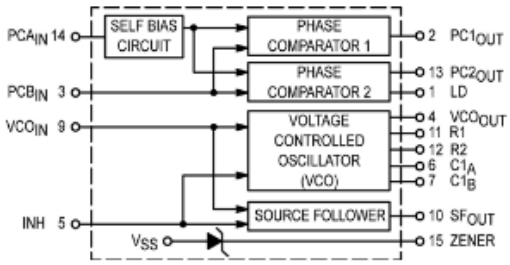
Rev 1.0
21/09/18

Pad Layout and Functions



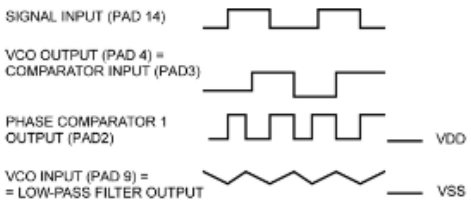
PAD	FUNCTION
1	LD
2	$PC1_{OUT}$
3	PCB_{IN}
4	VCO_{OUT}
5	INH
6	$C1_A$
7	$C1_B$
8	V_{SS}
9	VCO_{IN}
10	SF_{OUT}
11	R1
12	R2
13	$PC2_{OUT}$
14	PCA_{IN}
15	ZENER
16	V_{DD}
CONNECT CHIP BACK TO V_{DD} OR FLOAT	

Block Diagram



Pad 1 = V_{DD}
Pad 8 = V_{SS}

PLL Waveforms



Typical waveforms for CMOS PLL with phase comparator in locked condition of f_{osc}

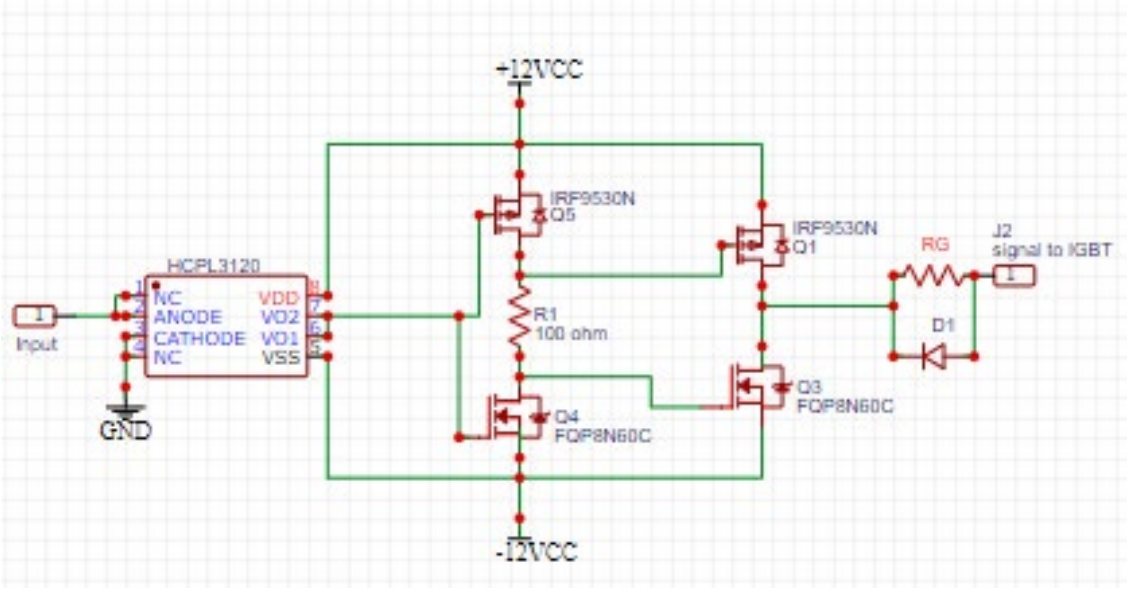
Appendix (E)

The IGBT's Driving Circuits

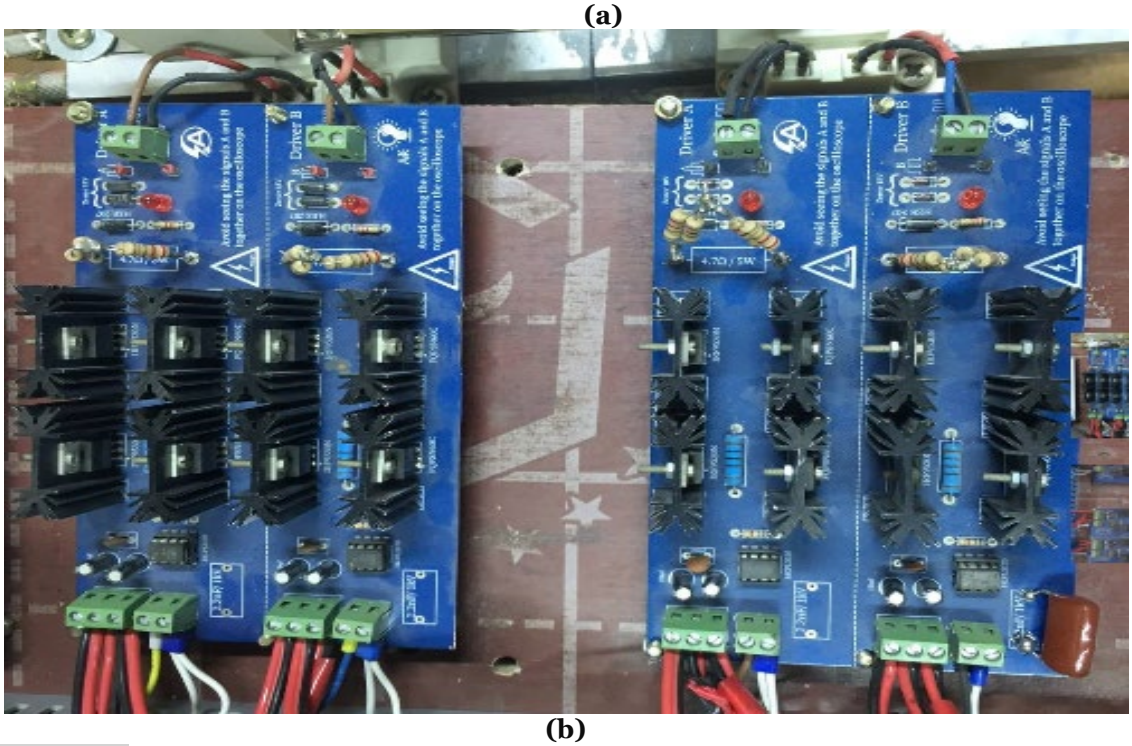
The type of IGBT for CFI is **SKM300GBD12T4,**

When driving the gate of a high-power transistor, such as an IGBT or power MOSFET, a power amplifier serves as the gate driver. It receives its high-current drive input from a controller integrated cct. (IC's) low-power input.

Figure (E-1) illustrates the isolation of the four driving circuits. Each one provides +12 and -12 volts that can be used to power an IGBT in the inverter.



(a)



(b)

Figure (E-1) (a) The circuit diagram of the gate driver (b) The implemented circuit of the gate driver.

The water-cooled heat sink shown in Figure (E-2) was used to absorb the excessive heat stresses on the IGBT and the MOSFET during the heating process.

Figure (E-2) The Water-Cooled Heat Sink.

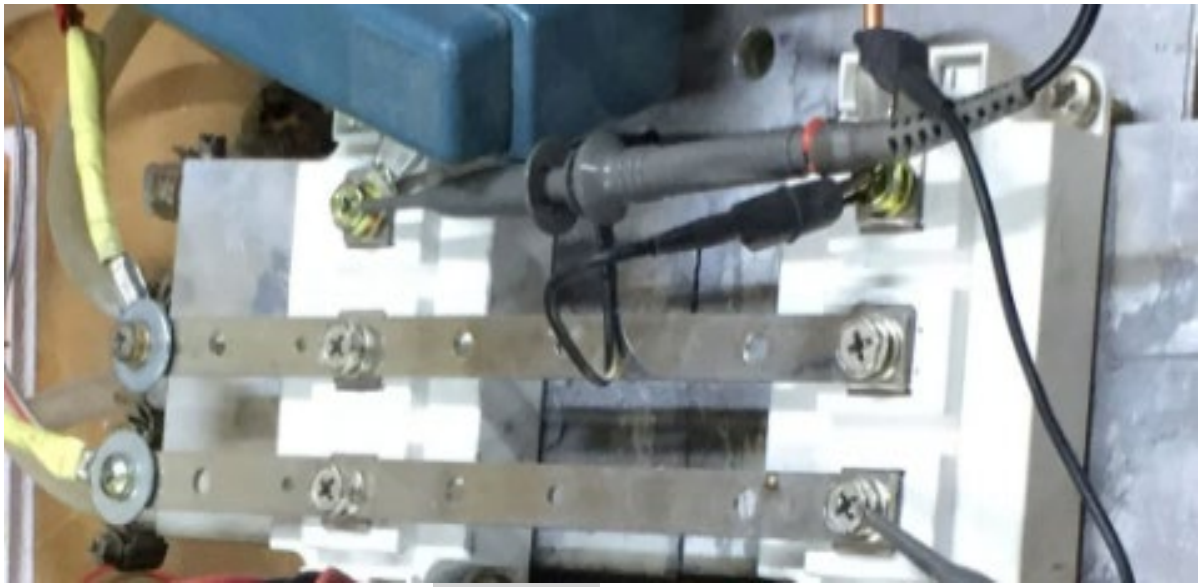


Figure (E-3) IGBT for CFI.