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A Comparative Study of Total Harmonic Distortion betweenTwo Topologies 27- and 31 Multi Level Inverter

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ABSTRACT

In recent times, Multilevel inverters are considered an essential component of power electronics with widespread use in a wide range of high-voltage and high-power industrial and commercial applications. The use of multi-level inverters, also known as MLIs, has been preferred over conventional inverters due to the characteristics that these MLIs possess. These characteristics include low harmonic distortion caused by satisfacory performance of MLIs. This paper is concerned with analyzing harmonics to gain a deeper understanding of the performance of cascaded H-Bridge multilevel inverters (CHB-MLI). The model was constructed by using MATLAB/SIMULINK. A comparison was made between an asymmetrical cascaded 27 and 31-level multi-level inverter (MLI) by using the Phase disposition sinusoidal Pulse Width Modulation (PD-SPWM)and Phase Opposition Disposition sinusoidal Pulse Width Modulation (POD-SPWM) techniques. According to the outcomes of the simulations, 31 levels are better than 27 where Total Harmonic Distortion (THD) in 31 levels is lower than 27 levels. The best result obtained during this study is 31 levels that use (PD-SPWM) technology, where the percentage of total harmonic distortion is small compared to the rest of the results and equal to 3.63%.

Keywords:

Multilevel inverter, phase disposition sinusoidal Pulse Width Modulation (PD-SPWM) , Total Harmonic Distortion, Phase Opposition Disposition sinusoidal Pulse Width Modulation (POD-SPWM) Asymmetrical multi-level inverter (AML).

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1. INTRODUCTION

Multi-level inverters have a greater number of benefits when compared to conventional two-level inverters [1,2], multilevel inverters have gained popularity in high power, and medium voltage applications because they may be used without a transformer and with less noise and harmonic distortion.

The primary benefits of multilevel inverters (MLIs) include lower total harmonic distortion (THD) in output voltage because of the many levels of the waveform, lower switching frequency which results in lower switching losses, the use of switches with lower voltage ratings to achieve higher output voltage. In addition, DV/DT stress is being little, which leads to a reduction in electromagnetic coupling [3,5].

Increasing the number of levels results in the formation of a very fine ladder state wave that is closer to the intended sine wave, and as a result, the total harmonic distortion (THD) reduces [4]. . multi-level inverters are divided into three types: 1) diode clamped 2) flying capacitors, 3) cascade H -bridge [6,7]. It has been determined that the H-Bridge cascade inverter is the most suitable option for both the grid and photovoltaic systems (CHB-MLI) [5]. The H-shaped cascading multilevel inverter is created with fewer components and is designed to bridge quickly when compared to other multi-level inverters. Figure 1 illustrates types of MLI. Figure 1(a)

shows a three-level diode clamped, and Figure 1 (b) shows a three-level flying capacitor.

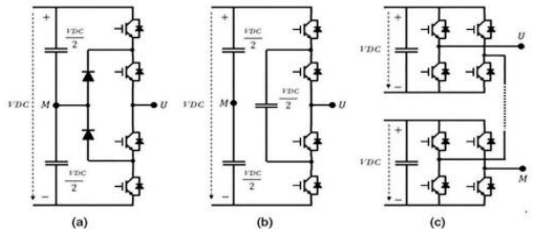


Fig.1 One leg of multi-level inverter topology

Figure(1,c), shows the structure Cascaded H-bridge inverter in which each cell is separated from the others and feeds these separated cells from several different DC sources[9].

In addition, each cell generates three different voltage levels (VDC, 0,-VDC) .In comparison to other kinds of inverters,the Cascaded Bridge multi-level inverter is distinguished by its high level of dependability as well as its user-friendly control [10]. Cascaded H-bridge MLI includes two types: symmetric and asymmetric. If voltage sources are equal, the CHB is symmetrical MLI. And the level of the output voltage can be determined in this case by applying the following equation:

$$m = 2n+1$$

where n: denotes the total number of H-bridges

m: indicates the total number of levels.

If dc-sources are different, the CHB is asymmetrical. The major advantage of the asymmetric CHB topology is that it can considerably increase the number of output voltage levels by using few dc voltage sources and IGBTs or MOSFETs.While symmetric Cascaded MLI, the voltage is the same in every cell and the voltage increases by increasing the number of cells. In this paper , a basic 27 and 31 single-phase asymmetric multilevel inverters are discussed.

Table (1) shows the comparison between three types of MLI topologies [19].

Table 1: comparison of topologies

S.N	Characteristics	Cascaded H-Bridge	Bridge Diode Clamped	Flying Capacitor
1	Main switching device	2(m-1)	2(m-1)	2(m-1)
2	Main Diodes	2(m-1)	2(m-1)	2(m-1)
3	Clamping Diodes	0	(m-1)(m-2)	0
4	DC bus capacitor	(m-1)/2	(m-1)	(m-1)
5	Balancing Capacitor	0	0	(m-1)(m-2)/2
6	Redundancy	Redundant	Not Redundant	Redundant
7	DC Bus Sharing	Separate DC	DC Bus Sharing	DC Bus Sharing
8	Structure	Modular	Not Modular	Not Modular
9	Flexibility	Flexible	Not Flexible	Not Flexible

Modulation Technique

Multi-Carrier modulation PWM includes two methods that are commonly used and can be categorized as:

1. Phase shift multicarrier Modulations

In this technique, multi-carrier waves and one sine wave will be needed [12]. In general, for a multi-level inverter with n level, the number of triangular waves is required (n-1), Where n represents the number of cells in each phase. All triangular carriers in the Phase shift have the same frequency and peak-to-peak amplitude but they show phase shift, as shown in figure 2 [16,13].

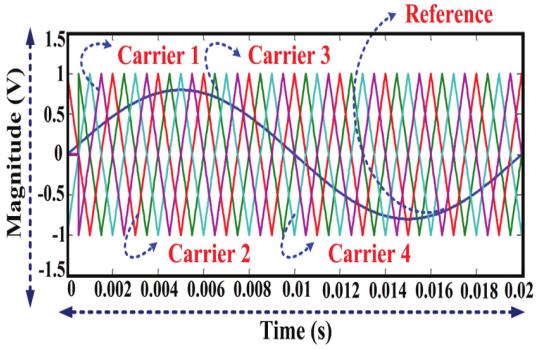


Fig. 2 PhaseShift –PWM

2. Level –shifted Multicarrier Modulation

An m-level CHB inverter employing a level-shifted multi-carrier modulation technique, similar to phase-shifted modulation, requires (m – 1) triangular carriers with the same frequency and amplitude but doesn't have a phase shift. This type is divided into three techniques:

•Alternative Phase Opposite DispositionModulation: Through a (figure 3.a), we notice that in this type, each triangular wave is the opposite of the next wave [17,18].

• Phase Opposition Disposition: In this type of level shift technique, the lower waves are opposite to the upper waves, that is, the waves above zero are in the same phase, and the lower waves that are below zero are in the same phase as shown in (figure 3.b)

• Phase disposition: in this technique, all carriers are in phase [18], demonstrated in (figure 3.c)

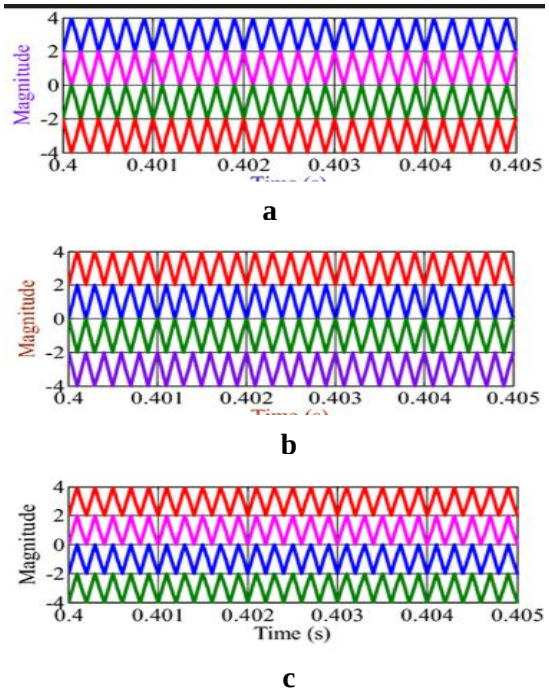


Figure3. LS-PWM carrier arrangements: a) PD, b) POD, c) APOD

MULTILEVEL INVERTER TOPOLOGIES

1.Basic twenty seven Cascaded H-bridge asymtric Multilevel inverter

The basic configuration of a 27-level Cascaded H-bridge Multi-Level Inverter is illustrated in figure(4). The proposed DC-AC cascaded H-bridge multilevel inverter's topology. where The inverter uses three H bridges with three unequal DC sources, and the values of sources are in the following ratios:1VDC:3VDC:9VDC. This structure can only produce twenty-seven levels with a range from+13 to -13 including zero voltage, Table.2 illustrates switching cases in the 27-levels to create different voltages between +13 and -13.

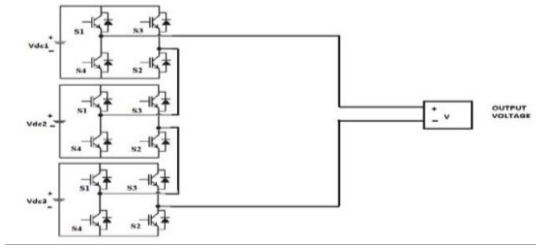


Fig 4. 27 level Cascaded H-Bridge Multilevel inverter

Vo	Switches in Cascaded H-Bridge 27 level MLI											
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
+13 V	1	1	0	0	1	1	0	0	1	1	0	0
+12 V	1	0	1	0	1	1	0	0	1	1	0	0
+11 V	0	0	1	1	1	1	0	0	1	1	0	0
+10 V	1	1	0	0	1	0	1	0	1	1	0	0
+9 V	1	0	1	0	1	0	1	0	1	1	0	0
+8 V	0	0	1	1	1	0	1	0	1	1	0	0
+7 V	0	0	1	1	0	0	1	1	1	1	0	0
+6 V	1	0	1	0	0	0	1	1	1	1	0	0
+5 V	0	0	1	1	0	0	1	1	1	1	0	0
+4 V	1	1	0	0	1	1	0	0	1	0	1	0
+3 V	1	0	1	0	1	1	0	0	1	0	1	0
+2 V	0	0	1	1	1	1	0	0	1	0	1	0
+V	1	1	0	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	1	0
-V	0	0	1	1	1	0	1	0	1	0	1	0
-2V	1	1	0	0	0	0	1	1	1	0	1	0
-3V	1	0	1	0	0	0	1	1	1	0	1	0
-4V	0	0	1	1	0	0	1	1	1	0	1	0
-5V	1	1	0	0	1	1	0	0	0	0	1	1
-6V	1	0	1	0	1	1	0	0	0	0	1	1
-7V	1	1	0	0	1	1	0	0	0	0	1	1
-8V	1	1	0	0	1	0	1	0	0	0	1	1
-9V	1	0	1	0	1	0	1	0	0	0	1	1
-10 V	0	0	1	1	1	0	1	0	0	0	1	1
-11 V	1	1	0	0	0	0	1	1	0	0	1	1
-12 V	1	0	1	0	0	0	1	1	0	0	1	1
-13 V	0	0	1	1	0	0	1	1	0	0	1	1

Table 2: swtiching states of 27 CHBMLI combinations that generate the required Twenty Seven level output signals

2.Basic 31 Cascaded H-bridge asymtric Multilevel inverter

The 31-level cascaded Multilevel inverter circuit is seen in figure 5, which contains 16 switches with four different DC source voltages, and which must be in the following ratios:1VDC:2VDC:4VDC:8VDC. This circuit can generate up to 31 levels of output voltage, range of output voltages between +15 and -15 including zero voltage level.

Table (3) shows the appropriate Switching states and terminal output voltages of a 31-level Cascaded H-bridge Multi-level inverter.

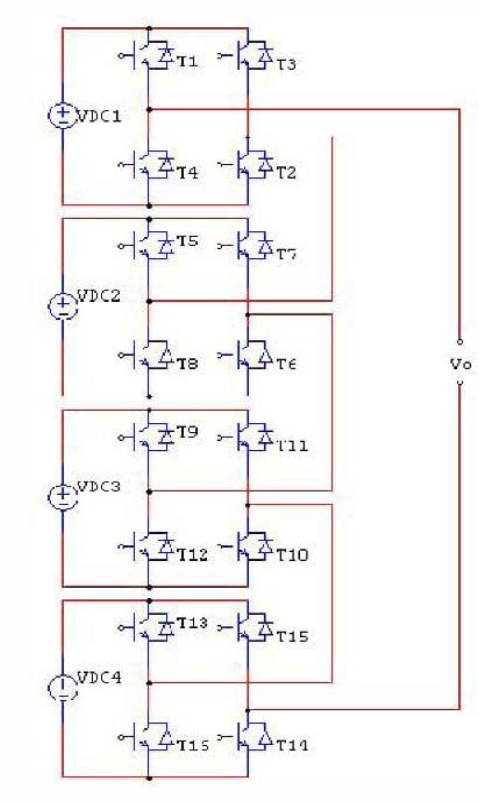


fig.5. 31 Level Cascaded H-Bridge MLI

Table 3: Switching States and Terminal Voltage of 31 Level Cascaded H-Bridge

T16	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	VO
0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	15
0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	1	14
0	0	1	1	0	0	1	1	0	1	0	1	0	0	1	1	13
0	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1	12
0	0	1	1	0	1	0	1	0	0	1	1	0	0	1	1	11
0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	10
0	0	1	1	0	1	0	1	0	1	0	1	0	0	1	1	9
0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	8
0	0	1	1	0	1	0	1	0	1	0	1	1	1	0	0	7
0	1	0	1	0	0	1	1	0	0	1	1	0	1	0	1	6
0	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	5
0	1	0	1	0	0	1	1	0	1	0	1	0	1	0	1	4
0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	1	3
0	1	0	1	0	1	0	1	0	0	1	1	0	1	0	1	2
0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	1	1	1	0	0	-1
0	1	0	1	0	1	0	1	1	1	0	0	0	1	0	1	-2
0	1	0	1	0	1	0	1	1	1	0	0	1	1	0	0	-3
0	1	0	1	1	1	0	0	0	1	0	1	0	1	0	1	-4
0	1	0	1	1	1	0	0	0	1	0	1	1	1	0	0	-5
0	1	0	1	1	1	0	0	1	1	0	0	0	1	0	1	-6
0	1	0	0	0	1	0	1	0	1	0	1	0	0	1	1	-7
1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	-8
1	1	0	0	0	1	0	1	0	1	0	1	1	1	0	0	-9
1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	-10
1	1	0	0	0	1	0	1	1	1	0	0	1	1	0	0	-11
1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1	-12
1	1	0	0	1	1	0	0	0	1	0	1	1	1	0	0	-13
1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	1	-14
1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	-15

Simulation Results

The circuit of the cascading asymmetric multi-level inverter with 31 levels and 27 levels was built based on the MATLAB /Simulink program.

The MATLAB / Simulink model of a 31 Level- Cascaded H - Bridge Inverter is shown in Figure 6.Where Four cells with unequal voltages were used and R value is 100 connected to the output of the inverter. The values of voltages are: VDC1=8, VDC2=16, VDC3=32, and VDC4=64. This model can generate 31 levels only in output voltage as shown in figure(7).

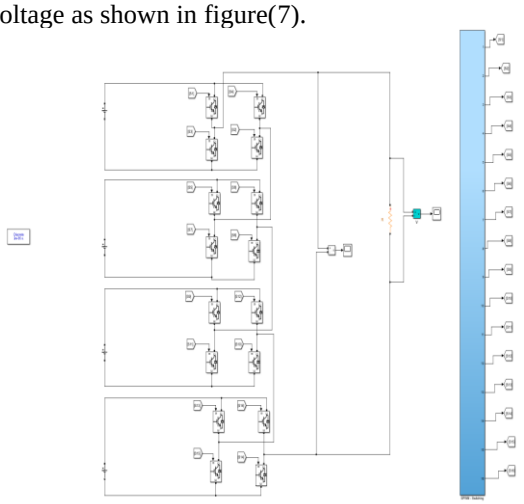


Figure.6 simulation model of 31 Level-Cascaded H-Bridge inverter

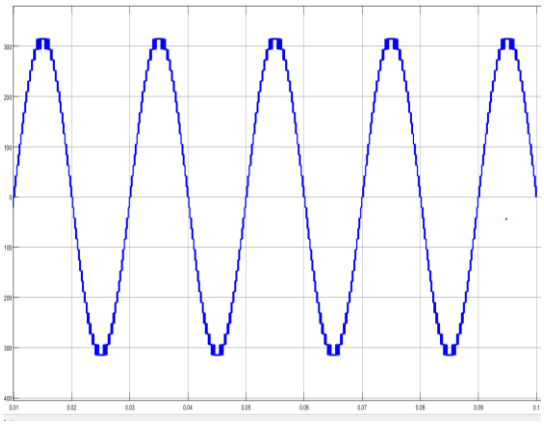


Fig 7.output voltage for 31 levels

phase disposition sinusoidal pulse-width Modulation and phase opposition disposition sinusoidal Pulse Width Modulation techniques were used where the total harmonic content was analyzed by using fast Fourier transform analysis and was the value of THD at use (PD-PWM) as shown in the figure(8), but when using a (POD-PWM) technique, it was a value as shown in the figure(9).

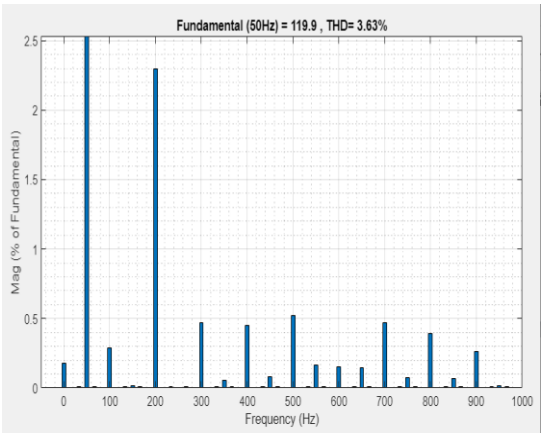


Fig 8.THD in (PD-SPWM) technique for 31 levels

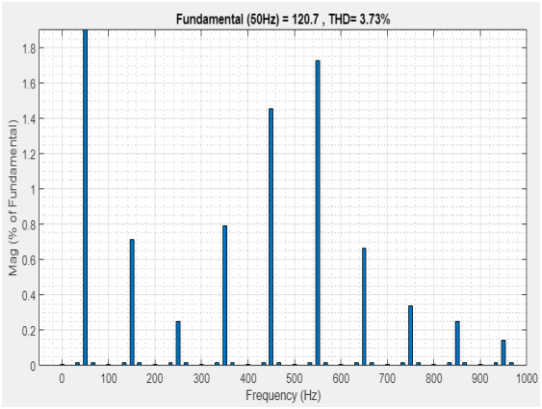


Fig 9.THD in (POD-PWM) technique for 31-level

As for the circuit for 27, three sources of different values were used as well, values were VDC1=8, VDC2=24, and VDC3=72, the output wave contained 27 levels as shown in figure (10).

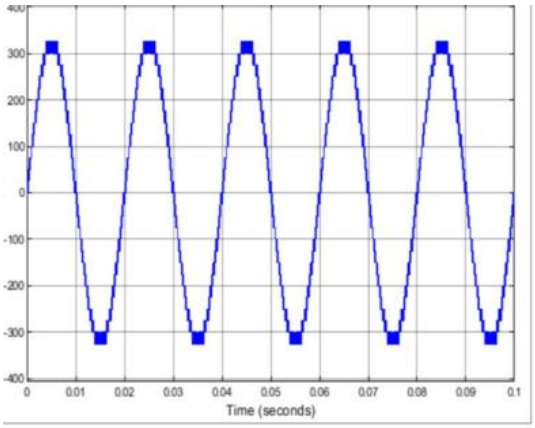
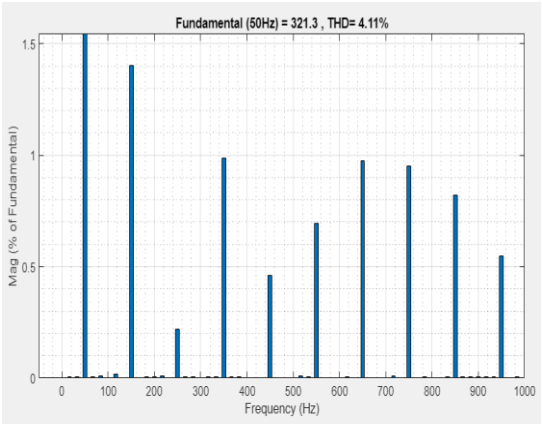
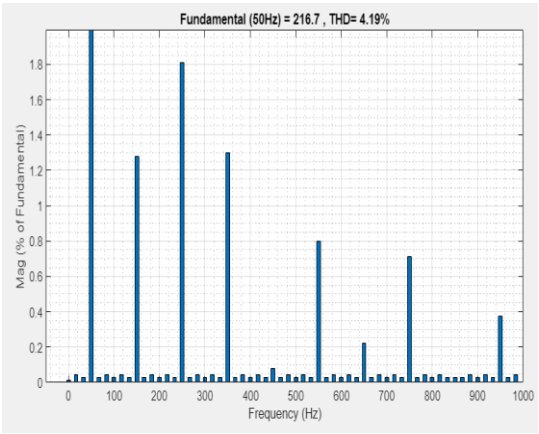


Fig 10. output voltage for 27 levels

This circuit also was analyzed in Matlab using FFT analysis, figure (11) shows the THD ratio when using the (PD-PWM) technique, and figure(12)displays THD when using the (POD-PWM)-technique.



Fig(11).Total Harmonic Distortion in (PD-SPWM)for 27- level



Fig(12).Total Harmonic Distortion in (POD-SPWM)technique for 27- level

Table (4) the comparsion analysis for the 31-level and 27-level under the two different techniques.

Table 4 THD for 27 and 31 levels

Inverter level	No.of switches	THD%	
		PD-SPWM	POD-SPWM
27	12	**4.11**	**4.19**
31	16	**3.63**	**3.73**

Conclusion

This paper presents a THD analysis of 31 CHB-MLI and 27 CHB-MLI. Phase-Shift SPWM and phase-opposition- SPWM techniques were used to compare the performance of the 27-level and 31-level cascading H-bridge topologies. The simulation results show that 31 levels were better than 27-levels using (PD-SPWM) and (POD-SPWM) techniques because 31 levels have lower THD in both techniques. Simulation results also show that THD in 31-levels and 27 levels are lower in (PD-) SPWM) compared to POD-SPWM technology. In addition, by increasing the number of levels, the total harmonic distortion will decrease and the waveform has become closer to the sine wave.

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جدول المختصرات

Altarntive Phase Opposition Disposition	**APOD**
phase disposition	**PD**
Phase Opposition Disposition	**POD**
Cascaded Bridge	**CHB**
Asymmetrical multi-level inverter	**AMLI**
symmetrical multi-level inverter	**SMLI**
Total Harmonic Distortio	**THD**
Multi Level Inverter	**MLI**

دراسة مقارنة للتشوه التوافقي الكلي بين المستويين 27 و 31 لمغيرات متعدد المستويات احادي الطور

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الملخص

تم تفضيل استخدام المحولات متعددة المستويات ، والمعروفة أيضًا باسم MLIs ، على المحولات التقليدية نظرًا للخصائص التي تمتلكها MLIs. تتضمن هذه الخصائص أن التشوه التوافقي الناجم عن MLIs ضئيل للغاية ، وأن أداؤها مرضٍ. لذلك ، ظهرت المحولات متعددة المستويات كعنصر أساسي في إلكترونيات القدرة وتم استخدامها بشكل كبير في مجموعة واسعة من التطبيقات الصناعية والتجارية عالية الجهد وعالية القدرة. الغرض من هذا البحث هو الاستفادة من التحليل التوافقي لاكتساب فهم أعمق لأداء مغيرات القنطري المتعاقب متعددة المستويات (CHB-MLI). حيث تم إنشاء النموذج باستخدام MATLAB / SIMULINK ، وتم إجراء مقارنة بين العاكس متعدد المستويات 27 و 31 مستوى (MLI) باستخدام تقنية تعديل عرض النبض الجيبي لترتيب الطور (PD-SPWM) وتقنية (POD-SPWM). وفقًا لنتائج عمليات المحاكاة ، كان 31 مستوى أفضل من 27 لأن المحتوى التوافقي الكلي ل 31 مستوى أقل من المحتوى التوافقي الكلي ل 27 مستوى ، وأفضل نتيجة تم الحصول عليها خلال هذه الدراسة كانت لـ 31 مستوى في التكنولوجيا (PD-SPWM) ، حيث كانت النسبة المئوية للتشوه التوافقي الكلي صغيراً مقارنة بباقي النتائج ، حيث كانت القيمة تساوي 3.63٪.

الكلمات داله

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