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Dependence of Structural and I-V Characteristic on Annealing Temperature of a-As/c-Si Heterojunction

دراسة تأثير التلدين على الخواص التركيبيه وخواص I-V للمفرق الهجين a-As/c-Si

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Abstract

In this work the effect of annealing temperature on the structure of a-As and electrical properties of a-As/c-Si heterojunction have been studied. The heterojunction fabricated by deposited of a-As film on c-Si using thermal evaporation technique. Electrical properties of a-As/c-Si heterojunction includes I-V characteristic in dark at different annealing temperature and C-V characteristic are considered in the present work.

C-V characteristic show that the fabricated diode was abrupt type , built in potential determined by extrapolation from $1/C^2$-V curve. The built in potential (vb_i) for the a-As/c-Si system was found to be increase from 0.35 to 0.8 V with increasing annealing temperature.

الخلاصة:

في هذا البحث تم دراسة تأثير التلدين على الخواص التركيبية للزرنيخ والخواص الكهربائية للمفرق الهجيني a-As/c-Si الناتج من ترسيب السلنيوم بطريقة التبخير الحراري على السلكون.

الخواص الكهربائية للمفرق الهجين تتضمن خصائص التيار- فولتية في حالة الظلام وبدرجات تلدين ممختلفة وخصائص سعة-فولتية.

من خصائص سعة –فولتية تبين ان المفرق الهجيني هو من النوع الحاد وان جهد البناء تم حسابه من منحني الفولتية ومقلوب مربع السعة وتبين ان جهد البناء للمفرق الهجيني يزداد من 0.3 الى0.8 فولت بزيادة التلدين.

Introduction

The heterojunction device of the amorphous- crystalline semiconductor type have been much attention considerable interest from researchers both from a fundamental physics and technological field ,for example Mimer and Hatenaka 1987 [1] showed that a-Si:H/c-Si has application to imaging devices,Kentaro and Nakazawa 1988;Lovejoy 1992 have also studied amorphous-polycrystalline of silicon films have possible application in a photoelectonics [2] Amorphous arsenic generally, were among the first and most widely investigated amorphous semiconductors[3] , The understanding of the behavior of arsenic in highly doped near surface silicon layers is of crucial importance for the formation of *n* -type ultrashallow junctions in current and future very large scale integrated technology.[4] This is of particular relevance when studying recently developed implantation and annealing methods, The use of arsenic as *n*-type dopant silicon has been Extensively Investigated and applied for the past and present semiconductor technology. Compared to other *n*-type dopants, arsenic offers a relatively high solid solubility and a high mass that gives low penetration depth when the dopant atoms are introduced by ion implantation [5]. In this paper we will present a deposition a-As thin film fabricated by the thermal evaporation technique. The preliminary result of structural and electrical properties of this alloy film have been presented .

Experimental Work

Substrate of p-type single crystal Si wafers with orientation (111) were used in the present study. After scribing these wafers in to small pieces (typically $1cm^2$ in size), with one surface polished with 3ml HNO_3 1ml H_2O for 1-3 minutes and they where dried by using blower and wiped with

soft paper before arsenic deposition [6] The films of a-As were prepared by thermal evaporation under vacuum of the order of 10^{-5} Torr, The rate of deposition was ≈ 2.08 nm/sec onto clean Silicon mirror-like side substrate at room temperature (~300 K). The average thickness of the deposit were determined by microbalance method The maximum error in the determinate of thickness was of the order of10% estimated for the thinnest films(As/Si films of thickness 500 nm). Ohmic contact of Al study on the electrical properties a-As/c-Si Heterojunction aluminum were. evaporated on the Silicon side and As/Si side

Results And Discussions

1-A X-Ray Diffraction Studies

X-ray diffraction (XRD) studies have been carried out to identify the a-As phase present in the film.Fig.1 show the XRD pattern recorded on a-As film , we can see the degree of crystalline increase with increasing annealing temperature this may be attributed in term filled the vacancy and dangling bonds and the structure become more regular and completed in 3-D in lattice . This is due to the increase of grain size and can be explained by the movement of atoms after annealing to array its selves in different sizes of grains [7]

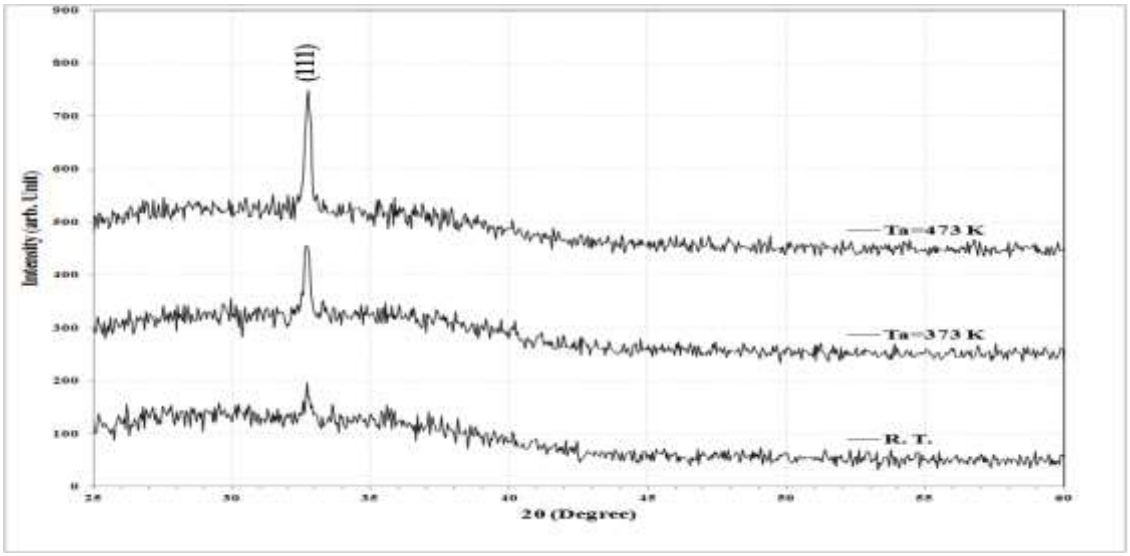

Fig.(1) Effect of annealing temperature on the XRD spectrum for a-As coated glass substrate thin films at different Ta.

1-B Atomic Force Microscopy (AFM) Analysis:

The morphological characteristics of a-As thin films have been studied by using Atomic Force Microscope (AFM) to observe nanostructure. Fig.2(a-b-c) shows the surface topographical images recorded for a-As thin films grown by thermal evaporation technique on glass substrate. AFM images of the films reveal a structure with dense grains, crystalline structure and clear grain boundaries which became apparent at annealing T_a (373 and 473) K. From this figure we can see the variation in crystal structure and increase in grain size with increasing annealing temperature and decrease the grain boundary this result confirm the XRD analysis for same films which indicate the increase the degree of crystallinty with increase $\mathbf{T_a}$ similar result have been observed by ref. [8]. The variation of grain size with $\mathbf{T_a}$ are listed in table below:

Table (1) the value of the roughness average at different $\mathbf{T_a}$

T_a K	Roughness average (nm)
RT	18.3
373	37.3
473	41.6

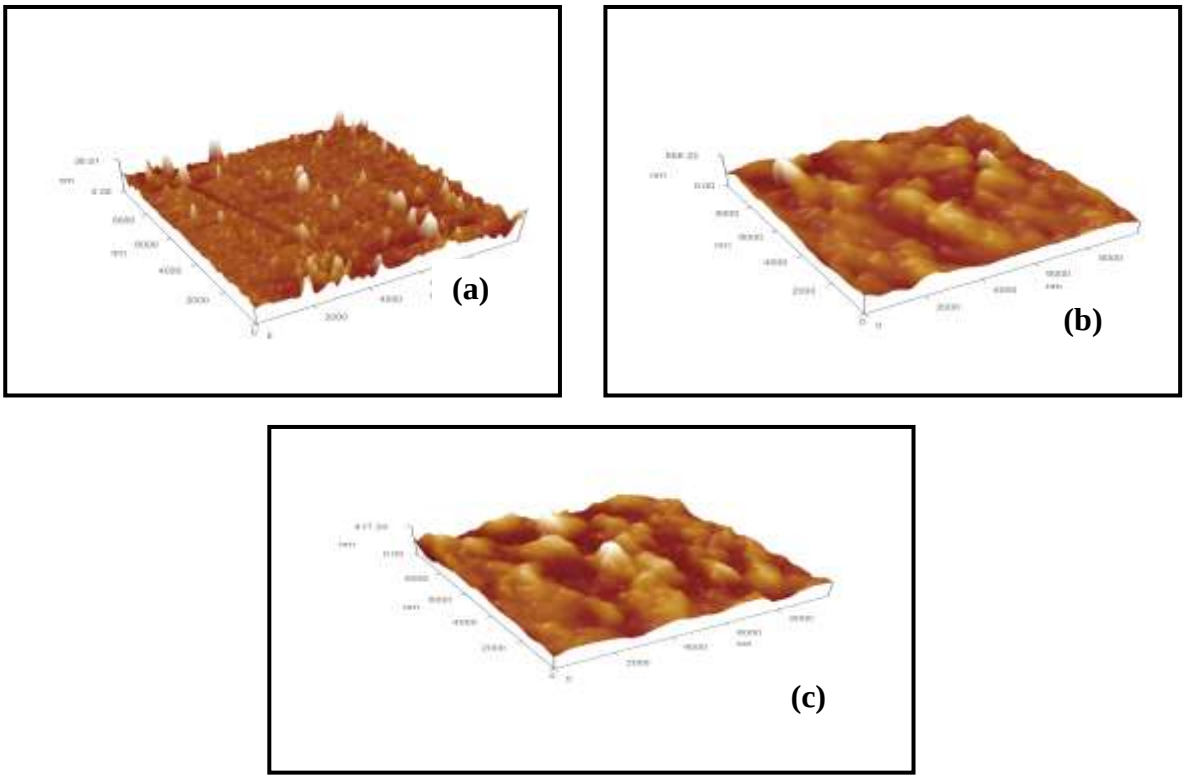

Fig. (2) Effect annealing on the structure of a-As thin films at (500nm):(a) as deposited (300K) (b) annealing (373K)(c) annealing (473 K)

2-I-V characteristics

The (I-V) characteristic shown in fig.(3).This illustrated in dark, for forward and reverse bias of n-As/p-Si heterojunction that the current increases slightly with increasing of annealing temperature because the increasing of temperatures causes a rearrangement of the interface atoms and reduce the dangling bond, surface states and dislocation at interface layer between a-As and c-Si which leads to improvement of the junction characteristics.

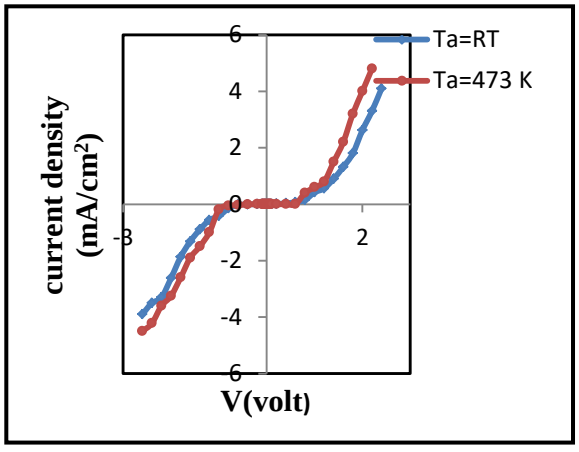

Fig.(3)I-V characterisitics in the dark for n-As/p-Si heterojunction at different annealing temperture

The ideality factors of general p-n junction diodes have been presented with values of (1-3) , under room temperature, The ideality factor is an important parameter for device performance , The mechanism of transport current is estimated from the value of ideality factor (n) where the saturation current can be calculated from intercepting the straight line with the current axis at zero voltage bias.

3. C-V Characteristic

The junction capacitance measured as a function of bias voltage for the n-As/p-Si diodes shows C∝V-1/2 dependence .Fig.(4) which indicates an abrupt junction in that case. According to the distances during which the transition from one region to other is completed near the interface. Under these conditions, the C-V characteristics of the heterojunction can be explained on the basis of Anderson,s model [9], according to which

$$\frac{C}{A}=\left[\frac{q\varepsilon_n\varepsilon_p\mu_n\mu_p}{2(\varepsilon_n N_n+\varepsilon_p N_{p)}}\right]^{1/2}(V_D-V)^{-1/2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(1)$$

Where *Nn* and *Np* are the donor and acceptor concentrations respectively, and ε_n and ε_p are the dielectric constant of n and p-type semiconductor respectively, V_D is the built-in junction potential, V is the applied voltage, and A is the area of the junction. It is interesting to note from this expression that a plot of C-2 against applied voltage is linear and its extrapolated intercept on the voltage axis gives the built-in junction potential, Value of V_D estimated from $1/C^2$ versus V polt that obtained for heterojunction that built-in potential (Vb_i) for the n-As/p-Si system was found to be increase with increasing of annealing temperature this result are agreement with ref.[10]

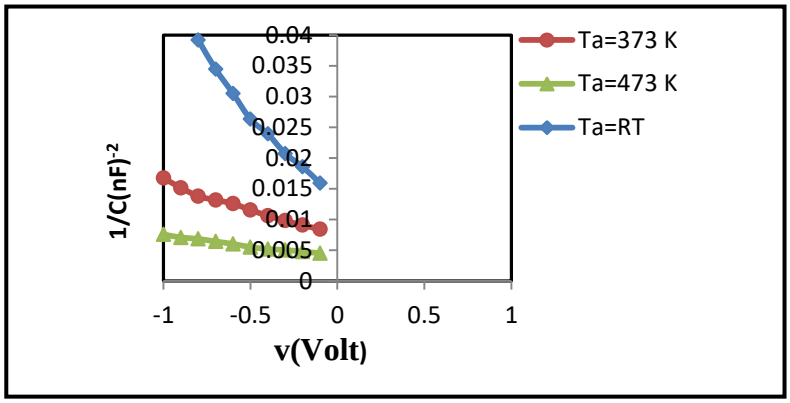

Fig.(4): $1/C^2$ as a function of reverse bias voltage and at different annealin temperature

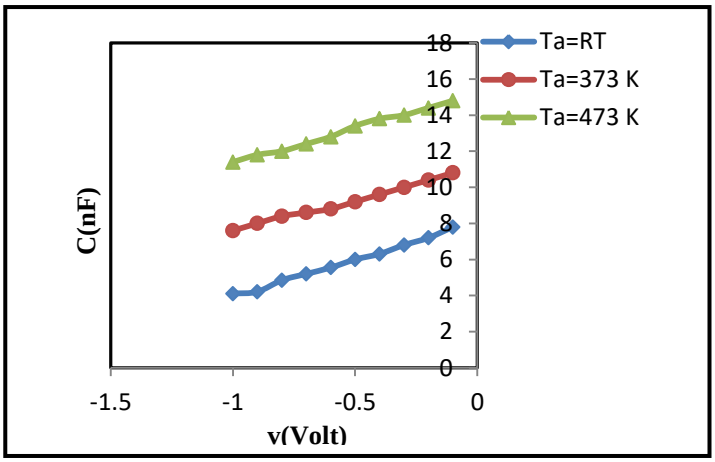

Fig.(5) The variation capacitance with voltage for a-As/c-Si heterojunction at different annealin temperature

Table(2) Values of (V_{bi}) for As/ Si heterojunction withdifferent annealin temperature

Annealing temp.(K)	Vbi(V)
R.T	0.35
373	0.61
473	0.80

Conclusion

From what has been mentioned above, We can conclude that this type of n-As/p-Si heterojunction that the current increases slightly with increasing of annealing temperature The junction is abrupt type the built-in potential (V_{bi}) for the n-As/p-Si System was found to be increasing with increasing of annealing temperature.

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