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Improved Y-Source Single-Stage Transformerless Micro-Inverter for PV Residential Applications

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K E Y W O R D S

Impedance source network, Y-source network, transformerless micro-inverter, leakage current, leakage inductance.

A B S T R A C T

Y-Source Impedance Network (YSN) is one of the most suitable for providing high voltage gain. It generatesa high voltage gain by using a small shoot-through duty cycle, which makes it suitable in applications require a wide range of input voltages such as the Photovoltaic (PV) power plants. However, traditional (YSNs) are unable to boost low voltages in certain applications to the DC-link voltage (about 400V) since it requires a high number of the turns ratio. Higher turns ratio implies higher leakage inductance resulting in higher DC-link voltage spikes. Also, traditional YSNs have high voltage stresses across the components. In this paper, a developed new transformerless Micro-Inverter (MI) is presented that can overcome all the aforementioned drawbacks. The proposed MI has been developed and designed to eliminate both the leakage inductance due to three-winding coupled transformer and leakage current due to using transformerless MI configuration. In addition, the proposed MI reduced the components' stress significantly and increases the converter voltage gain capability in one single-stage. The proposed high boost ratio transformerless MI is analyzed through the PLECS software simulator and implemented in a small scale MI prototype to ensure the results agree with the analysis and simulation results.

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1. Introduction

One of the priorities in recent years is the development of alternative sources to generate electricity particularly from renewable sources, which produce low levels of environmental contamination. These renewable sources play an important role in the long term and can bring significant changes to the global energy system. Solar energy is the most available source of renewable energy [1]. Solar panels are used to convert Sun energy into electricity-producing direct current (DC).

The inverter plays a key role in the PV system which is converting direct current (DC) into alternating current (AC) needed in the electricity grid [2]. Inverters can be classified as a central inverter, sting-inverter, and MI. The MI offers the benefit of high power expansion, reduced shading, easy monitoring and, easy installation. It attracted a lot of attention to the development of PV systems [3 and 4].
The line-frequency or high-frequency transformer is generally used for PV grid-connected MI in order to increase the voltage and provide galvanic isolation between the grid and the PV panel. However, a line-frequency transformer reduces the efficiency of the PV grid system and increases costs and volumes. Also, the high-frequency transformer and DC-DC switches cause additional loss of power. Consequently, the interest in transformerless single-stage MI topologies is increasing.[٥]
Impedance network developments provide an efficient means of converting power and offer a wide range of voltage gains. In addition, new improvements have also been made to the basic network with coupled magnetics to increase the voltage while using a small shoot-through duty cycle [6]. These include switched inductor Z-source [7], embedded Z-source [8], extend Z-source [9]. However, the output voltage range can be extended only by adding a number of stages of the impedance network, which results in increasing inverter volume and cost and reducing inverter efficiency. By introducing coupled magnetic winding instead of an inductor, different boost factor can be achieved. For instance, Trans-Z-source inverter. [10], Γ-Z-source inverter [11] and T-source inverter [12]. A high step-up YSI [13], which suggested a new configuration to provide a high voltage gain ensured by recycling of the leakage energy. Recently, a Modified Y-Source Inverter (M-YSI) has been proposed [5], the configuration consists of two capacitors, diode, input inductor L_{in}, and a three-winding coupled inductor (N_1, N_2, and N_3). The three coupling inductor and shoot-through duty cycle, enabling it to be utilized in a wide range of input voltage (solar module). However, it has some common drawbacks, such as (i) a higher number of turns ratio required to achieve high voltage gain. Higher turns ratio implied higher leakage inductance result in higher DC-link voltage spikes and power losses. (ii) High voltage stresses across the components. (iii) Leakage current due to the absence of galvanic isolation. Hence, to overcome all drawback mention above the contributions of this work is summarized in the points below:

1. Designing a new impedance source based on three coupling winding configuration. The output voltage gain of the proposed configuration is twice higher than that of the improved YSI [5]. Hence, less number of turn ratios are required, which consequently reduce the leakage inductance.
2. Reducing the voltage stress of the proposed MI on the diode D_1 by (1/K). The voltage stress equals to the voltage attained at the DC-link voltage. On the contrary, the voltage stress on the diode D_1 is equal to DC-link voltage multiplies by K of traditional YSN. It means that the diode voltage stress of the traditional YSN affected by the number of winding factors (K), as (K) increases the voltage stress also increases. While the voltage stress of the proposed MI on diode D_1 is constant and equal to the DC-link voltage.
3. The diode (D_2) acts as a clamping diode, which is used to limit the voltage spike generated on the switches caused by the leakage inductance that may in turn cause current distortion, EMI, and additional system losses. This active clamping feature is very necessary with the use of cheap ferrite core such as the one proposed in this work. Hence, there is no need for restriction when using expensive cores such as the MP cores.
4. By connecting the negative pole of the PV module directly to the neutral line of the grid, the grounding leakage current can be extremely eliminated. The voltage across the floating capacitor (C_4) provides a virtual DC-link voltage that can be used to provide an output voltage during negative half-cycle, while the DC-link voltage is the voltage across capacitors C_1 and C_2.

This paper is organized as follows, section 2 introduces the proposed configuration topology. Section 3 shows the operation modes. Section 4 shows the simulation and experimental results. Section 5 provides conclusions.

2. The Proposed Configuration

The proposed MI is shown in Figure 1. It employs an impedance-source, virtual DC bus inverter, an LC output filter, and a resistive load. The impedance-Source network consists of three capacitors, two passive diodes, input inductor (L_{in}), and three winding coupled inductors wounded in a single magnetic core. The virtual DC bus inverter includes five switches and a capacitor C_4 (floating capacitor). The

positive lead of the floating capacitor connected at the common point between S_2 and S_4 while the negative lead linked to the common point between S_3 and S_5 as illustrated in Figure 1.

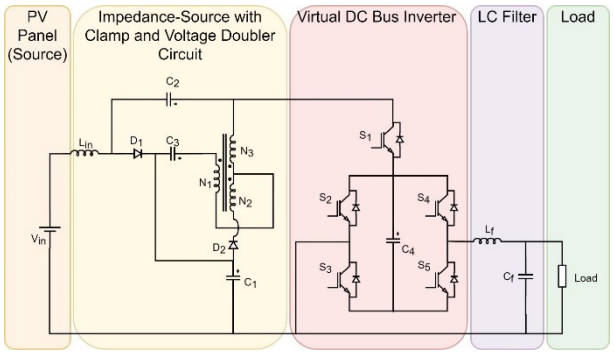


Figure 1: Proposed Single-Phase Transformerless Micro-Inverter.

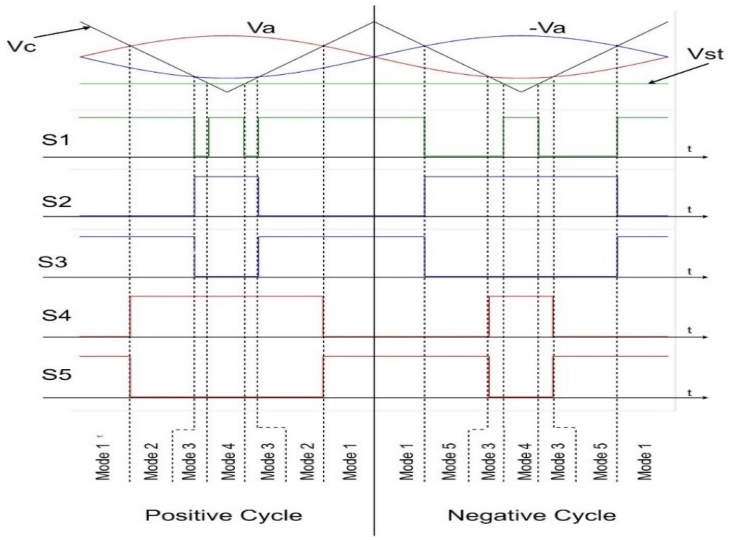


Figure 2: Modulation strategy of the proposed Single-Phase Transformerless Micro-Inverter.

3. The Operation Modes

The switching pattern of the modified unipolar sinusoidal pulse width modulation is shown in Figure 2. The reference signal Va is compared with carrier signal Vc for modulating switches S_2 and S_3, while -Va is the reference signal for modulating switches S_4 and S_5. Vst represents the reference signal for shoot-through time intervals. In the PWM strategy, the switches in the same leg cannot be turned on simultaneously because the floating capacitor provides the virtual DC-link voltage. In the modified PWM, S_3 commutates complementary to S_2 while S_5 commutates complementary to S_4. S_1 commutates at synchronous with S_3. In addition, during the freewheeling mode with S_2 and S_4 conduct, S_1 is conducting again when the Vst is higher than the Vc. The operation modes of the proposed topology can be divided into five operation modes per one cycle where the equivalent circuit for each mode is shown in Figure 3.

1. Mode 1: is the freewheeling mode, in this mode S_1, S_3, S_5 are ON and S_2, S_4 are OFF. Because the voltage sum of the capacitor C_3, inductor N_2, and N3 are higher than the voltage of capacitor C_1, the diode D_2 is reversed-biased. The capacitor C_1 is charged by the input source and input inductors Lin, while the capacitor C_2 and C_3 are charged by inductors N_1 and N_3. Meanwhile, the capacitor C4 is charged by the input source, inductors Lin, N1, and N3.
2. Mode 2: active mode, this mode exists only during the positive half cycle. During this mode switches S_1, S_3, and S_4 are ON while S_2 and S_5 are OFF. Like in mode 1 the capacitors C_1, C_2, C_3 and C_4 are charged by the input source and the inductors.
3. Mode 3: also known as freewheeling mode, during this mode, S_2, S_4 are ON while S_1, S_3, S_5 OFF. The input source and input inductors L_{in} are discharged by the capacitor C_1. Meanwhile, the capacitor C_2 and C_3 are charged by the inductors N_1 and N_3.

4. Mode 4: known as shoot-through (ST) mode, in this mode S_1, S_2, and S_4 are ON while S_3 and S_5 are OFF. The diode D_1 is blocked since the voltage of capacitor C_1 is higher than the input source voltage in combined with an inductor Lin voltage. The capacitor C_1 is discharged by the inductor N_3 through switches S_1 and S_2, while the input source and the capacitor C_2 charge the inductor Lin. In addition, the capacitor C_3 is discharged by the inductors N_1 and N_2 .
5. Mode 5: also known as active mode, this mode exists only during the negative half cycle. The switches S_2 and S_5 are ON while S_1, S_3, and S_4 are OFF. The capacitors C_1, C_2, and C_3 are charged by the input source and the inductors. Meanwhile, the capacitor C_4 provided the voltage required for the load.

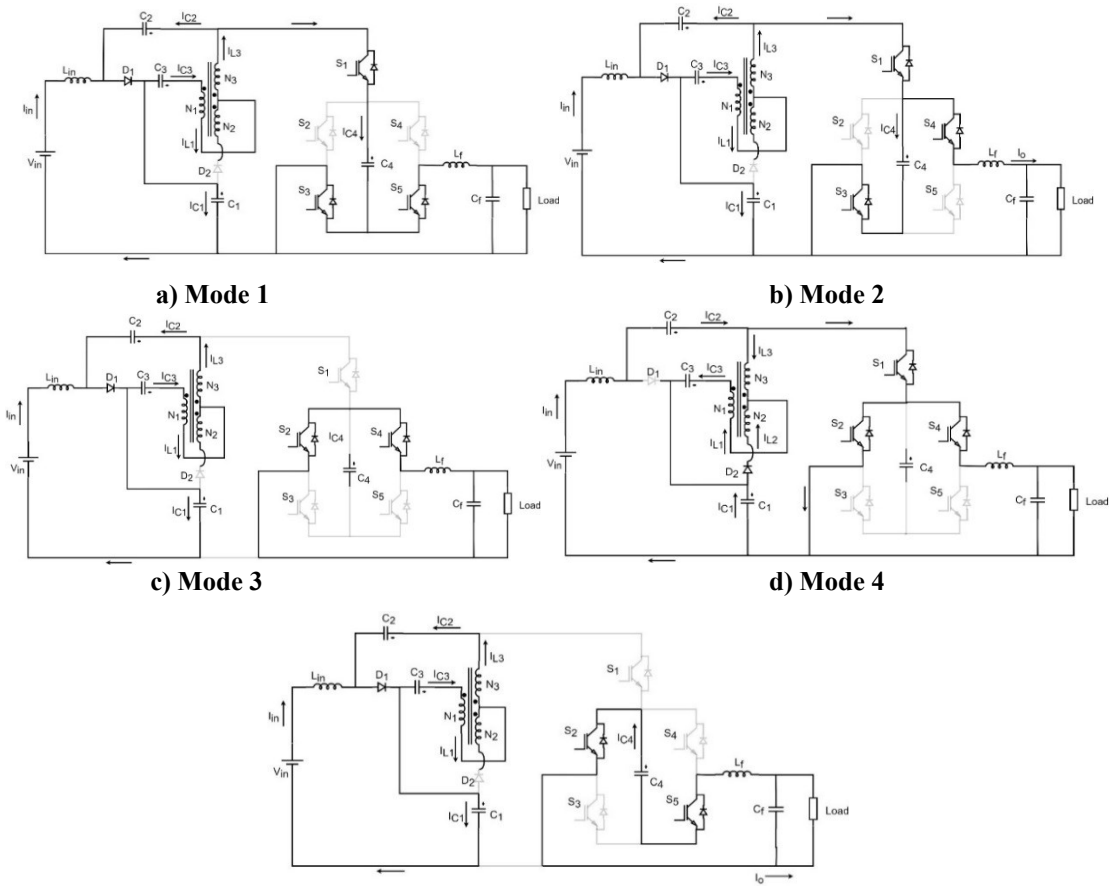


Figure 3: The equivalent circuits of the proposed MI during five modes.

I. Voltage analysis

1. Shoot-Through Mode (ST**)**

The equivalent circuit during the ST mode shown in Figure 4a. ST mode can be achieved by turning on the switches S_1 and S_2 simultaneously. The diode D_1 is reverse biased while diode D_2 is conducting. The circuit expressions during this mode can then be written as follows (1)-(3):

$$V_{C3} - \frac{N_1}{N_3} V_{Lm} - \frac{N_2}{N_3} V_{Lm} = 0 \quad (1)$$

$$V_{in} - V_{Lin} + V_{C2} = 0 \quad (2)$$

$$V_{C1} + \frac{N_2}{N_3} V_{Lm} - V_{Lm} = 0 \quad (3)$$

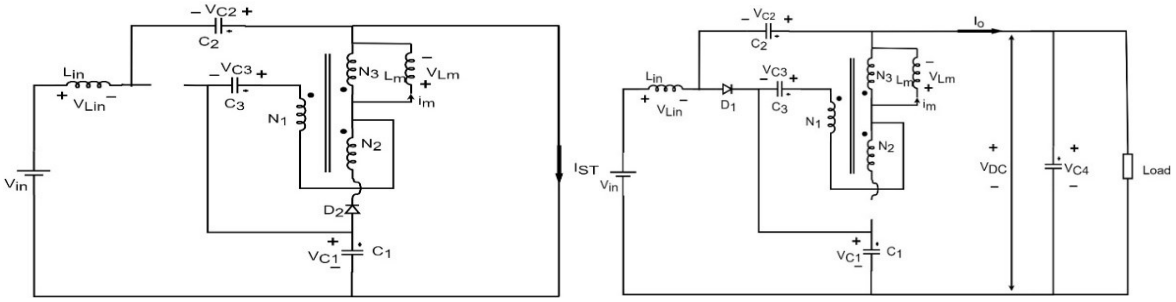
2. Non-Shoot-Through Mode

The equivalent circuit in this mode is shown in Figure 4b. During NST mode the diode D_1 is forward based while the diode D2 is blocking. In this mode, the capacitors C_1, C_2, C_3, and C_4 are charged while the inductors are discharged. During NST mode the following equations (5)-(6) can be derived:

$$V_{C2} + V_{Lm} + \frac{N_1}{N_3} V_{Lm} - V_{C3} = 0 \quad (4)$$

$$V_{in} - V_{Lin} - V_{C1} = 0 \quad (5)$$

$$V_{DC} - V_{C1} - V_{C3} + \frac{N_1}{N_3} V_{Lm} + V_{Lm} = 0 \quad (6)$$



a) ST mode **b) NST mode**

Figure 4: Equivalent circuit of the proposed MI.

The capacitor voltage and the boosting factor of the proposed inverter can be driven by utilizing the circuit expressions during ST mode or DT time interval and non-shoot-through mode or (1-D) T time interval.

From eqs (1) and (4), by applying the voltage second-balance. The voltage of capacitor C_3 can be found:

$$V_{C3} = \frac{(1-D)(N_1+N_2)V_{C2}}{N_1+N_2-DN_2+DN_3} \quad (7)$$

In the same manner, by applying the voltage second-balance for equations (2) and (5). Then the voltage of capacitor C_2 can be found:

$$V_{C2} = \frac{V_{C1}-DV_{C1}-V_{in}}{D} \quad (8)$$

The voltage across C_1 can be found by solving equations (1) and (3) as shown below.

$$V_{C1} = \frac{(N_3-N_2)V_{C3}}{N_1+N_2} \quad (9)$$

Then the voltage across C_1 in term of input voltage V_{in} can be derived as shown below

$$V_{C1} = \frac{(-1+D)(N_2-N_3)V_{in}}{-DN_1-N_2+DN_2+N_3-2DN_3} \quad (10)$$

In the same manner, the voltage across C_2 and C_3 can be expressed as

$$V_{C2} = \frac{(DN_2-N_1-N_2-DN_3)V_{in}}{DN_1+N_2-DN_2-N_3+2DN_3} \quad (11)$$

$$V_{C3} = \frac{(D-1)(N_1+N_2)V_{in}}{DN_1+N_2-DN_2-N_3+2DN_3} \quad (12)$$

By solving the eqs. (4) and (6), the voltage of the DC-link V_{DC} of the proposed inverter can be found as shown below.

$$V_{C4} = V_{DC} = \frac{(N_1+N_3)V_{in}}{DN_2+N_3-DN_1-N_2-2DN_3} \quad (13)$$

By introducing a winding factor K, where $K = \frac{N_3+N_1}{N_3-N_2}$. Then the capacitor voltage eqs. (10), (11), and (12) in addition to DC-link voltage eq. (13) can be rewritten and simplified in terms of shoot-through duty cycle D and winding factor K.

$$V_{C1} = \frac{(1-D)V_{in}}{1-(1+K)D} \quad (14)$$

$$V_{C2} = \frac{(D+K-1)V_{in}}{1-(1+K)D} \quad (15)$$

$$V_{C3} = \frac{(1-D)(K-1)V_{in}}{1-(1+K)D} \quad (16)$$

$$V_{DC} = V_{C4} = \frac{KV_{in}}{1-(1+K)D} \quad (17)$$

Thus, the boosting factor can be obtained from Eq. (17) which is equal to the DC-link voltage over input voltage.

$$B = \frac{V_{DC}}{V_{in}} = \frac{K}{1-(1+K)D} \quad (18)$$

The voltage gains of the proposed MI at different winding factor K and turn ratios (N_1: N_2: N_3) are depicted in Table 1. It can be seen that there is more than one combination of winding turns ratios (N_1: N_2: N_3) to be selected for each winding factor K value for a specific voltage gain and range of shoot-through duty cycle.

Table 1: Gain of the proposed with different winding factor K and turn ratios.

Winding Factor K	$0<D<D_{max}$	Proposed MI Gain	Turn Ratio (N_1:N_2:N_3)
2	0<D<1/3	$\frac{2}{1-3D}$	(1:1:3), (2:1:4), (1:2:5)
3	0<D<1/4	$\frac{3}{1-4D}$	(1:1:2), (3:1:3), (2:2:4)
4	0<D<1/5	$\frac{4}{1-5D}$	(2:1:2), (1:2:3), (5:1:3)
5	0<D<1/6	$\frac{5}{1-6D}$	(3:1:2), (2:2:3), (1:3:4)
6	0<D<1/7	$\frac{6}{1-7D}$	(4:1:2), (3:2:3), (2:3:4)

The winding factor K is previously determined in the designing of the inverter. Thus, the boosting factor of the proposed inverter was determined only by the value of the ST duty cycle. The higher the duty cycle D, the higher the output voltage can be obtained. Figure 5 shows the boosting factor of proposed MI with different duty cycles and winding factor.

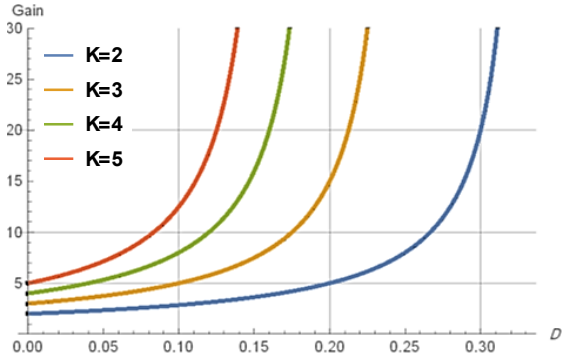


Figure 5: Boost factor of the proposed topology at the different shoot-through duty cycle and winding factor.

The AC output voltage of the proposed inverter can be obtained as follows:

$$V_{AC} = BMV_{in} = \frac{K}{1-(1+K)D} MV_{in} \quad (20)$$

Where M represents the modulation index. The maximum modulation index corresponding to the ST can be driven below:

$$M=1-D \quad (21)$$

II. Current analysis

Similar to the voltage analysis, there are two operation modes the ST mode and non-shoot-through mode. The magnetizing current can be calculated as follows:

$$\begin{cases} N_3(i'_3) + N_2 i_2 + N_1 i_1 = 0 \\ i'_3 = i_3 - i_m \\ N_3(i_3 - i_m) + N_2 i_2 + N_1 i_1 = 0 \\ i_m = \frac{N_1}{N_3} i_1 + \frac{N_2}{N_3} i_2 + i_3 \end{cases} \quad (22)$$

Where i_1, i_2, and i_3 are the instantaneous currents via windings N_1, N_2, and N_3 respectively, while i_m is the magnetizing current

1. Shoot-Through Mode

The circuit expressions during ST mode using KCL can be written as follows:

$$i_1 = -i_{C3} \quad (23)$$
$$i_2 = i_{C1} + i_1 \quad (24)$$
$$i_3 = -i_{C1} \quad (25)$$
$$i_{C2} = -i_{in} \quad (26)$$

2. Non-Shoot-Through Mode

The circuit expressions during NST mode using KCL can be written as follows:

$$i_{C1} = i_{in} - i_o \quad (27)$$
$$i_1 = i_3 = -i_{C3} = (i_{C2} + i_o) \quad (28)$$
$$i_2 = 0 \quad (29)$$
$$i_{C2} = i_3 - i_o \quad (30)$$

By applying charge-second balance on the current equations can be obtained as

$$I_m = \frac{i_{in}(N_1+N_3)}{N_3} \quad (31)$$
$$I_o = \frac{(-1+2D)i_{in}}{-1+D} \quad (32)$$

4. Simulation and Experimental Results

Simulation and experimental of the proposed topology are carried out to confirm the theoretical analysis above, while the circuit parameters are given in Table 2.

Table 2: Parameters that used for simulation analysis

Parameter		The Proposed MI
Input voltage (V_{in})		25V
Output voltage (V)		30 V r.m.s
	L_{in}	3mH
	L_f	3.3mH
Inductors	N_1	15
	N_2	15
	N_3	45
	C1	220uF
	C2	220uF
Capacitors	C3	220uF
	C4	940uF
	C_f	10uF
K		2
Power		25W
Operation frequency		50 Hz
Switching frequency		10 kHz

I. Simulation Results of the Proposed MI

The overall system performance has been analysed and evaluated through the PLECS software simulator. The DC-link voltage according to the mathematical analysis equal to 108V at Vin=25V, K=2, and D=0.18. However, the simulation result of the DC-link voltage was about 100V as shown in Figure 6. The PLECS simulator uses the specifications for the circuit design to provide more realistic results. Figure 7 shows the simulation result of the DC-link voltage of the traditional YSN with the virtual DC bus inverter [5]. The simulation carried out at the same parameters used for the proposed MI. It is clearly shown that the DC-link voltage of YSI is roughly half of the DC-link voltage of the proposed MI, where

it's measured equal to 52V. The unfiltered output voltage, sinusoidal output voltage and load current of the proposed topology are shown in Figure 8, Figure 9, and Figure 10 respectively.

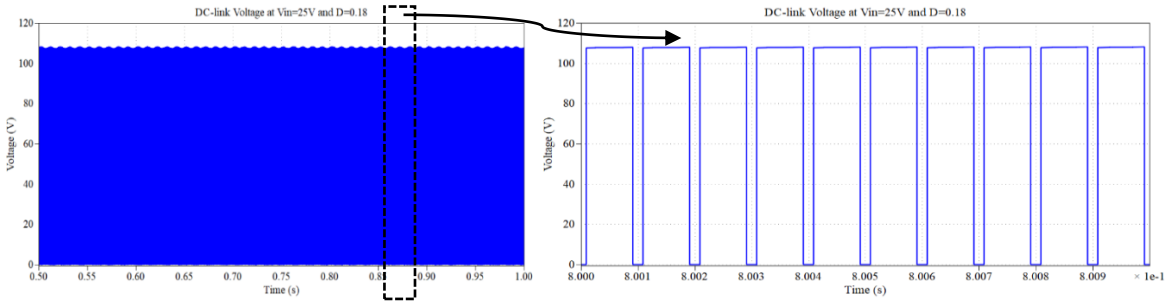


Figure 6: Simulation results of the proposed MI operating with two modes shoot-through mode and active mode (non-shoot-through mode). DC-link voltage at Vin=25V, K=2 and D=0.18.

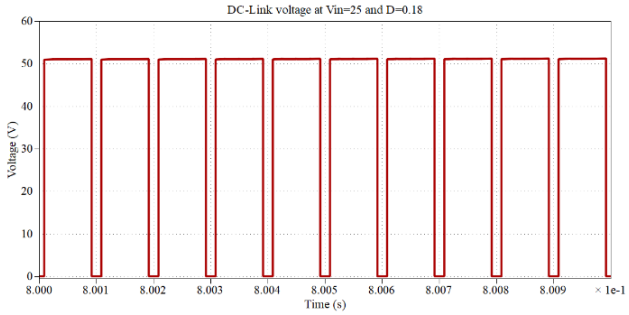


Figure 7: Simulation results of the traditional YSN DC-link voltage at Vin=25V, K=2, and D=0.18.

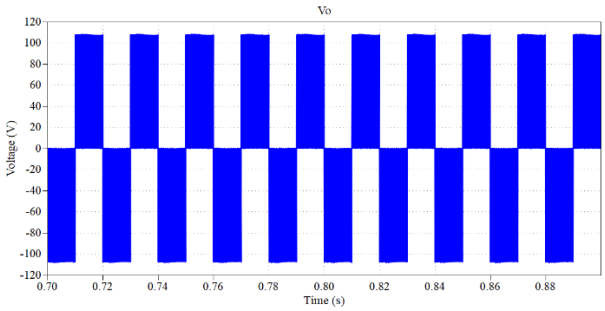


Figure 8: Simulation results of output voltages without a filter.

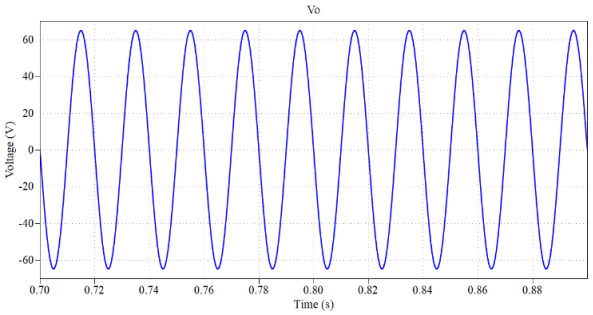


Figure 9: Simulation results of sinusoidal output voltages with filter.

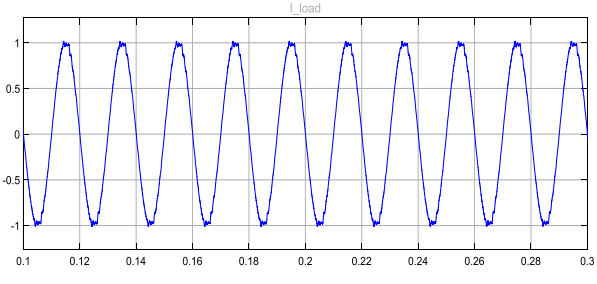


Figure 10: Simulation results of load current.

The proposed MI exhibit lower voltage stress across the diode D_1 than traditional YSI as shown in Figure 11, which clearly indicates that the voltage stresses across YSI diode D_1 are about 3 times greater than of the proposed MI at the same output voltage. This is considered one of the most important points that solved in this topology. The voltage stresses across diodes D_1 and D_2 are shown in Figure 12. It can be seen that the diode D_1 stress during ST mode equal to the DC-link voltage, while the D_2 is zero, implies it is conducting during ST. On the contrary, during the NST the diode D_2 is blocking and the voltage across it equal to half the voltage 50V. Figure 13 shows the voltage of the capacitors, where the voltage of C_1 and C_3 have equal voltage values. The voltage of C_4 is the same as the DC-link voltage. Figure 14 shows the input current of the proposed topology. It can be seen that the input current is free of ripple and increases during ST mode and decreases during NST mode. The current through winding inductors is shown in Figure 15. The current through switch S_3 which is shown in Figure 16, where the stress of S_3 has higher stress during the negative half cycle.

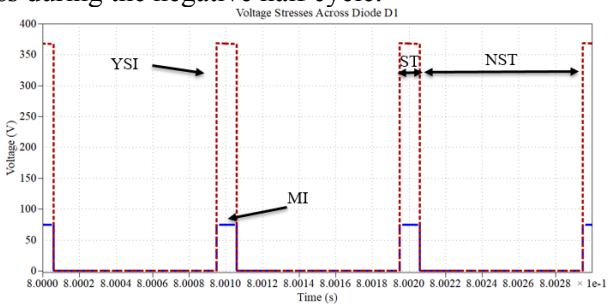


Figure 11: Simulation results of voltage stress across diode D_1. Both topologies compared at the same output voltage.

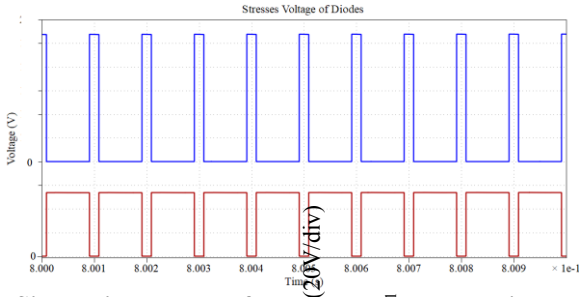


Figure 12: Simulation results of voltage stress across diodes D_1 and D_2.

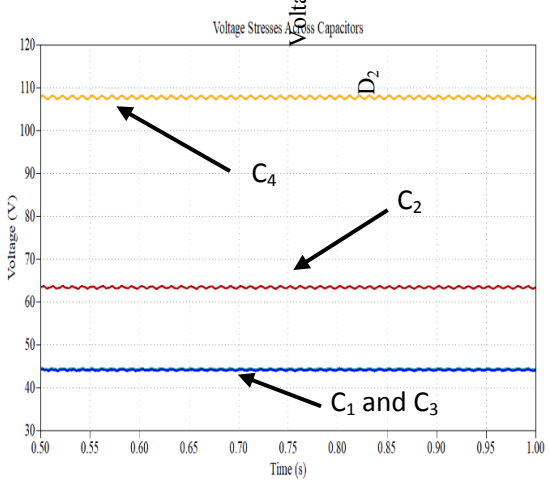


Figure 13: Simulation results of the voltage across capacitors C_1, C_2, C_3, and C_4.

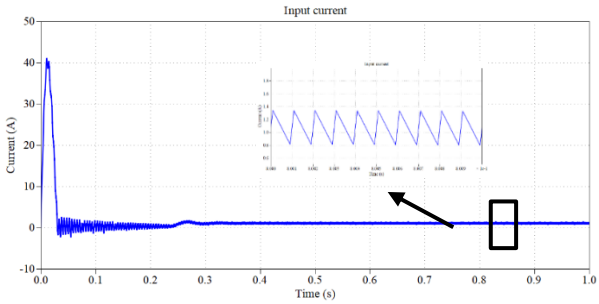


Figure 14: Simulation results of the input current.

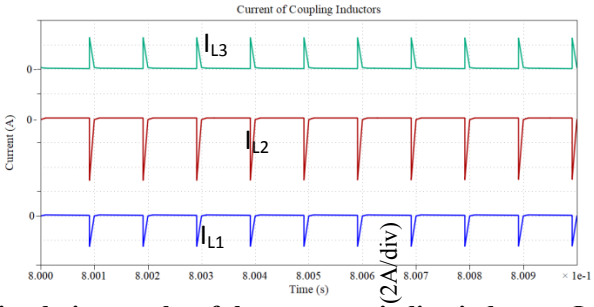


Figure 15: Simulation results of the current winding inductors L_1, L_2, and L_3.

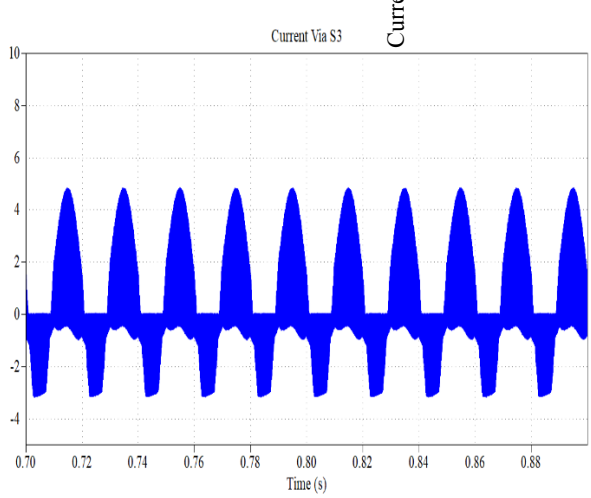


Figure 16: Simulation results of the current through switch S_3.

5. Experiential Results

To validate the performance of the proposed transformerless boost MI, a 25W scale-down prototype is developed. A photograph of the laboratory experimental set-up is shown in Figure 17.

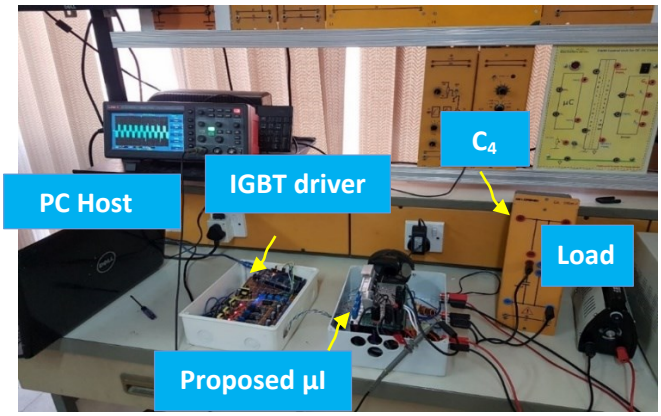


Figure 17: Photograph of the 25W MI experimental set-up.

It can be seen in Figure 18, that the DC-link voltage increased to 100V at D=0.18 which is due to three factors. These are the winding factor, voltage doubler operation of the proposed converter, and the change of D. As such, from 25V as input voltage, 100V DC output voltage is obtained which is difficult when using traditional boost converter or YSI at the same D. It can be clearly shown that the result is in good agreement with the mathematical and simulation results. The results illustrated that there is no spike voltage applied across the IGBT switches. Hence, the influence of leakage inductance is completely eliminated. Thus, the passive snubber circuit requirement is not needed in the proposed MI, which increases the overall efficiency of the converter. This is due to that the converter based on an active clamp circuit to recover the leakage inductance energy of the three-winding transformer. Figure 19 shows the output voltage of the converter with the LC filter. It is clear that the peak filter output voltage is reduced due to the effect of PWM and LC filter. Also, the obtained peak voltage at D=0.18 is equal to 56V. The voltage stresses across the diodes D_1 and D_2 cycled= 0.18 is shown in Figure 20. The voltage stresses of diode D_1 and D_2 are 100V and 60V respectively. The voltage stresses across S_3 is shown in Figure 21. As observed in the simulation results, the voltage stresses across all five switches are the same and equal to DC-link voltage which equals to 100V at D=0.18. The voltage spikes are clamped to the DC-link voltage, thanks for clamping diode.

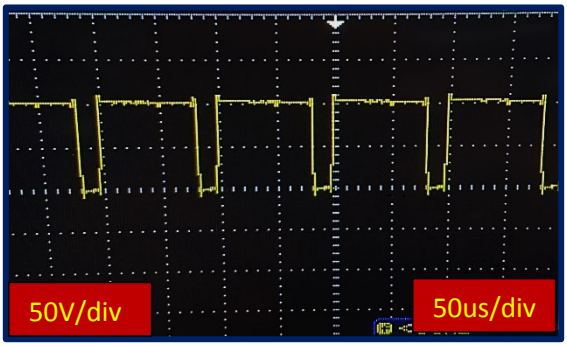


Figure 18: Experimental result of the proposed MI. DC-link voltage at D=0.18, K=2, and V_{in}=25V.

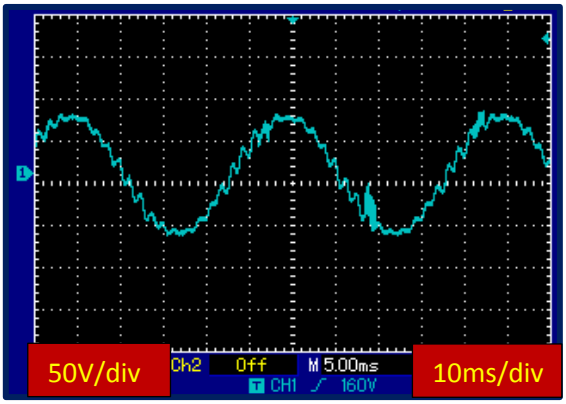
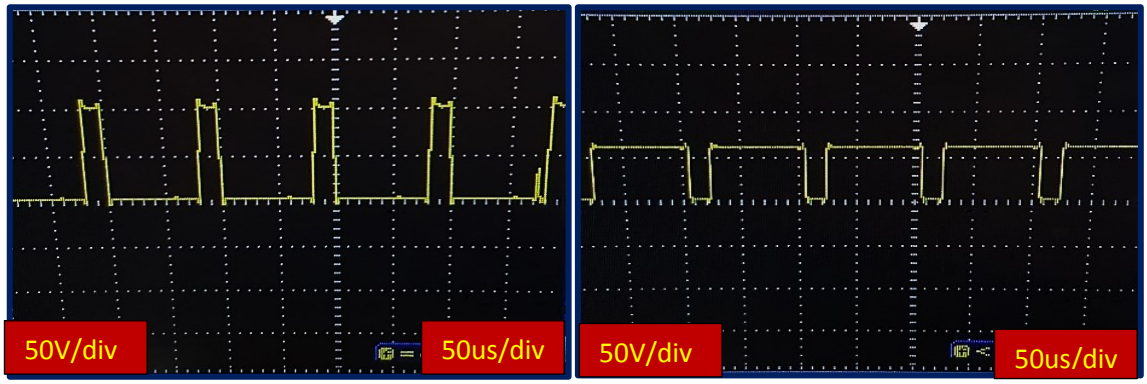


Figure 19: Experimental results show alternating output voltage with the filter at D=0.18, K=2, and V_{in}=25V.



a) Diode D_1 **b) Diode D_2**

Figure 20: Experimental result shows the voltage across the diodes at D=0.18, K=2, and Vin=25V.

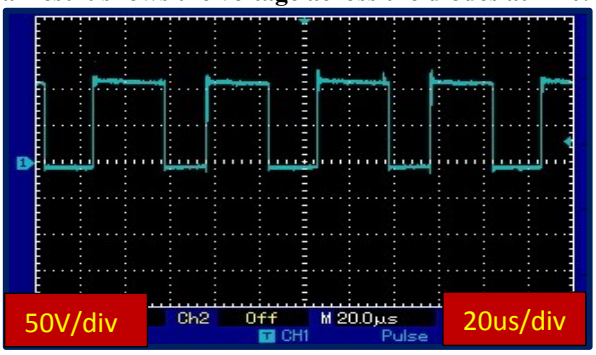


Figure 21: Experimental result shows the voltage across switches S_3 at D=0.18, K=2 and, Vin=25V.

The input current of the proposed MI at D=0.18 is shown in Figure 22. It is clear that the input current is continuous with ripple less than 0.5A. Thus, the proposed MI is the most suitable MI for PV applications maintain MPPT tracking. Figure 23 shows the currents through the three windings L_1, L_2, and L_3 at D=0.18. It can be seen that the current in continuous conduction mode via the L_1 and L_3, while in critical mode through L_2. However, the current stress through the windings is within an acceptable range. Figure 24 shows that the common-mode voltage is very small which eliminating the leakage current. This is one of the important features of integrating the proposed impedance network with the common ground virtual DC bus inverter configuration that performs the proposed MI.

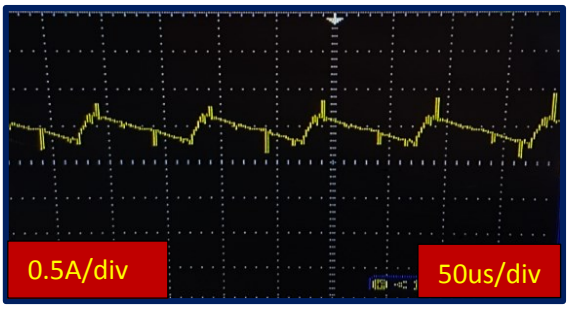
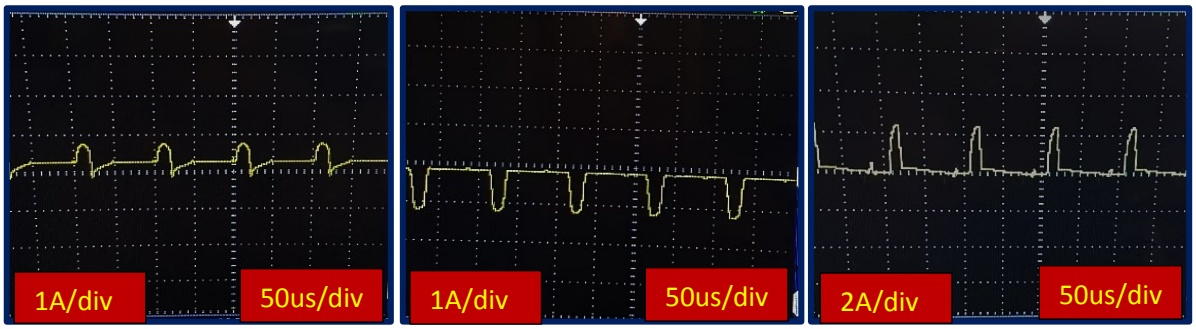


Figure 22: Experimental result shows the input current through inductor L_{in} at D=0.18, where K=2 and V_{in}=25V.



a) L_1 **b) L_2** **(c) L_3**

Figure 23: Experimental result shows the current through coupling inductors at D=0.18, K=2, and V_{in}=25V.

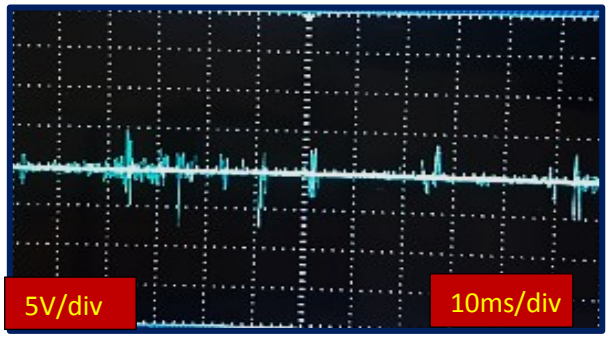


Figure 24: The common-mode voltage waveform.

Based on all previous results, the experimental results agree with the mathematical and simulation results. However, as mentioned earlier due to the non-availability of some of the required components such as the ferrite core (type and size) and high-frequency capacitors with high-level value, scaling-down of the output voltage was necessary to validate the proposed MI. The converter can produce higher voltage gain to the required DC-link voltage of industrial MI with DC-link voltage up to 400V. Thus to prove that the proposed MI can be reached to the voltage of grid utility which is 220Vrms, simulation analysis was conducted based on the parameter listed in Table 3.

Table 3: The proposed MI parameters used in the simulation.

Parameter		The Proposed µI
Input Voltage range		40-60V
Duty cycle range		0.1-0.14
Output voltage (V)		220V r.m.s
Inductors	L_{in}	3mH
	L_f	3.3mH
	N_1	60
	N_2	30
	N_3	60
Capacitors	C_1	220uF
	C_2	220uF
	C_3	220uF
	C_4	940uF
	C_f	10uF
K		4
Power		300W
Operation frequency		50 Hz
Switching frequency		10 kHz

The DC-link voltage and AC output voltage of the simulation results are shown in Figure 25 and Figure 26 respectively.

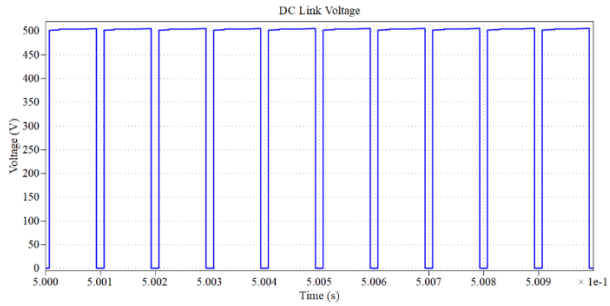


Figure 25: Simulation results of the DC-link voltage of the proposed MI.

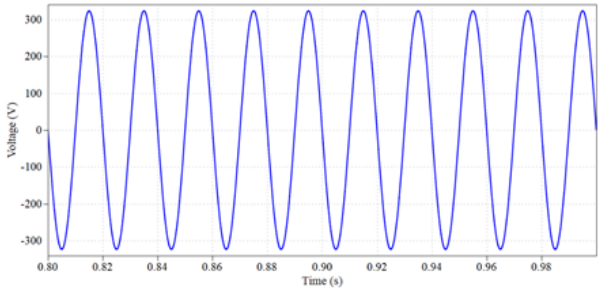


Figure 26: Simulation results of the sinusoidal output voltage of the proposed MI.

6. Conclusions

This paper presents a new design of transformerless single-stage MI based on impedance source configuration. The proposed MI produces a double high voltage gain than traditional Y-source inverter at the same number of the turns ratio. This reduces the leakage inductance resulting from the coupling inductors. Also, the negative pole of the PV panel is directly connected to the neutral line, eliminating the leakage current completely. Active clamping is used to eliminate leakage current, thus no passive snubber circuit is needed. The proposed converter is operating in continuous conduction mode in all conditions, even with a light load with a ripple current less than 0.5A. Nevertheless, the impedance source structure provides blocking DC coupling for the ferrite core due to using one additional capacitor. These factors make the proposed MI more suitable for PV residential applications. Finally, simulation and experimental results verified the mathematical model of the proposed MI.

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