The Electrical Conduction Process and Trapping Studies In SiO_2 Films

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Abstract

Electrical conduction in Silicon dioxide (SiO_2) films of thickness range from 100-200 nm with aluminum top-contact have been studied. The (MOS) metal-Oxide-semiconductor structure is found to be strongly rectifying. In forward applied bias, the current is space-charge limited (SCL) with clear indications of progressive filling of traps. In reverse biasing condition, a Schottky-type, field-enhanced emission from the top-contact is believed to occur with $\varphi = 0.44$ eV.

Introduction:

The properties of a thin amorphous silicon dioxide grown above a silicon wafer have been studies by many researchers[1, 2]. Silicon dioxide films are used for purpose of surface passivation and diffusion masking during fabrication processes of planar silicon devices[3]. Therefore, recently, such insulating films has been applied to many kinds of electronic devices such as insulated gate thin film transistors, static random access memory devices, as a metal-oxide-semiconductor in field effect transistors and as metal-insulator-semiconductor structure[4-7]. The electrical and dielectric properties of these oxide films are strongly affected by two important factors, Firstly, the technique used for the fabrication of the insulating films. Many authors,[8, 9] have been used the thermal oxidation, anodisation, sputtering and plasma oxidation technique for the preparation of the SiO_2 films. Secondly, The annealing temperature after fabrication of SiO_2 films.

In this paper, we fabricated the SiO_2 films by using thermal oxidation under the condition of dry pure oxygen.Their conduction mechanism have been studied in both forward and reverse biasing conditions. A space-charge-limits current (SCLC) and Schottky-type filed-enhanced emission conduction were proposed respectively.

Experimental Techniques:

The silicon substrates which have been used in this study- is a p-type of resistivity 5(Ω cm) and concentration 10^{16} cm^{-3}. All the wafers were first cleaned ultrasonically using trichloroethylene (TCE) at a temperature of 70 °C for 5 mins,then it is followed by cleaning with acetone and isopropanol Alcohol (IPA). All the substrates are then immersed in boiling is it deionized water for 5 mints and finally dried. Secondly; a chemical polishing procedure is carried out by using 1:10 HF: H_2O by volume. This step is followed by rinse in deionized water and dried. The silicon substrate is placed inside afurnace to expose the substrate to a steam of dried oxygen at a temperature 1100 °C for different periods of time (15, 30, 45, 60, 90) mints in order to obtain different oxide thickness (100-200) nm.

To form agood ohmic contact thin layer of high purity Al was evaporated at the back of the silicon wafers, then annealed in vacuum at temperature of 400 °C for time of 30 mints. To complete the MOS devices a circular dots of aluminum (area = 1.45×10^{-3} cm^2) were evaporated using a very thin metal mask under vacuum of around 1×10^{-5} torr. All the current-voltage (I-V) measurements were carried out at different temperature using a digital electrometer type Hp model (PM 2528).

Results and Discussions:

Fig. (1) shows the forward biased current-voltage characteristics of MOS structure at room temperature for three thickness (100, 150 and 200) nm. There is first of all, a steep increase of current with voltage and then a more or less distinct break-point above which the current rises more slowly with $I\alpha V^2$. This latter dependence is a first indication that current density becomes space-charge-limited (SCL) in this region and can be represented by using a relation with a set of traps at a single level as follows[10]:

$$J=\frac{9}{8}\mu\theta\varepsilon V^2/d^3 \quad \ldots (1)$$

Where d is the oxide thickness, θ is the ratio of free to trapped carriers and μ is the mobility of electron.

In order to confirm that equation (1) applies in a given case it is in fact more important to verify the $1/d^3$ rather than the V^2 dependence. The effect of thickness change is shown in Fig. (2). Currents being determined at a voltage within the square-law region (1-30) V for the three cases. A reasonable $\left(I \alpha \frac{1}{d^3}\right)$ dependence is obtained.

There is no indication of a traps-filled-limited voltage (V_{TFL}) which would be marked by a sharp rise in the current in the upper reaches of the V^2 region, except that most MOS structure broke down at voltages slightly in excess of those shown in Fig. (1). The trap density is given by using[10]:

Trap density = $2 E V_{TFL}/ed^2$,with using the maximum voltages reached, the minimum trap densities are found to be equal to 10^{24} m^{-3}.

As shown in Fig. (1), the steeply rising region in the characteristics of MOS structure must now be considered, and because the ultimate current appears to be SCL, it is logical to suppose that these arise from the space charge controlled conduction in the presence of a partially filled band. Such a band of traps must be at distinctly lower energy level than the single trap proposed for the V^2 region. If the transition to the V^2 region represents the filling of a lower band of traps, then this voltage may be used as

V_{TFL} to estimate the density of traps as above and the value of 10^{-33}-10^{24} m^{-3} is obtained.

Several authors[11,12] have been suggested that for much thinner films, the increase of current with applied bias voltage is due, not to a trap-filling process, but to the Poole-Frenkel effect reduction of the depth of the trapping state. Results are plotted according to this as shown in Fig. (2) and yield a very non-linear characteristic, in disagreement with the theory.

Applying reverse bias, for MOS structure is shown in Fig. (3), the result strongly suggests that the stable conduction mechanism is due to Schottky effect; that is, field-assisted thermionic emission at the top-electrode. A plot of ($ln*J/E$-V_s-$E^{1/2}$) was yield a very non-linear characteristic as shown in Fig. (4), suggesting that the Poole-Frenkel process of field-assisted release of charge from traps in the bulk was not occurring. According to the Schottky effect, the relation is given as[10]:

$$J = AT^2 \exp\left\{-\left(\varphi - \beta E^{1/2}/kT\right)\right. \quad \ldots (2)$$

Where A is the emission coefficient, φ is the zero-field barrier at the metal-dielectric interface and $\beta = (e^3/4\,\pi\varepsilon)^{1/2}$ is the Schottky coefficient.

In order to confirm the Schottky conduction mechanism, it is important to plot the relation between log (I/T^2)-vs-1000/T, as shown in Fig. (5). The results show clearly that the barrier involved decrease with applied field as it should. Extrapolation of the values of activation energy to zero applied field gives ϕ = 0.44 eV. Although agood agreement with equations (2) found for the field and temperature dependence, the actual current values are many orders of magnitude lower than predicted by equation (2) with using the value Richardson constant $A = 1.2\times10^6$ Amp. $M^{-2}K^2$ and zero filed value ϕ = 0.44 eV.

Conclusions:

The contrasting transients for the two polarities are taken to be strong evidence for easy electron injection and space-charge-limited (SCL) when the back contact is negative, and limited injection with consequent trap emptying when it is positive.

The trap-filling characteristics together with weakly dependent activation energy in forward applied bias suggest a high density band of trapping states in which the trap energy (E_t) is largely pinned so that (E-E_t) remains at approximately at 0.44 eV. In addition, strong forward injection gives the V^2 region and indicates a single set or narrow band of trapping levels.

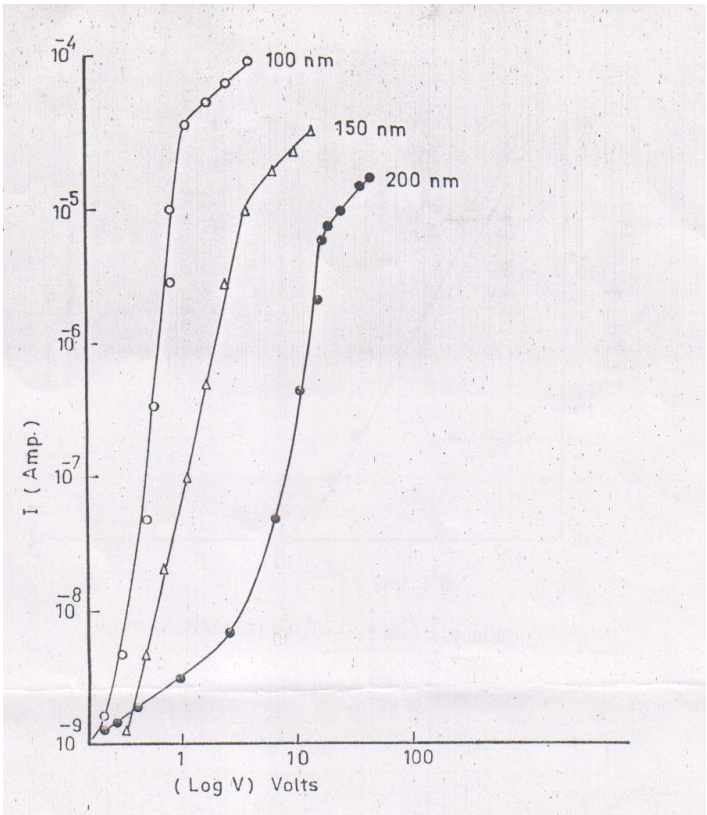

Fig. (1): Log I-vs– Log V for MOS structure at different oxide thickness.

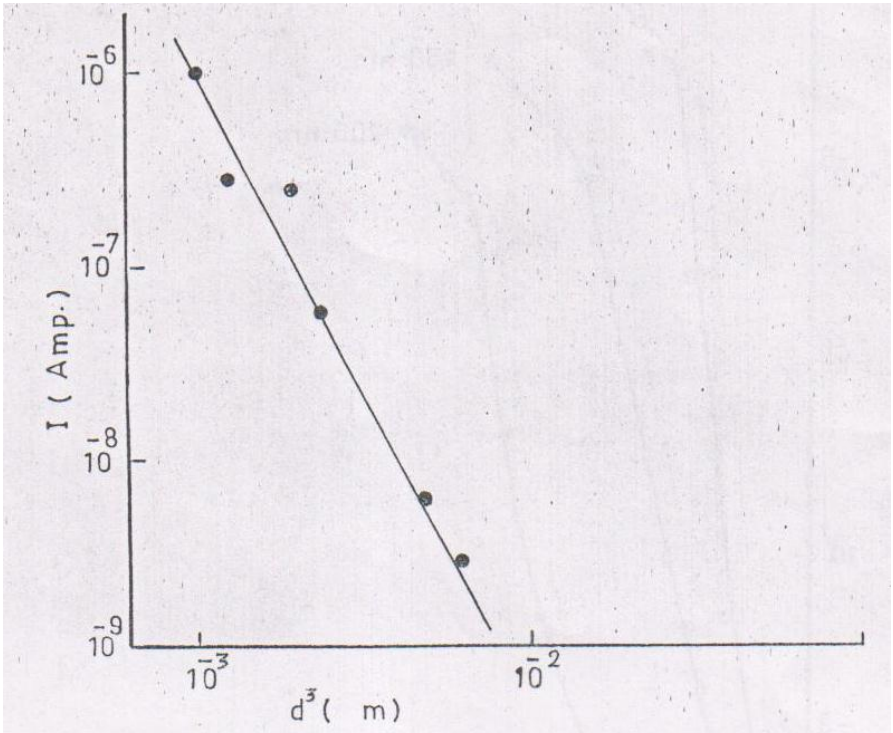

Fig. (2): Log I –vs-d^3 plot for MOS structure.

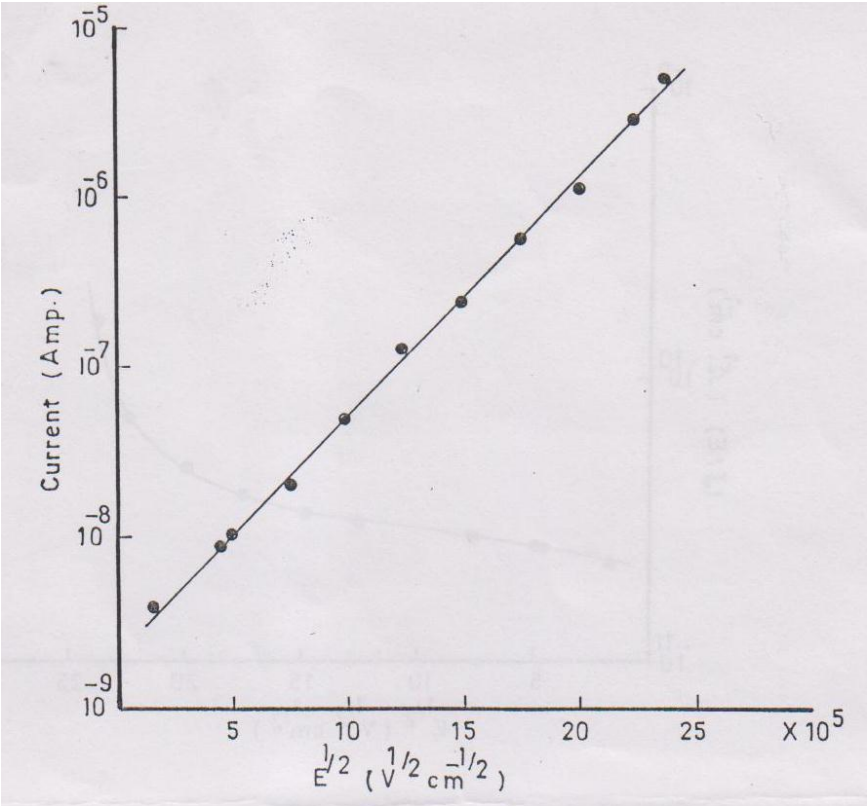

Fig. (3): I –vs-$E^{1/2}$ characteristics showing the Schottky plot.

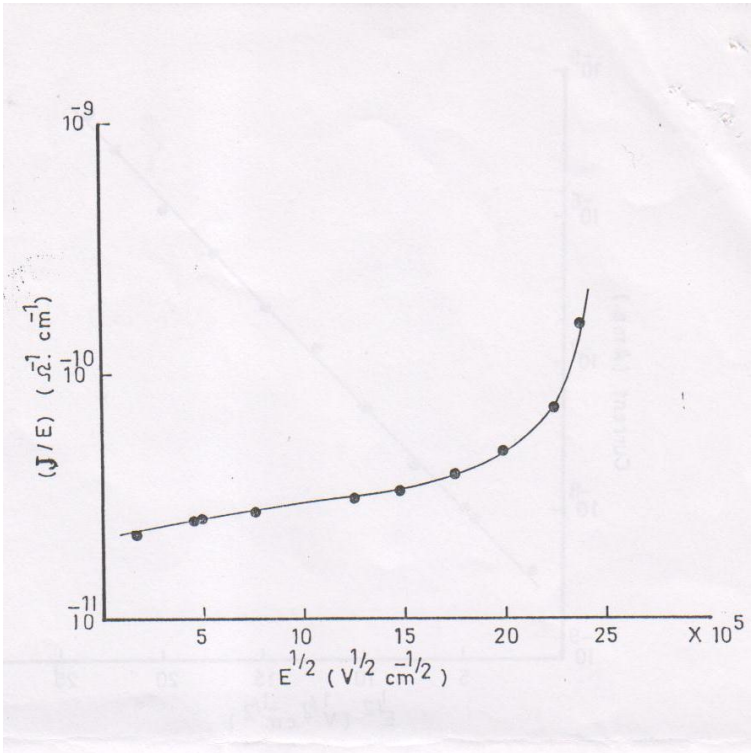

Fig. (4): (J/E) –vs-$E^{1/2}$ characteristics showing Pool-Frenkel plot.

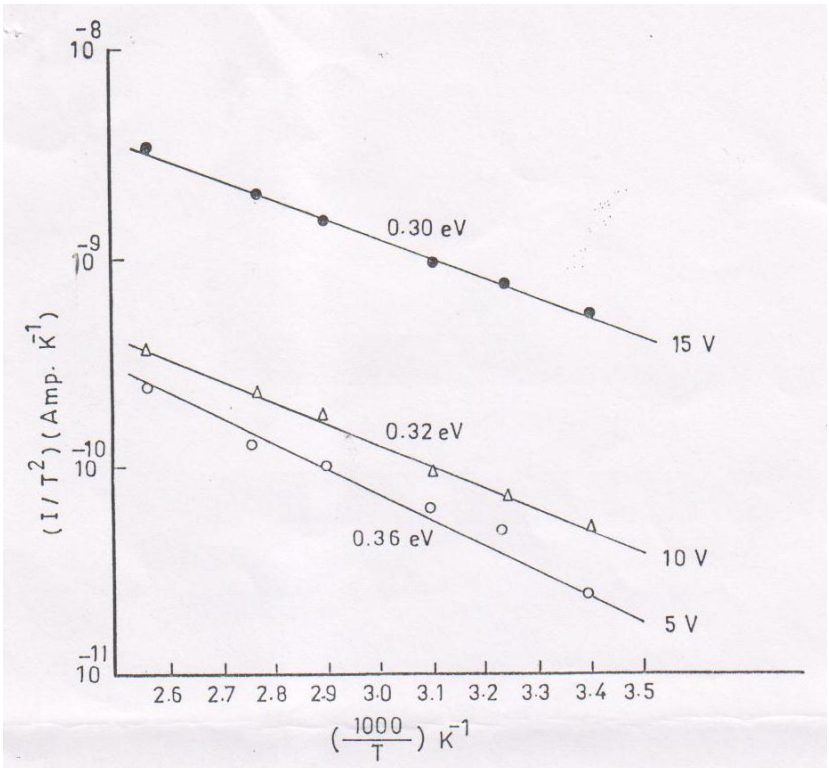

Fig. (5): (I/T^2) –vs-1000/T characteristics for MOS structure.

References:

1- Ng, K. K., Polito, W. J. and Ligenza, J. R. (1984), Growth Kinetics of Thin Silicon Dioxide in Controlled Ambient Oxidation System, J. Appl. Phys., Vol. 44, P. 626.

2- Chattopadhyay, P. and Daw, A. N., 1986. On the Current Transport Mechanism in a Metal-insulator-Semiconductor (MIS) Diode. Solid State Electronics, Vol. 29, P. 555.

3- Pulfrey, D. L., and Tarr: N. G., 1989. Introduction to Microelctronic Devices. Prentice-Hall International, Inc.

4- Asano, T. and Makihira, K. and Tsutae, H. Jap., 1994. "One-Gate-Wide MOS Inverter with Stacked Transistors. J. Appl. Phys.Vol. 33, P. 659.

5- Asano, T. Makihira, K., Jap., 1993. Control of Si Solid Phase Nucleation by Surface Step for High-Performance TFTs" J. Appl. Phys. Vol. 32, P. 482.

6- Okada, Y. Aoto, K. and Asano, T., 1996. Extended Abstract of the 1996 International Conference on Solid State Devices and Materials, P. 374, Augt., Yookohama, Japan.

7- Mohammed, M. A., 1994. Design of Ion Implanted MOSFETs with Very Small Physical Dimensions. J. Educ. And Sci., Vol. 19, P. 54.

8- Shabalov, A. L. and Feldman. M. S.m 1986. Atomic Defects and Stresses in r.f.-sputtered SiO_2 Thin Films. Thin Solid Films, Vol. 143, P. 53.

9- Shabalov, A. L. and Feldman. M. S. 1983. Standardized terminology for Oxide Charge Associated with Thermally Oxidized Silicon. Thin Solid Films, Vol. 110, P. 215.

10- Simmons J. G. (1971). "DC Conduction in Thin Films" Mills and Booy Limited, London.

11- Mohammed, M. A. and Mohammed, A. S., 1998. The Study of Space Charge limited Current (SCLC) Conduction in Anodic Tantalum Oxide Film. J. Educ. And Sci., Vol. 28, P. 67.

12- Oehrlein, G. S. and Reisman, A. (1983). Electrical Properties of Amorphous Tantalum Pentoxide Thin Films on Silicon, J. Appl. Phys. Vol. 54, P. 6502.

دراسة عملية التوصيل الكهربائي والقنص في أغشية ثاني أوكسيد السيليكون (SiO_2)

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الملخص

تم في هذا البحث دراسة التوصيل الكهربائي لأغشية ثاني أوكسيد السيليكون (SiO_2) لسمك اوكسيد يتراوح بين .nm (100-200) وباستخدام الألمنيوم للتوصيل الفوقي. وقد وجد بأن تركيب معدن . أوكسيد . شبه موصل (MOS) يمتاز بتقويم عالي ، وأن آلية توصيل التيار عند الانحياز الأمامي هو التيار المحدد بالشحنة الفراغية (SCL) مع دليل واضح لمليء القوانص. ظهر أيضاً بأن آلية توصيل التيار عند الانحياز العكسي هو نوع شوتكي . للانبعاث المجالي وبحاجز جهد قدره $\phi = 0.44$ eV.