Design and Fabrication of A Carbone Nanotube Field Effect Transistor Based on Dielectrophoresis Technique and Low Cost Photolithography

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Abstract

In this work, Micro- and Nanofabrication technology was used to fabricate and demonstrate a simple Carbon nanotubes (CNTs) field effect transistors (FETs) which is constructed on Si/SiO_2 substrate. Simple photolithography technique was used for patterning the photoresist using a mask and a UV LEDs. Thermal evaporator was utilized to deposit coper metal on the substrate. After liftoff, electrodes of 5 µm width and spacing of 3 µm were achieved. Deilecrophrisis technique was adopted to fetch the CNTs towards the fabricated electrode fingers. The fabricated CNT-FETs exhibit high electron mobility, around 10000 cm^2/Vs. Current transfer characteristic observed that the device has p-type semiconductor properties, which can be attributed to the oxygen molecules absorption of CNTs oxygen from the testing environment.

Keywords: Carbone nanotube transistor, Photolithography, Nanofabrication fabrication

الخلاصة

في هذا البحث استخدمت تكنولوجيا التصنيع النانوي والمايكروي لبناء واختبار ترانزيستور تاثير المجال باستخدام الكاربون نانو تيوب. تم تم تصنيع الترانسيستور على قاعدة من السليكون\ثاني اوكسيد السليكون واستخدمت تكنولوجيا الفوتوليثوكرافي باستخدام مواد رخيصة الثمن تتمثل بدايود مشع للاشعة فوق البنفسجية وقناع وذلك لعمل التشكيل المطلوب لالكترودات الترانسوستر المصنع. استخدم المبخر الحراري لتبخير مادة النحاس على سطح القاعدة. بعدها استخدمت طريقة الدايلكتروفورسز لسحب الكاربون نانوتيوب نحو الالكترودات ، اختبر الجهاز من الناحية الالكترونية . نتائج الاختبار اثبتت انه من نوع p-type وسبالتي ذلك يعود الى امتصاص جزيئات اوكسجين الجو في منطقة الاختبار من قبل الكاربونانو تيوب. ايضا كانت حركية حاملات الشحنات عالية نسبيا بمقدار 1000 سم^2\فولت.ثانية تقريبا.

الكلمات المفتاحية:– ترانسستور، كاربون نانوتيوب، فوتوليثوكرافي، تصنيع نانوي.

1- Introduction

Carbone nanotube shows great promise among electronic materials since its discovery, around 3 decades ago due to its remarkable mechanical and electrical properties (Janas, 2018; Dai, 2002; Dresselhaus *et.al.*, 2000). CNTs are ideal method to study one-dimensional electronic transport phenomena. Specifically, single-walled carbon nanotubes exhibit excellent electronic properties, such as high mobility of the charge carriers and high current capacity (Yao *et.al.*, 2000; Franklin, 2013; Fuhrer *et.al.*, 2002). Depending on the chirality of their atomic structure, the CNT is either metallic or semiconducting. Semiconducting nanotubes have been used in the fabrication of CNTs field effect transistors (CNTFETs) as an alternative to the conventional Si transistors (Fuhrer *et.al.*, 2002) . Great progress has been made to enhance the electronic properties of CNTFETs by several technologies such as decreasing the gate oxide thickness (Tans et al., 1998), using high dielectrics constant for the gate oxide (Tans *et.al.*, 1998; Bachtold *et.al.*, 2001; Javey *et.al.*, 2002), doping CNTs by electron donor/ accepter to obtain n-type or p-type semiconductors (Duclaux, 2002) or reducing contact resistance by selecting proper contact metals (Javey *et.al.*, 2004; Matsuda *et.al.*, 2010).

In this work, we suggest a simple tools to simplify the fabrication process of the CNT-FETs. In the following sections we will discuss in details the fabrication process, the operation principle, the testing setup, and experimental results of the CNT-FETs.

2- Device fabrication

a- Photolithography

Recently, several articles have reported a new technology for generating UV light using UV Light Emitting Diodes (UV-LEDs) (Yapici and Farhat, 2014; Byeon *et.al.*, 2012). This type of UV-LEDs was successfully used in the micro/nano fabrication. Examples include a single and array of LEDs for both direct patterning and special emission of the UV light. UV-LED exhibit a comparable performance to the conventional UV source.

In this work, a torch UV-LEDs was used as a UV source in the photolithography process.

Before involving the LEDs torch in the lithography process, its intensity was measured and calibrated by AB-M model 100-C UV intensity meter (Figure 1a). The calibration curve was obtained by applying several voltage values to the UV LEDs array and measuring the corresponding intensities. The calibration curve showed linear relationship (Figure 1b). Basically, the applied intensity and the time duration is depending on the type of the photoresist that supposed to be used in the photolithography.

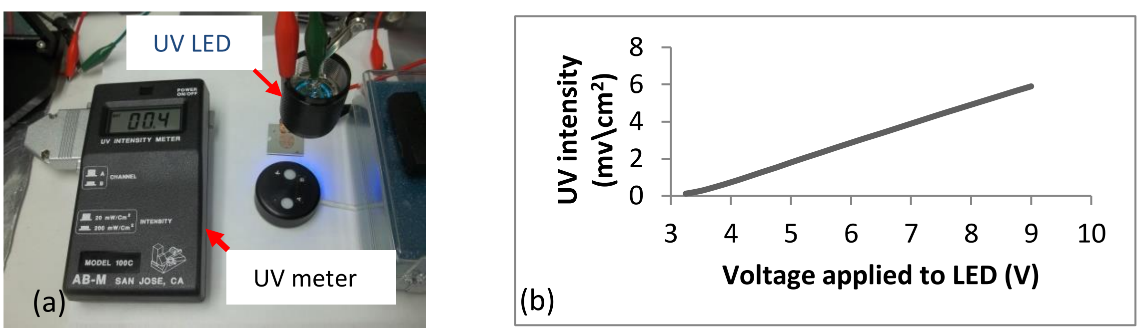


Figure (1): (a) Calibration setup of the UV LEDs. b) voltage-intensity relationship of the UV-LEDs

Figure (2) displays some patterns that were achieved using the torch LEDs as a UV source in the process of photolithography. Sharp patterns were achieved with a minimum line width of around 3 μm. In this experiment the S1813 negative photoresist was spin coated on a Si/SiO_2 substrate and then soft backed at 110 °C for 2 min. The substrate then exposed to the UV torch light for 20s though several masks patterns with various structures. After that, the sample was developed and finally was hard backed at 110 °C for 2 minutes.

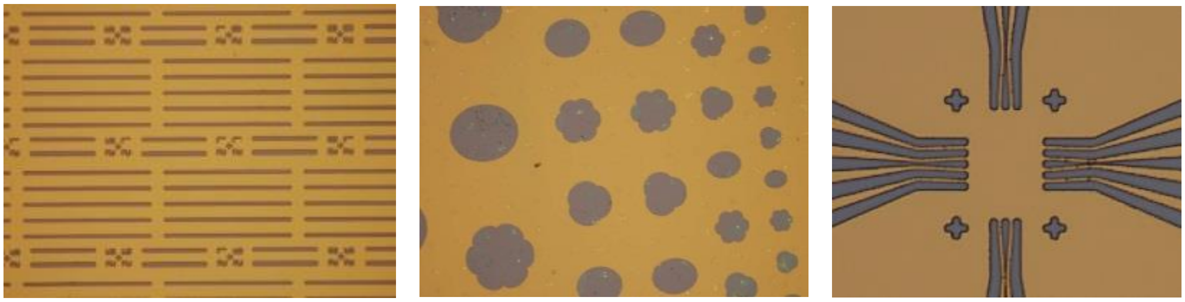


Figure (2) : Results of the photolithography process

b- Fabrication of metal electrodes

After lithography process, thermal evaporator was used to deposit coper metal over the Si/SO_2 substrate. Thus the sample immersed in acetone for 24 h for liftoff. Figure 3 shows the device after liftoff process. The width of the electrode is 5 µm and the spacing between electrodes is 3 µm.

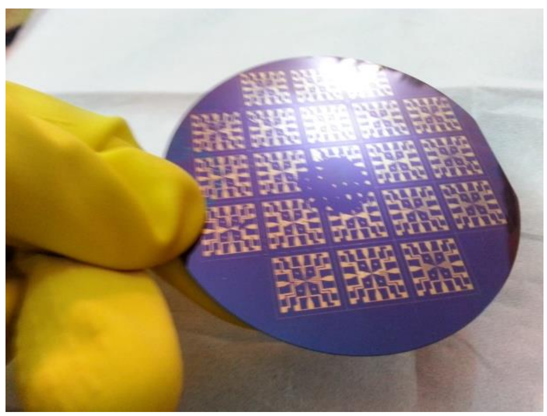


Figure (3) : The Si/SiO_2 wafer after liftoff.

3- Dielectrophoresis

a- Theory of the dielectrophoresis

When CNT subjected to an electric field, a dipole moment is induced. Practically, the electric field is nonhomogeneous, this leads to unequal force acting on each edge of the tube. This makes CNT to move in the medium. Specifically, it could push it towards the zone of high or low electric field perpendicular to the field lines (Dimaki and Bøggild, 2004; Heidari, 2016). When alternating current is applied through two parallel electrodes, an electric field is generating. The corresponding force and motion will remain the same because both dipole moment and electric field will be reversed at the same time.

Induced force by an electric field on a polarizable object can be defined by:

$F = (p \cdot \nabla)E$ ……………………………….(1)

Where,

E: electric field

P: dipole moment

For alternating field, the averaged force on CNT is:

$F_{av} = \Gamma\ \varepsilon_m\ \mathrm{Re}\{K_f\}\nabla|E|^2$ ………………… (2)

Where,

$\Gamma = \pi/6\ r^2\ L$ ………………………………...(3)

R: Radius of the CNT

L: Length of the CNT

ε_m: Permittivity of the medium (real part).

$K_{f:}$ imaginary part of the permittivity of both the CNT and the medium.

Figure 4 illustrates the schismatic diagram of the dielectrophoresis setup.

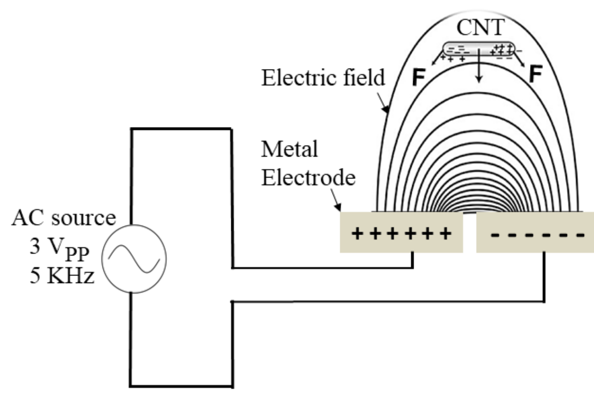


Figure (4): Schematic of Carbon nanotube subjected to dielectrophoresis.

b- Experimental

Single walled carbon nanotubes (SWCNTs) were purchased from cheaptube.com. The purity of the SWCNTs is less than 90 wt % . The following procedure has been used: Little powder of MWCNT was mixed in IPA solvent, then sonicated for around 1 hour. A drop of this CNT+IPA was on the SiO_2/Si substrate which consists of 5 fingers and five pads. 3V ac voltage of 10 KHz was applied through electrodes. When IPA get dried, the electrophoresis means ended.

4- Device testing and testing setup

The device was investigated under scanning electron microscope (SEM) with magnification range ×20k to ×30k. As illustrated in Figure (5), the CNTs located in between the electrodes fingers due to the dielectrophoresis effect.

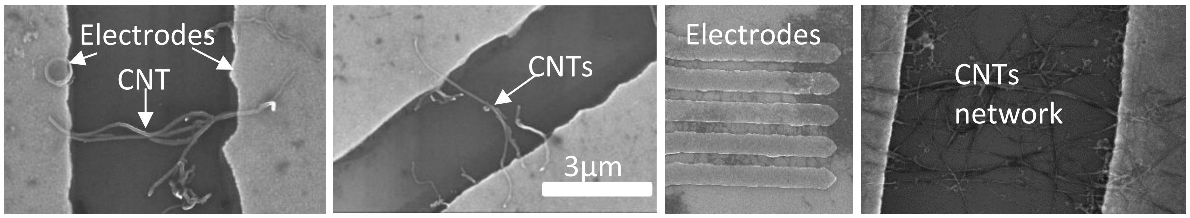
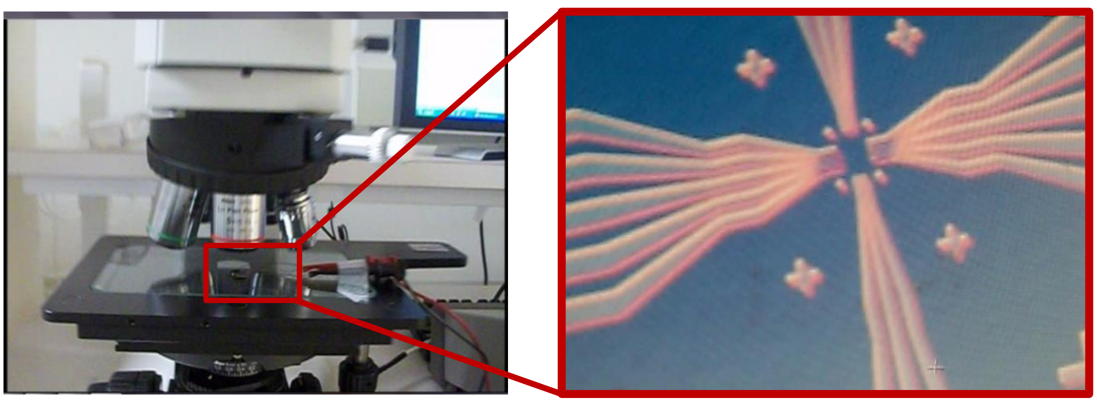


Figure (5): SEM images of the fabricated electrodes (drain-source).

The dielectrophresis process was watched and video recorded under optical microscope (Figure (6).



Figure(6): Dielectrophoresis process under optical microscope vision.

To verify the electronic properties of CNT-FET, the fabricated device was tested by applying a variable gate voltage and keeping drain voltage at a constant value. The source was connected to the ground (Figure 7). The back gate was fabricated by partially etching of the SiO_2 layer using hydrofluoric acid (49%). Then the back gate voltage (V_g) was applied through the Si layer of the substrate, which is show up after etching SiO_2. The device was demostrated by measuring the v_{ds}-I_{ds} relation at various values of gate voltages. Figure 8b shows three fabricated The device gate dependent characteristics of the drain current, representing typical p-type transport behavior of CNTs. Figure 8 (b) displys the current transport charecteristic of the FET. Obevously, increasing of the drain voltage (Vds) lead to elevate in the drain-sourse current (I_{ds}). Aditionally, the location of the Dirac point which is the minimum I_{ds} at a particular value of gate voltage at positive Vg value indicates the P-type semiconducter property of the device. The hole majarity carrires of the CNT-FET can be attributed to the adsobtion of the O_2 molecules in the testing enviroment.

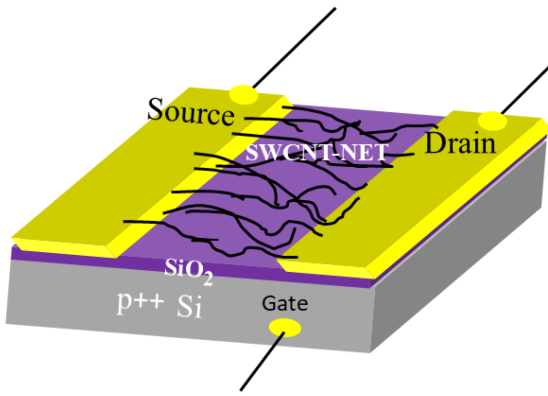
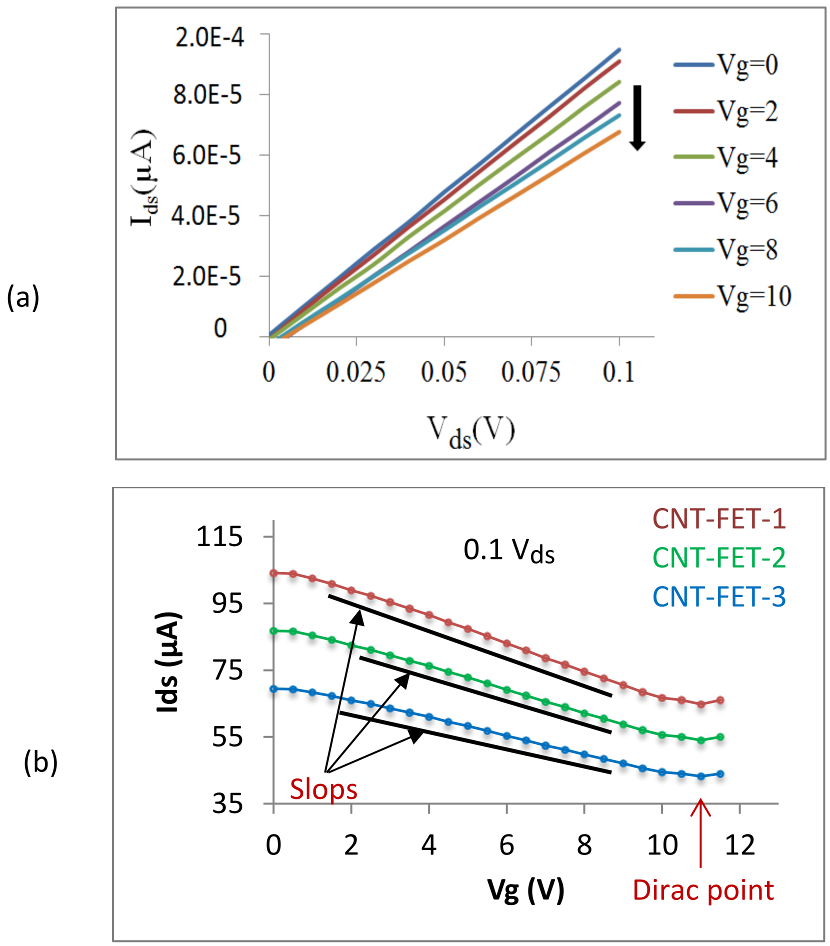


Figure (7): Schematic observes the drain, source and gate of the CNTFET.



Figure(8): Gate-dependent conductivity of CNTs network. (a) V_{ds} Vs I_{ds} relation at different gate voltages. b) V_g vs Ids at V_{ds}=0.1 V.

From transfer current characteristics of an FET one can determine the mobility of the charge carriers (holes) of the fabricated devices. This can be estimated empirically using the slope of the linear part of the conductance versus gate voltage characteristic curve. Figure 8 observes the slope of 3 fabricated devices. For a CNT- FET the following formula can be used to calculate the mobility of the charge carriers.

$\mu = L/C_g\ (dG/dV_g)$………………………..(4)

Where,

L: length of the CNT

Cg: Gate-nanotube capacitance (approximately 69 e -/V·µm), (Dürkop *et.al.*, 2002; Larentis *et.al.*, 2012).

The electron mobility of our fabricated devices was calculated to be in the range of 5000 to 10000 cm^2/Vs at room temperature, which is higher than the mobility of conventional semiconductors. The reason why the practical mobility is lower than the theoretical one is the contamination that usually attach the device during device fabrication.

5- Conclusion

As a conclusion we were designed and fabricated a CNTs field effect transistor based on simple fabrication tools. The electrodes were fabricated using simple photolithography and thermal deposition . Dielectrophoresis was used to lay the CNTs on the electrodes fingers. The device observes p-type semiconductor properties and excellent electron mobility. A video was recorded for the Dielecrophresis effect, which shows the swimming of CNTS in the solvent towards the electrodes.

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