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High Voltage Gain Impedance-Source Indirect Matrix Converter

Abstract- *This paper proposes a high voltage gain indirect matrix converter to eliminate the voltage degradation problems in AC drive. The proposed converter consists of modified LC-C-LC single-phase bridge rectifier combined with a three-phase Z-source inverter. The combined design of LC-C-LC filter with the single-phase diode rectifier is able to step up DC rectified voltage greater than peak AC input voltage without the requirement to active switching devices. In addition, it can also reduce the input current harmonics, improve input power factor and reduce reactive power consuming from AC supply. To further increase boost capability of the proposed converter and eliminate the voltage degradation problems, the LC-C-LC rectifier is combined with a Z-source inverter. This combination not only increase the converter's voltage gain but also reduce the reactive power and converter's size through using small LC-C-LC and Z-source parameters which consequently increase the system's efficiency. A new Modified Space Vector Pulse Width Modulation (MSVPWM) method has been proposed in order to dominate the shoot-through duty ratio of Z-source inverter. This method results in reducing the level of harmonic for the output current and increasing the dynamic range of the shoot-through duration. The overall drive system has been simulated and analyzed using a hybrid simulation between OrCAD/PSpice and Matlab/Simulink environments through using SLPS integration platform.*

Keywords- *LC-C-LC filter, Z-source inverter, a hybrid simulation*.

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1. Introduction

Most of three phase power electronic converters for the machine drives comprise of rectifier for AC to DC transformation, followed by a DC to AC PWM converter with active power electronic switches, which modulate the currents or voltages, delivered to machine. The DC output voltage that can be produced by using the three-phase bridge rectifier, ignoring the diodes voltage drop, changes between 1.65 and 1.73 times the input peak phase voltage. Hence, for 220V AC input system the DC voltage produced by the rectifier is varies between 514 to 538V. This variation depends on the DC link capacitor filter value and the applied load. If the rectifier designed with a ripple free output voltage (using bulky DC link capacitor) and under light load, the peak DC voltage is equal to 538V. Hence, the three-phase rectifier is a buck converter.

Based on the above, using a single-phase rectifier as a front-end converter for the IM drive system results in further reduction in the rectified DC voltage that is applied to the voltage-fed inverter in IMC system. For a single-phase input with 220V RMS, the maximum rectified voltage is roughly equal to 311V for assumption of free ripple with ignoring the voltage drops. Hence, the AC converted line voltage to the motor is less than 218V. This means that more degradation problem will occur leads to increasing the IM rating. Therefore, many research efforts have been focused on developing new converters suitable for IM drive system [1-8]. One of the most promising topologies is the Z-source inverter (ZSI). However, to obtain the required DC voltage by the ZSI system large inductors and capacitors in the Z-Network are required. These parameters are both energy storage devices, so their values should be optimally designed to ensure small size, low cost and low reactive power transfer. The Z-network parameters can be reduced but on the account of using large shoot-through duty cycle duration. Un-optimal design for the Z-network parameters and the shoot-through duty cycle results in a worse effect on the stability of the system. This is because they lead to increasing the non-minimum phase system response which means that the converter will exhibit a right–half–plane–zero (RHPZ). A RHPZ causes a phase lag at low frequencies that limits available bandwidth to control Z-capacitor voltages that leads to a slow dynamic response for converter.

This paper proposed a modified hybrid boosting impedance source IMC which consists of LC-C-LC single phase bridge rectifier combined with a

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three-phase Z-source inverter to eliminate the voltage degradation problems and reduce the input and output currents harmonics of the IMC drive system.

2. Impedance Source Boost Diode Rectifier

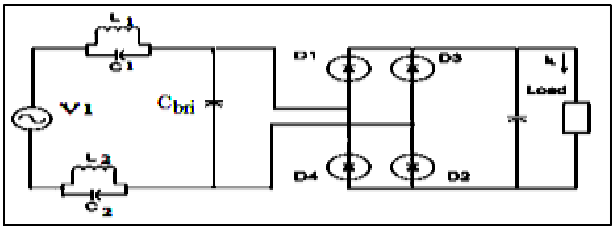
The single-phase diode rectifiers have the problems of poor power quality in terms of injected current harmonics, resultant voltage distortion and poor power factor at input of AC mains. In addition, the rectified DC output voltage ($\frac{2V_{ml}}{\pi}$) cannot exceed the AC input voltage. Therefore, a new passive filter has been proposed in this paper to improve the performance of this rectifier in two terms: enhancing the input and output currents harmonics of the drive system and eliminate the voltage degradation due to the inherent characteristics of the traditional IMC. The configuration of the proposed input filter is shown in Figure 1a. This impedance source filter consists of two series tuned LC filters (L_1, C_1, L_2, C_2) connected for each line of the single-phase grid and one input parallel capacitor (C_{bri}) connected across the bridge rectifier.

For analyzing the new rectifier configuration, it is enough to consider two successive intervals of the operation, as shown in Figure 1b, assuming single-phase voltage is expressed as:

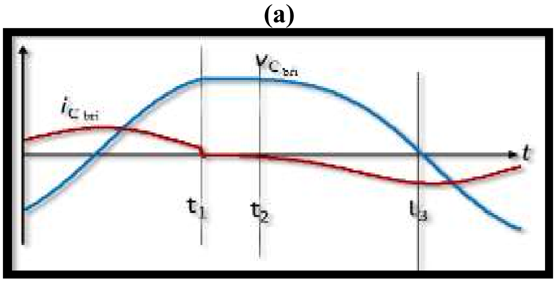
$$v_s = V_{ml}\sin\omega t \quad (1)$$

Interval 1: $t_1 \leq t \leq t_2$, where D_1, and D_2 are conducting. The current across capacitor C_{bri} equal to zero and voltage V_{Cbri} develop equal to V_o until t_3. An equation relating to this interval is:

$$v_s = L_1\frac{di_s}{dt} - L_2\frac{di_s}{dt} - V_o \quad (2)$$



(a)



(b)

Figure 1: Illustration of (a) Proposed Impedance Source Boost Diode Rectifier configuration (b) Voltage and current waveforms through Cbri of the LC-C-LC filter

Interval 2: $t_2 \leq t \leq t_3$, where all the diodes are turned off. The voltage across the parallel capacitor V_{Cbri} starts to discharge less than V_o until reach to zero at $t=t_3$ which causes in an increasing in the capacitor current i_{Cbri}. The LC tuned will operating to smoothing the input current and improving the power factor. The equation relating to this interval is:

$$v_s = L_1\frac{di_s}{dt} - L_2\frac{di_s}{dt} - V_{cbri} \quad (3)$$

Hence, the instantaneous voltage across the parallel capacitor can be given as:

$$v_{cbri} = \sqrt{2}V_s\frac{X_{Cbri}}{X_{Cbri} - 2X_L}\sin\omega t \quad (4)$$

By simplification (4), the voltage across C_{bri} is equal to

$$v_{cbri} = \frac{V_{ml}}{1 - 2\omega^2 LC_{bri}}\sin\omega t \quad (5)$$

From (3) it can be seen that the voltage across C_{bri} which is the input voltage to the rectifier is greater than input AC voltage by the factor equal to $(1/(1-2\omega^2 LC_{bri}))$. As shown in Figure 1b, the rectified output voltage V_o is equal to the v_{cbri} for the lossless rectifier with output ripple free. Thus, the voltage conversion ratio is not equal to the peak of the input voltage V_{ml} but is greater than this peak value by the factor $1/(1-2\omega^2 LC_{bri})$ and changes between $+V_o$,$-V_o$. Hence, the voltage boost factor B_1 of the proposed rectifier is equal to:

$$B_1 = \frac{1}{1 - 2\omega^2 LC_{bri}} \quad (6)$$

where

$\omega = 2\pi f$, and f is the fundamental frequency.

So, this rectifier step up rectified voltage without using active devices. For getting a good reduction in harmonic currents tuned filters L_1C_1 and L_2C_2 are designed to be calculated based on the resonant frequency equation:

$$\omega_{re} = \frac{1}{\sqrt{LC}} \quad (7)$$

3. High Voltage Gain Impedance-Source Indirect Matrix Converter

The Z-source inverter can produce any required voltage gain but on the account of using large Z-inductances/large shoot through duration. Z-source parameters and shoot-through zero states duration have to be optimally selected to maintain low harmonics orders and at the same time achieve the rectified DC link voltage for the drive system.

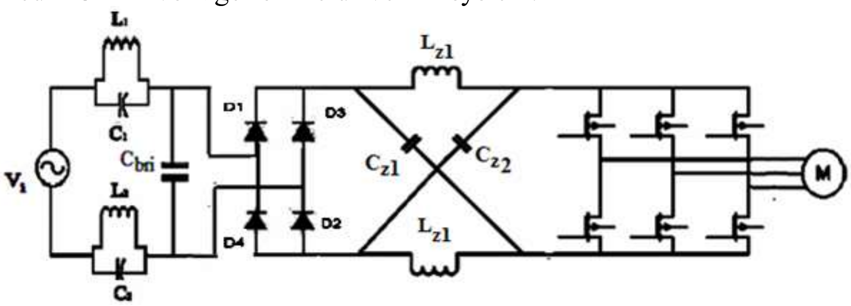
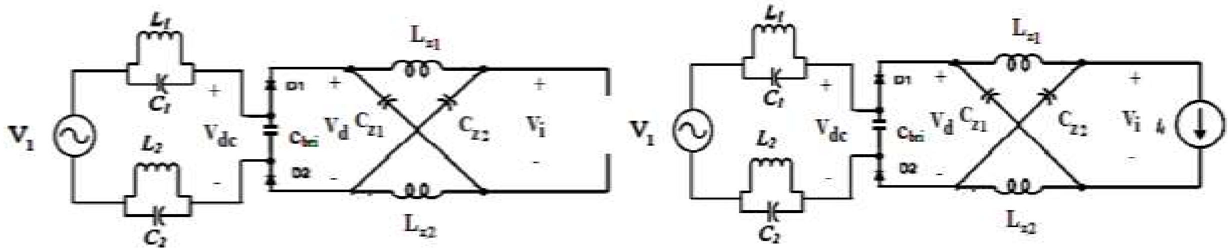
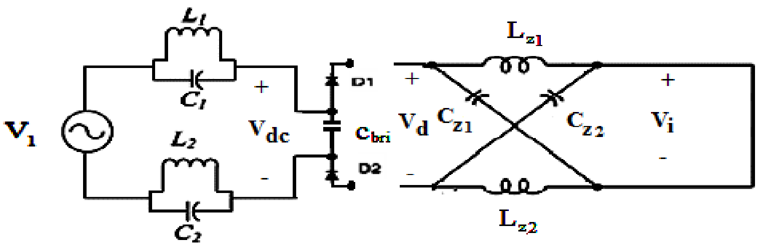


Figure 2: Main circuit configuration of proposed IMC system



(a) Active-state mode (b) Zero-state mode



(c) Shoot-through mode

Figure 3: Equivalent circuit of the proposed IMC in three different states

In the proposed converter, these two issues are considered for further developments to enhance the performance of IMC fed AC drive system. The main circuit configuration of proposed IMC system is shown in Figure 2.

The operation principles of the proposed converter are similar to those of the conventional Z-source converter. The main difference is that the input converter to the inverter is a single-phase rectifier with a modified input filter configuration. The parallel capacitor C_{bri} with one of the diagonal diodes of bridge rectifier is operating as the DC supply for the Z-source network. Hence, since the V_{cbri} is always greater than V_{ml}, as shown in the previous section, the applied DC voltage to the Z-source network is higher than the DC voltage generated by the traditional single phase and even three-phase rectifiers (this depends on the design of the LC-C-LC filter). Thus, small Z-source network parameters can be used which consequently increasing the duration range of the shoot-through zero state and further increase the voltage gain capability of the converter.

The proposed converter can be operated in three modes as described below:

I. Active-State Mode

In this mode, the proposed IMC is operating in one of the six traditional active states. The inverter bridge acts as a current source viewed from the DC link. The equivalent circuit of this state is shown in Figure 3a. The diodes (D_1D_2) conduct and carry currents. The line current will flow through L_1, Lz_1, Lz_2, and L_2. This will lead to further smoothing the input current and reduce the input current harmonics. The Z-source circuit always compels diodes D_1D_2 to conduct and carry the current difference between the Z-source inductor current and inverter DC current.

II. Zero-State Mode

In this mode, the proposed IMC is operating in one of two traditional zero states and shorting through either the lower or upper three devices, thus acting as open circuit viewed from Z-source circuit. The equivalent circuit of this state is shown in Figure 3b. The diodes D_1D_2 conduct and carry currents thus in this mode the input current harmonics remains in reduction mode.

III. Shoot Through Zero State Mode

In this mode, the proposed IMC is operating in one of the seven shoot-through states. In this mode, the bridge rectifier is separated from the AC line. The line current still has low harmonics orders since the tuned impedance input source L_1C_1 and L_2C_2 will be operated on that reduction. Figure 3c describe this state. This means unlike traditional rectifier, there is no zero current interval in the input line current and the rectifier operates in this mode in a continuous conduction mode. The shoot-through state to be utilized in each switching cycle through the conventional zero state period is produced by PWM control. According to how much a voltage boost is wanted, its duty cycle (T_{sh}/T_z) or the shoot-through interval (T_{sh}) is determined.

With traditional single-phase 220V bridge diode rectifier, the generated DC voltage that will be seen by the Z-source network is about 311 V. With the proposed converter, the generated DC voltage is always bigger than 311V depending on the designed factor B_1. As B_1 increases this means increase in the input LC-C-LC parameters. Hence, an optimal selecting for these parameters has been accomplished to obtain the required DC voltage with the lower input impedance parameters and Z-network parameters. This optimal design is also considered using a small shoot-through zero states using a modified SVPWM to reduce the inverter output current harmonics. However, the boost factor which is generated using the Z-source inverter can be found using the following equation (8) [1].

$$B_2 = \frac{T_z}{(T_{nonsh} - T_{sh})} \quad (8)$$

where

T_{sh} is the Shoot-through time.

T_z is switching time.

T_{nonsh} is non shoot-through time.

Finally, the total boost factor which is generated using the proposed IMC can be found using the following equation:

$$B_t = B_1 + B_2$$

$$B_t = \frac{1}{1-2LC_b\omega^2} + \frac{T_Z}{(T_{nonsh}-T_{sh})} \quad (9)$$

Hence, this high voltage gain feature gives wide range in obtaining the required output voltage with low passive components values and contributes to harmonics reduction and eliminates the voltage degradation problem.

4. Implementation of Modified Space Vector Pulse Width Modulation for Z-Source Inverter (MSVPWM)

Traditional space vector control strategy has to be changed to distribute the shoot-through states into the zero vectors without compromise to the active space vector [9]. The traditional SVPWM has eight space-vectors. This vector is utilized in (MSVPWM), but with extra shoot-through period additional to conventional SVPWM's switching time. The addition can step up DC link voltage. The zero voltage periods T_0 would be reduced to produce a shoot-through time T_{sh}, whilst the active state times T_1, T_2 remain constant. Through the shoot-through period, both switches of the phase leg are together connected for increasing the DC capacitor voltage.in this paper three methods have been developed to modify the MSVPWM [10].

I. First method ($MSVPWM_1$)

In this method, the shoot- through state has been distributed as shown in Table 1. By using this method, the Z-source inverter can enhance the boost voltage, but the total harmonic distortion of the output current will be increased.

II. Second method ($MSVPWM_2$)

In this method, the zero time is reduced as shown in equation (10),

$$T_0 = (Tz - (T_1 + T_2))/16 \quad (10)$$

Hence, the shoot-through period represents all the zero time as shown in Table 2.

By using this method, the Z-source inverter can enhance the boost voltage and the total harmonic distortion is lower than in method 1, but this is on the account of the stability of the output voltage.

Table 1 Vector distribution for MSVPWM $_1$

$T_0/4-T_{sh}$	T_{sh}	$T_1/2$	$T_2/2$	T_{sh}	$T_0/2-2T_{sh}$	T_{sh}	$T_2/2$	$T_1/2$	T_{sh}	$T_0/4-T_{sh}$

Table 2 Vector distribution for MSVPWM $_2$

$T_0/4$	$T_1/2$	$T_2/2$	$T_0/2$	$T_2/2$	$T_1/2$	$T_0/4$

Table 3 Vector distribution for MSVPWM

$T_0/2\text{-}(1/2)\,T_{sh}$	$(1/3)T_{sh}$	T_1	T_2	$(1/3)T_{sh}$	$T_0\text{-}T_{sh}$	$(1/3)T_{sh}$	T_2	T_1	$(1/3)T_{sh}$	$T_0/2\text{-}(1/2)T_{sh}$

III. Third method (MSVPWM$_3$)

In this method, the zero time is reduced based on equation (10) and the shoot-through state has been distributed as shown in Table 3. The shoot-through state is divided into four parts. The aim of this distribution is to obtain the required voltage gain with the lower output current harmonics. Figure 4 shows the generated PWM based on the improved MSVPWM.

5. Hybrid Evaluation Approach

The ability to trade-off between simulation speed and model fidelity is a critical issue for efficient improvement prior to building of a practical converter system. The PSpice program is a quite appropriate to simulate power electronic circuits which contain non-linear transformers, switching devices and other non-linear elements. However, it is less appropriate for control system simulation because of potential convergence difficulties. In addition, simulating control system in PSpice may need a large amount of time for analysis. On the other hand, Matlab/Simulink is a quite powerful program for control engineering. However, it is less appropriate for accurate modelling of power electronic circuit characteristics. So, to get around this problem, a hybrid evaluation approach has been used in this work based on integrating the converter model in PSpice with MSVPWM in Simulink, utilizing SLPS integrated simulation platform. Moreover, for further improvement in the speed time of the simulation, all the modelled parts that required long time simulation have been implemented using a Matlab Function Block. This block is available in Simulink where the Matlab function can be added to the Simulink models. Thus, Matlab coding algorithms have been implemented instead of using a graphical language of Simulink which could results in increasing time simulation.

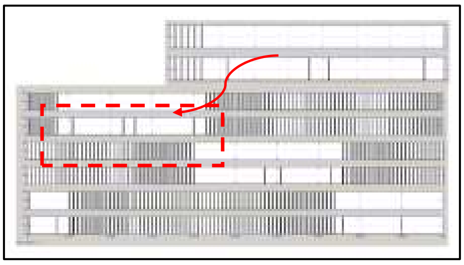


Figure 4: SVPWM signals applied to the Z-source inverter's switch

I. Simulation Verification of the Proposed LC-C-LC Boost Rectifier

The designing of the single-phase LC-C-LC impedance source rectifier represents the first step for designing the proposed high voltage gain impedance-source indirect matrix converter. The simulation of the LC-C-LC impedance source rectifier has been performed by using OrCAD/PSpice program version 16.6 as shown in Figure 5. The values of the inductances and capacitances for the LC-C-LC impedance source rectifier were calculated using equations (6&7) as $L_1 = L_2 = 5mH$, $C_{series1} = C_{series2} = 81\mu F$ and bridge capacitor is $C_{bri} = 275\mu F$ for a line frequency of 50Hz.

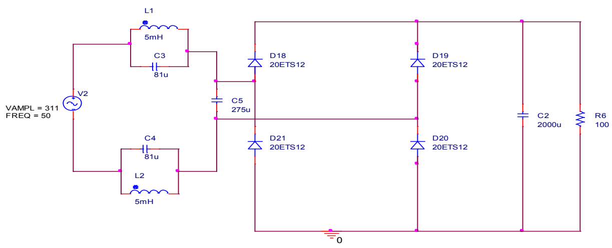


Figure 5: PSpice model for the LC-C-LC impedance source rectifier

The AC input voltage and the DC output voltage for the LC-C-LC impedance source rectifier are shown in Figure 6. It can be noted from this figure that the rectified DC voltage is greater than the peak value of the AC input voltage (>311V). That means the proposed impedance source rectifier is a boost converter without to need for active switching devices in contrast to the traditional rectifier which is a buck converter. This will result in reducing the voltage degradation significantly when this rectifier is used as a front-end converter for the AC drive system.

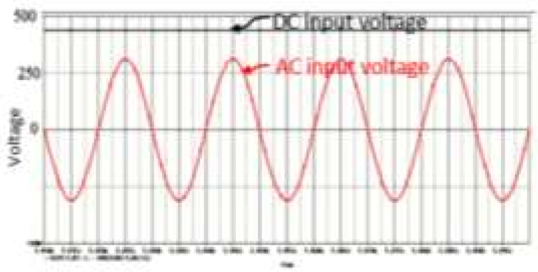
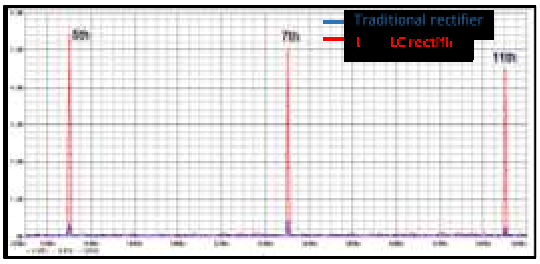
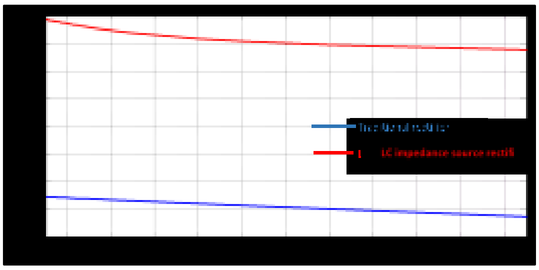


Figure 6: The AC input voltage and DC output voltage for the LC-C-LC impedance source rectifier

Furthermore, it was found through extensive analysis that this rectifier not only operates as a boost converter but also shows a high degree of enhancement in the harmonic reduction of AC line current. Figure 7 shows the 5^{th} and 7^{th} and 11^{th} harmonic levels of the proposed rectifier in comparison to conventional one. Figure 8 show output voltage of traditional and LC-C-LC impedance source rectifiers at variable load. It can be seen from this figure that the rectified voltage is boosted by 30%-40% above the peak line voltage. In addition, the simulation results show that the new topology results in overall harmonic levels of less than 2%; in particular, the 5^{th} and 7^{th} harmonic current is greatly reduced as shown in Figure 9.



Figures 7: The level of ac 5_{th}, 7_{th} and 11_{th}harmonics for the input current



Figures 8: Output voltage of traditional and LC-C-LC impedance source rectifiers at variable load.

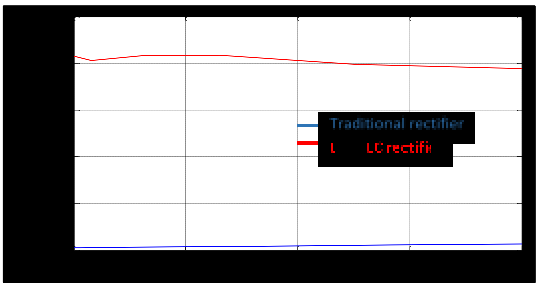


Figure 9: Comparison of input current THD for the proposed and traditional rectifiers at different loads

II.Proposed IMC System Performance

For evaluating improvement achievable with proposed IMC which is used to drive a 2.2kW, 308V IM, the detailed drive system has been simulated utilizing SLPS simulator. Here, the proposed IMC circuit is simulated in PSpice, while, the IM model, the MSVPWM algorithm, and measurement circuits have been modelled in Simulink, as displayed in Figure 10. The simulation in has also been performed when the rotor speed is 150 rad/sec.

Figure 11 shows output line voltages of proposed IMC.It's clear from this figure that the produced phase-phase voltage is boosted to 380V that leads to enable the IM operate at full load. This boosting in the AC output voltage has been achieved with using low Z-source network inductors and shoot-through duration in contrast to the traditional ZSI that requires either increase in shoot-through duty cycle or increasing the Z-source inductors to obtain the required boost voltage. Figure 12 shows the output phase voltage of the proposed IMC.

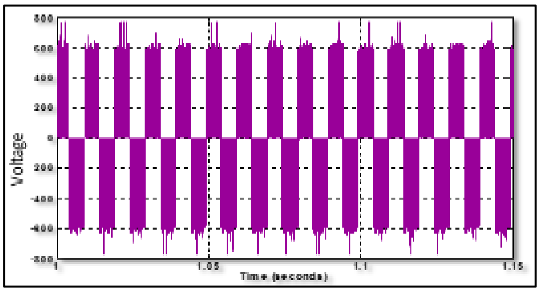


Figure 11: Output line voltages of proposed IMC

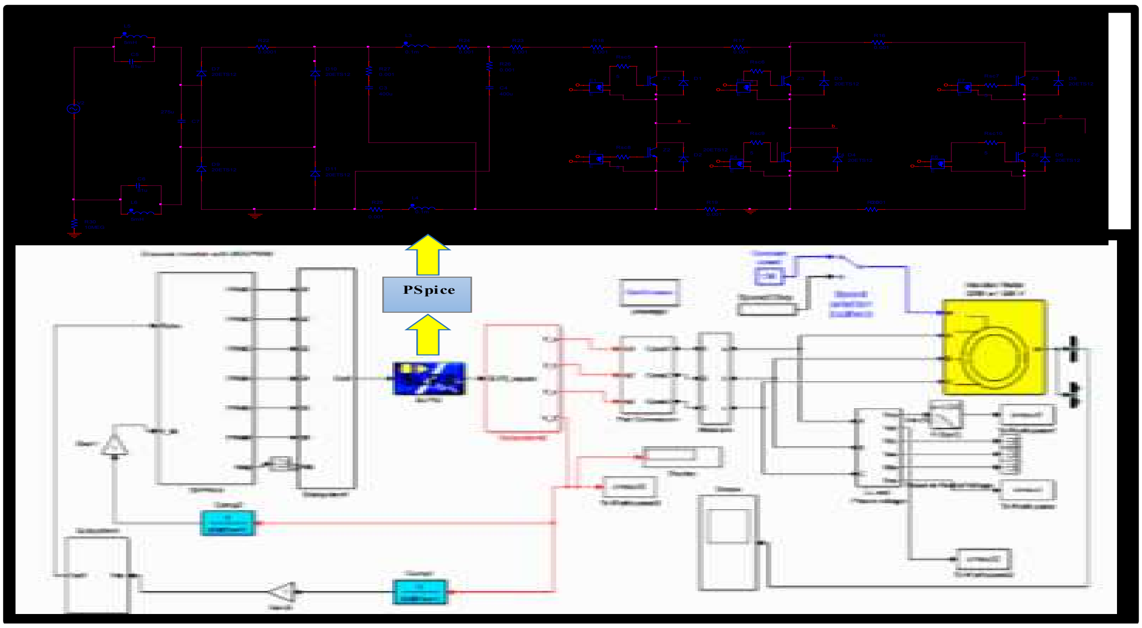


Figure 10: The simulation model of the high voltage gain impedance source IMC

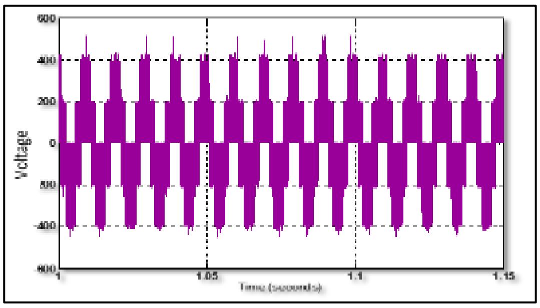


Figure 12: Output phase voltage of the proposed IMC

As it is known that the harmonics is responsible for on temperature increasing of the motor due to the induced eddy currents in different frequencies which are multiples of the fundamental frequency. These eddy currents are the cause of iron losses and are proportional (losses) with the square of frequency of eddy current. Because of the non-sinusoidal shape of the motor current waveform due to the inverter switching, this current must be analyzed to investigate the harmonics content.

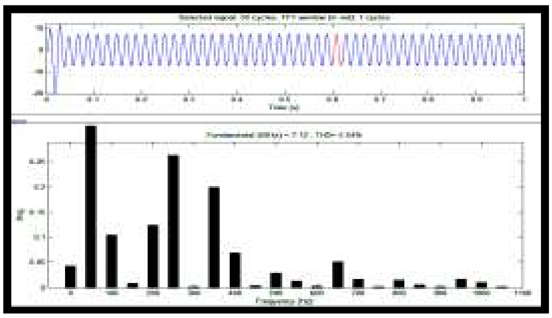


Figure 13: Harmonics analysis of output current for traditional IMC

The total harmonic distortion of the motor current has been measured by using the Powergui block from a Matlab program as shown in Figure 13. The measuring of THD is performed up to 20th and the system is tested under motor rated command speed equal to 150 rad/sec.

6. Conclusion

The main inferences from this work are summarized below:

1. The proposed IMC system has been eliminated the degradation problems in AC drive system that can be results in reducing the rating capability of the adjustable drive system. With the proposed system, a high voltage gain is realized not only by using the Z-source inverter but also through using a single-phase rectifier. In contrast to the traditional indirect matrix converter, the proposed system operating as a boost converter in the rectification and inversion modes.
2. Compared to the traditional Z-source inverter system, the proposed converter requires a smaller inductance value and can be produced a same voltage gain of the traditional IMC with a smaller shoot-through duty ratio. Thus, results in obtainable a lower voltage stress on the power switching devices.
3. The proposed converter can be implemented with a lower weight, a lower reactive power and a smaller size, which results consequently in increasing the converter's efficiency.
4. Due to using a small shoot-through duty ratio an improving in the power quality of the drive

system has been achieved, where the generated input and output current harmonics orders in the developed system is smaller than a traditional system.

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