Circuit Design and Implementation of Dental System Controller Based on FPGA

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Abstract:

In this paper, a hardware circuit was designed and implemented for controlling the time of dental curing system by using VHDL as a design tool and the FPGA as target technology to create a counter.

The control was achieved by designing a card containing seven segment, halogen lamp and buzzer and connect these component with FPGA .The time which needed for curing to towel was controlled automatically by preset value which was input from a push –button switch. Buzzer signal used to state that the needed time of counter is over and the device was stopped from the operation.

The design is implemented in a Spartan-3E Starter Kit. The speed of counter can be controlled by using the clock divider of the kit (50 MHz) to the quite clock to get the necessary delay between the numbers of counter.

The advantage of using FPGA is its performance which is supported with hardware parallelism , flexibility, reliability and long time maintenance.

Keywords: FPGA, seven segment, dental curing system.

المستخلص:

في هذا البحث تم تصميم وتنفيذ دائرة سيطرة، بمكونات الكترونية مادية للسيطرة على زمن منظومة حشوة أسنان باستعمال لغة (VHDL) كوسيلة للتصميم وبمصفوفة بوابات تبرمج حقليا (FPGA) كهدف تقني لتوليد العداد.

أنجزت السيطرة بتصميم بطاقة تحوي مصباح هلوجين،جرس والقطع السبعة وتم ربطهم مع مصفوفة بوابات تبرمج حقليا بحيث إن الزمن المطلوب لتجفيف الحشوة سيطر عليه ذاتيا عن طريق قيمة مسبقة يتم إدخالها عن طريق مفتاح زرٍّ دفعٍ،كذلك تم استخدام إشارة صوت أو تنبيه لتبين إن الوقت المطلوب لتجفيف الحشوة قد انتهى والجهاز توقف عن العمل.

نفذ التصميم بطاقم (Spartan-3E Starter Kit، بحيث يمكن السيطرة على سرعة العداد باستعمال مقسم عداد الطاقم (clock divider) ذي التردد (50 MHz) للعد الفعلي وللحصول على تأخير بين أرقام العداد.

تكمن فائدة استعمال (FPGA) بفاعليته المعززة بالتنفيذ المتوازي، المرونة، الثقة وطول فترة الصيانة.

الكلمات المفتاحية: FPGA، شريحة سبعة، ونظام علاج الأسنان

1-Introduction

A dental curing light is a piece of dental equipment that is used for polymerization of light cure resin based composites. It can be used on several different dental materials that are curable by light. The light used falls under the visible blue light spectrum. This light is delivered over a range of wavelengths and varies for each type of device. There are four basic types of dental curing lights; the Tungsten halogen and light-emitting diode (LED),plasma arc curing (PAC), and laser. The two main dental curing lights are the halogen and LED [Sherwood, 2010].(Ali hussein hamed) control of dental system by using microcontroller [Ali , 2006].

In this paper, FPGA is used for fast implementation and quick hardware verification. A major benefit of using FPGAs is the fact that different architectural variations can easily be tested and evaluated on real applications.

FPGAs have the capability of being programmed on the fly to perform a specified algorithm. They can be programmed and reprogrammed as many times as the user wishes in order to achieve the desired result [Younis, 2007].

Xilinx Spartan-3E is used for implemented the design. VHDL is a hardware description language used for programming the control of the time of cure light of dental by using counter display in seven segment. The key advantage of VHDL

when used for systems design is that it allows the behavior of the required system to be described (modeled) and verified (simulated) before synthesis tools translate the design into real hardware (gates and wires) [Vrinda *et al.*, 2008].

The simulation of this program is shown in this paper.

2- 7-Segment LED

The LED7SEG User Module is capable of multiplexing up to eight 7-segment displays. This user module is compatible with common cathode, common anode, or any drive polarity (in this paper using common anode). This allows a wide range of flexibility with various displays. Digits and segments may be driven directly by PSoC pins without the use of transistors or drivers as long as the current sinking and sourcing limits of the PSoC pins are not exceeded [San , 2011].

The following diagram shows how common anode and cathode7-segment displays are configured:

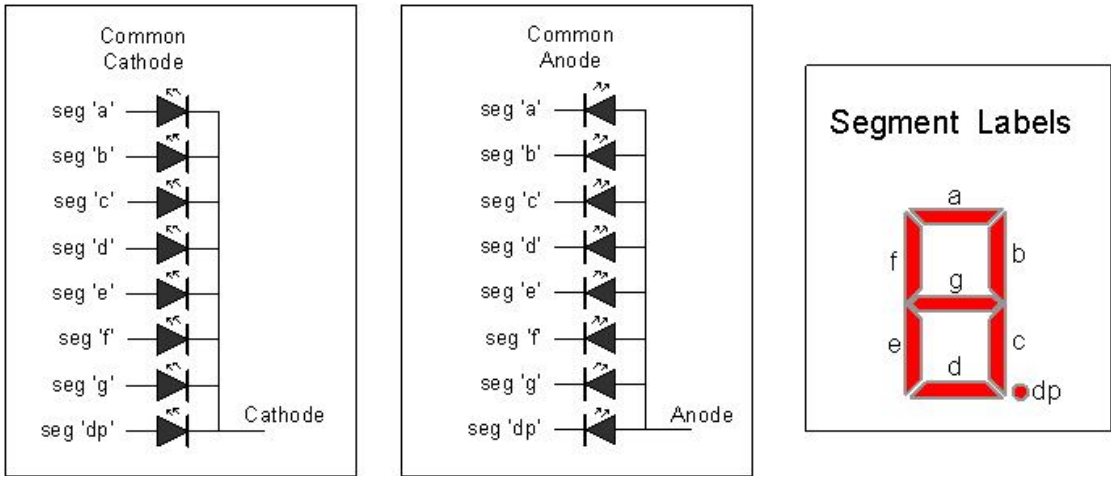


Figure (1) 7-Segment Display Configurations

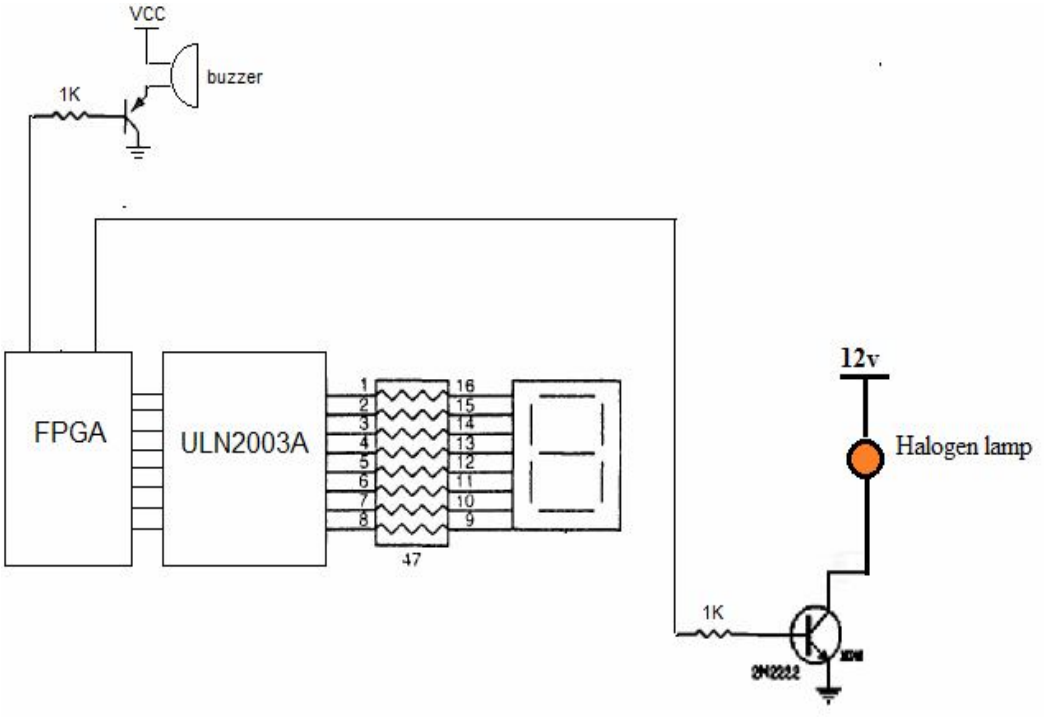
3-How Multiplexing Works

When 2 or more displays are multiplexed, only one digit is on at a time, although to the eye it appears that all digits are on continuously. To achieve this illusion, the rate at which the displays are turned on and off must be higher than the response of the human eye. For a four digit display, the multiplex rate should be near 1 kHz; for an eight digit display the multiplex rate should be double that, or 2 kHz. When multiplexing an N-digit display, each digit is bon for 1/N of the total time. For example, for a system with 8 digits and a refresh rate of 2 kHz (500 uS period), each display is on for 500 uSec every 4 mSec (8 digits * 500 uSec/digits) [San , 2011].

4-The driver circuit

The Drive circuit of 7-segment consist of ULN2003A chip which is switched on and switched off by the sequence come from the output pins of the Spartan-3E Starter Kit. The VHDL program sends the specified codes to the output pins to display the digit on 7-sgment display.

It is necessary to choose resistor values have to allow 60mA of current flow per segment. This circuit use 47Ω resistors[BARY , 2003]. Also using driver for halogen lamp and buzzer with type of transistors.



Figure(2) Halogen lamp,buzzer,7-segment interfaced to FPGA

5-FPGA Design Flow

The Integrated Software Environment (ISE) is the Xilinx design software suite that allows taking the proposed design from design entry through Xilinx device programming. The ISE Project Navigator manages and processes the proposed design through the following steps in the ISE design flow. Block diagram of the FPGA design flow is shown in Fig.(3) [Xilinx, 2007].

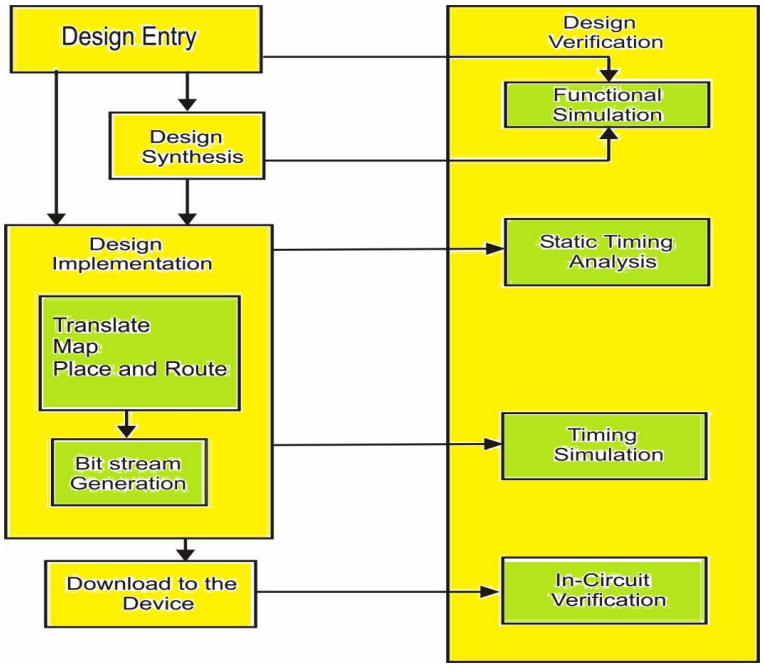


Figure (3) FPGA Design Flow

6-Spartan-3E: the target board

Xilinx XC3S500E Spartan-3E FPGA with package of 320-pin has some features such as 50MHz clock oscillator, eight discrete LEDs,four slide switches,three Digilent 6-pin expansion connectors and rotary- encoder with a push-button shaft [UG230 2008].

In this work the output (sequence signals for counter) from FPGA kit are used to drive the ULN2003A chip through header J1 and J4 witch used to output the value of voltage to 7-segment ,each output pin is connected to one of the ULN2003A pins Fig. (4) shows the header J1,J2,J4,also other signals output from the header are used to fit the driver of buzzer and halogen lamp. Fig.(5) show the practical connection circuit.

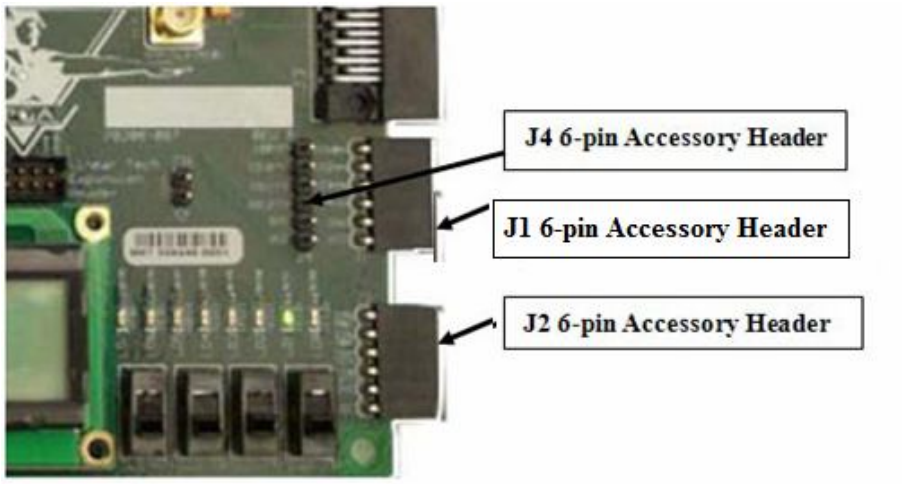


Figure (4) Headers J1, J2, and J4

The User Constraint File (UCF) location of these pins are shown below

```
# ==== 6-pin header J1 ====

#NET "J1<0>" LOC = "B4" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 6 ;
#NET "J1<1>" LOC = "A4" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 6 ;
#NET "J1<2>" LOC = "D5" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 6 ;
#NET "J1<3>" LOC = "C5" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 6 ;

# ==== 6-pin header J2 ====

#NET "J2<0>" LOC = "A6" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 6 ;
#NET "J2<1>" LOC = "B6" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 6 ;
#NET "J2<2>" LOC = "E7" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 6 ;
#NET "J2<3>" LOC = "F7" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 6 ;

# ==== 6-pin header J4 ====

#NET "J4<0>" LOC = "D7" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 6 ;
#NET "J4<1>" LOC = "C7" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 6 ;
#NET "J4<2>" LOC = "F8" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 6 ;
#NET "J4<3>" LOC = "E8" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 6 ;
```

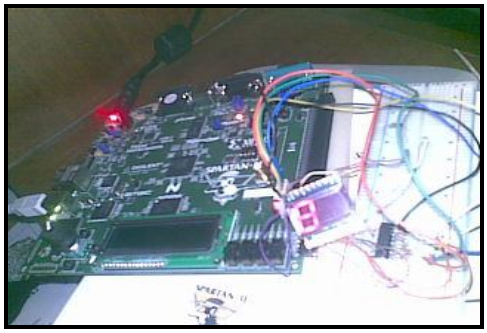


Figure (5) Practical circuit

The speed of the counter was been controlled by using clock divider to divide the clock of FPGA which has a value of 50MHz to the required frequency as shown in these instruction:

```
Process (clk, clk_divider)
begin
if clk'event and clk='1' then
clk_divider<=clk_divider+1;
end if;
slow_clk <=clk_divider(i);
end  process;
```

The output clk_divider [0] has a frequency half of the clock frequency, the output clk_divider [1] has a frequency half of clk_divider [0], etc. Thus, a counter can be used to divide the frequency f of a clock, where the frequency of the output clk_divider (i) is [Richard E. Haskell, Darrin M. Hanna 2009]

$$f_i = f_{clk} / 2^{(i+1)} \quad \text{.....(1)}$$

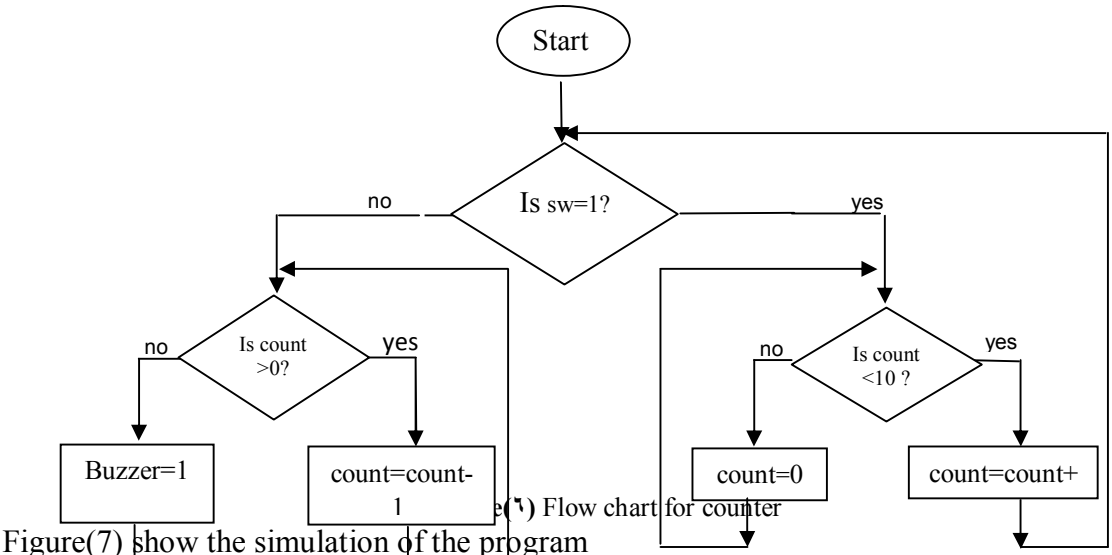
f_{clk}: FPGA clk(50MHz).

The frequencies and periods of the outputs of a 24-bit counter driven by a 50 MHz clock are shown in Table 1.

Table 1 Clock divide frequencies

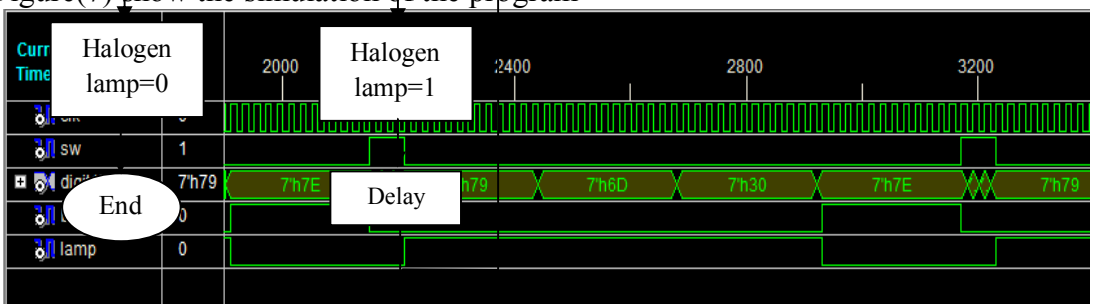
clk_divider [i]	Frequency (Hz)	Period (ms)
I	50000000.00	0.00002
0	25000000.00	0.00004
1	12500000.00	0.00008
2	6250000.00	0.00016
3	3125000.00	0.00032
4	1562500.00	0.00064
5	781250.00	0.00128
6	390625.00	0.00256
7	195312.50	0.00512
8	97656.25	0.01024
9	48828.13	0.02048
10	24414.06	0.04096
11	12207.03	0.08192
12	6103.52	0.16384
13	3051.76	0.32768
14	1525.88	0.65536
15	762.94	1.31072
16	381.47	2.62144
17	190.73	5.24288
18	95.37	10.48576
19	47.68	20.97152
20	23.84	41 .94304
21	11.92	83.88608
22	5.96	167.77216
23	2.98	335.54432

One push button switch is utilized for counting purpose, by pressing the switch the seven segments will display the time in seconds, each press will increase the time 10-second such as if this switch is pressed in one, the count will be in 10sec and for each iteration the time will doubled until reach 90sec.When the press of the push button switch is release the count at seven segment began decrease with one until zero, each decrement has time 10 seconds. The light of halogen lamp become at ON state when the seven segment not equal to zero i.e. when the counter is in counting state and when the counter end from counting the lamp is become in OFF state and the buzzer signal become at logic one. Figure (6) represents the flow chart of these processing.



Figure(7) Flow chart for counter

Figure(7) show the simulation of the program



Figure(7) simulation of program

Table (2) The device utilization summary

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	22	9,312	1%	
Number of 4 input LUTs	56	9,312	1%	
Total Number of 4 input LUTs	56	9,312	1%	
Number of bonded IOBs	11	232	4%	
IOB Flip Flops	2			
IOB Latches	7			
Number of GCLKs	1	24	4%	

7. Conclusions:

The most important results of this study for the purpose of controlling of light curing in dental system are:

1. The Usage of FPGA, provide the small size of the system.
2. The full reliability of the control card comparing to its relatives.
3. VHDL language makes the changes on the design easier to be carried out.
4. The design can be modified easily and quickly without need to change hardware components.
5. The control card of the early equipment is semi-mechanical.
6. The most sophisticated control card that is in use is designed with the digital design techniques.
7. The resources used from the FPGA in this design was not exceeded the 4% of the total kit used.

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