Design and Implementation of Forward Link Channel CDMA2000-1x System Based on SDR Using FPGA

Hadi T. Ziboon ***Alaa Y. Eisa***
University Of Technology/ Electrical Eng. Department / Baghdad / Iraq.

Abstract

This paper is proposed an enhancement for forward link channel of CDMA2000-1x system by using 32QAM and 64QAMbased on SDR technology by using FPGA. The Simulink HDL Coder has been used for converting the MATLAB-Simulink models to VHDL language. The verification of the generated VHDL code has been done using Altera- ModelSimprogram, while the synthesis reports and board programming files have been obtained using the Quartus IIprogram. System implementation has been done using FPGA technology with Altera Cyclone II boards. The implementation of the forward link channel by using Simulink HDL coder shows feasibility and flexibility in solving the problem of complex multiplication of complex spreading code also the practical results were closed to that obtained from ModelSimprogram. The results show that the forward link channel of CDMA2000 with 32QAM and 64QAM is a suitable technique to increase the data rate up to 2Mbps in the presence of AWGN and Rayleigh fading channel. However the results of simulation for forward link channel of CDMA2000 system shows improvement when using three levels of codes (LPNC, Walsh code and complex coding) within (0.5-3.2) dB in the presence of AWGN and Rayleigh fading channel. MATLAB (2009) is used for simulation of the proposed system in the presence of AWGN and Rayleigh fading channel.

***Keywords*: CDMA, SDR, FPGA, LPNC.**

الخلاصـة

أقترح هذا المنشور تحسين لقناة الوصلة الامامية لتقسيم الشفري لتعدد الوصولية (CDMA-2000) باستعمال تقنية التضمين المتعامد الكمي-32 (QAM-32) والتضمين المتعامد الكمي-64 (QAM-64) بالاعتماد على البرمجيات المعرفة راديويا (SDR) باستعمال مصفوفة البوابات المنطقية الواسعة (FPGA). تم استخدام مشفر لغة الكيان المادي الكتلي (Simulink HDL coder) لغرض تحويل (MATLAB-Simulink models) اللغة (VHDL). تمت عملية التحقق من الكود باستخدام برنامج (ModelSim-Altera) اما نتائج البناء وعملية تحميل البيانات وملفات البرمجة تمت باستخدام برنامج (Quartus II). تم بناء النظام باستعمال تقنية مصفوفة البوابات المنطقية الواسعة (FPGA) معAltera Cyclone II board. بناء قناة الوصلة الامامية بواسطة استعمال مشفر لغة الكيان المادي الكتلي (Simulink HDL coder) الذي بين ملائمة ومرونة من خلال حل مشكلة الضرب المعقد لشفرة الانتشار المعقدة وكذلك كانت النتائج العملية مقاربة لما تم الحصول عليه من برنامج (ModelSim).اثبتت النتائج بانقناة الوصلة الامامية في التقسيم الشفري لتعدد الوصولية (CDMA-2000) مع (QAM-32) و (QAM-64) هي تقنية مناسبة لزيادة معدل سرعة نقل البيانات وبحدود (2Mbps) بوجود الضوضاء والخفوت. علاية حال نتائج محاكاة قناة الوصلة الامامية لنظام التقسيم الشفري لتعدد الوصولية (CDMA-2000) بينت وجود تحسين بحدود (0.5-3.2) dB بوجود الضوضاء والخفوت عند استعمال ثلاث انواع من الشفرات (الشفرة الطويلة للضوضاء المزيفة (LPNC), شفرة Walshوالتشفير المركب).تما ستخدام برنامج(MATLAB - 2009) لمحاكات النظام المقترح بوجود الضوضاء والخفوت.

1. Introduction

The basic cellular system consists of mobile stations, base stations, and a switching center. Each mobile communicates via radio with one or more base stations. A call from a user can be transferred from one base station to another during the call (Abu-Rgheff, 2007).

In IS-95 CDMA standard, user data from a vocoder at 9.6Kbps or 14.4Kbps are spread to 1.2288Mcps (chips per second). Retrieval of the original narrowband information is possible only if the spreading sequence is known. CDMA technique is more secure and ensures more privacy than the other 1G and 2G techniques. IS-95

supports various optional features, such as Short Message Service (SMS), voice mail, caller Identifier Defined (ID) (Abu-Rgheff, 2007).

In 1998, the IS-95B standardization adopted a framework that combined the different vendor's proposals and later became known as CDMA2000. Qualcomm was the first company to succeed in developing a practical and cost-effective CDMA2000. CDMA2000 is a family of 3G mobile technology standards, which use CDMA channel access, to send voice, data, and signaling data between mobile phones and cell sites. The set of standards includes: CDMA2000-1x, CDMA2000-EV-DO, CDMA2000-EV-DV, and CDMA2000-3x (Khan, 2005). However, implementation of CDMA system with flexibility remains the main problem to born the practical system. Thus Software Defined Radio (SDR) is used to implement and develop CDMA2000 system.

In 2006, MathWorks introduced Simulink HDL Coder, which automatically generates synthesizable Hardware Description Language (HDL) code from models created in the company's widely-used Simulink and Stateflow software. The product produces target-independent Verilog and VHDL code and test benches for implementation and verification by using FPGA. Simulink HDL Coder accelerates the design, implementation, and verification of hardware, by providing a path directly from system models to programing FPGA. Simulink HDL Coder also generates Verilog and VHDL test benches that enable reusing system simulation data for verification of the implemented design (Mathwork Inc., 2011).

2. Proposed System Design

The proposed design procedure for Forward Fundamental Channel (FFCH) - Direct Sequence (DS) -CDMA2000 - Single Carrier(1x) is shown in figure (1).Table (1) shows the proposed design parameters of the system. The main parts of the proposed system are in the following sections.

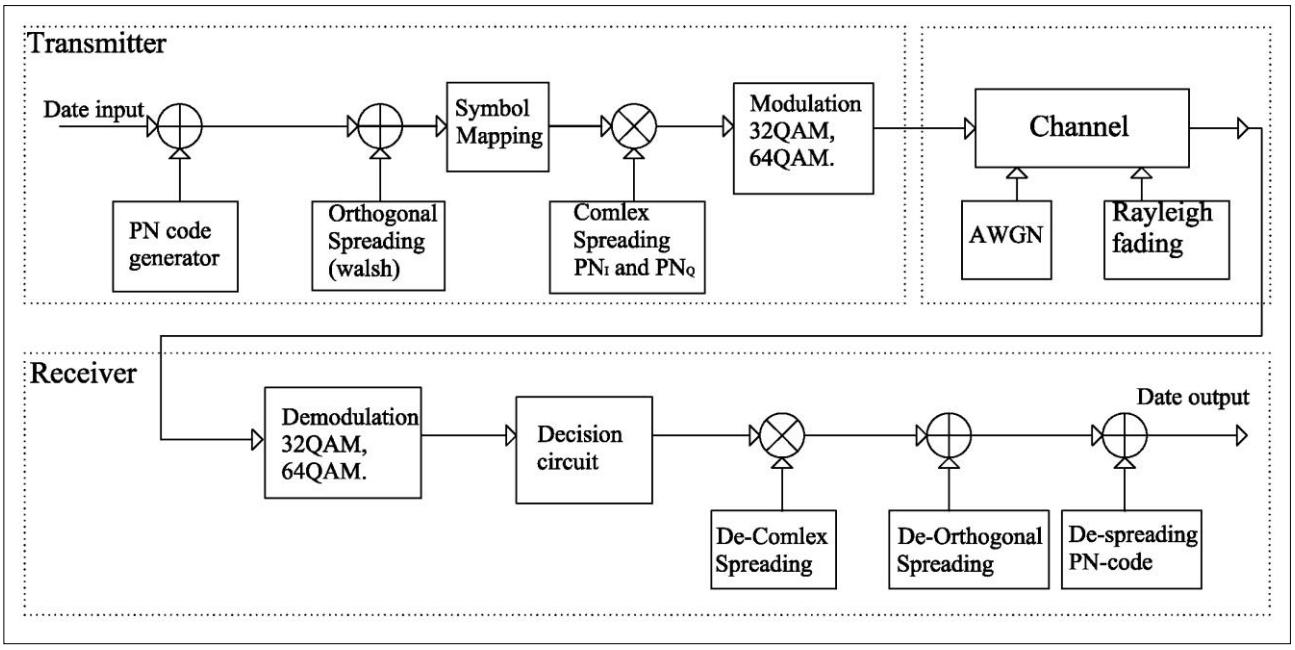


Figure (1): Block diagram of the proposed system.

Parameter	Selected types or values	Comment
Modulation type	32QAM and 64QAM	Used in this system to increase the data rate of transmission
Intermediate Frequency (IF)	10MHz	Moderate frequency can be used to implement SDR system
Bandwidth	1.25MHz	standard of CDMA2000-1x
Data rate	9.6kbps - 2Mbps	
Doppler Frequency (DF)	5Hz - 230Hz	This value is compatible for CDMA2000
Multiplier	PDF-type	PDF is chosen to provide error signal phase and frequency
Arm filter	Raised Cosine Filter	Suitable filter for CDMA
Decision circuit.	Soft decisions	
Long PN code	$2^{42}-1$	1.2288Mp/s
Walsh code	256	1.2288Mp/s
PN_I and PN_Q	$2^{15}-1$	1.2288Mp/s

Table (1): Design parameters goals.

2.1 Long PN Code Design

Pseudorandom-Noise (PN) sequences or Maximal Length Sequence (MLS) are used to spread the data to be transmitted for forward channel. Mobile Stations (MS) also use these sequences to identify Base Stations (BTSs) within the network. The long code is generated by a 42-stage shift-register circuit chips described by the polynomial p(x), ($2^{42}-1$ Chips) and the transmission rate of this sequence are 1.2288 Mcps(Xia, 2005).

$$P(x) = x^{42} + x^{35} + x^{33} + x^{31} + x^{27} + x^{26} + x^{25} + x^{22} + x^{21}x^{19} + x^{18} + x^{17} + x^{16} + x^{10} + x^{7} + x^{6} + x^{5} + x^{3} + x^{2} + x + 1 \quad (1)$$

2.2 Walsh Code Design

Walsh sequences are often referred to as Walsh codes. The Walsh matrix is a square matrix equal (number of elements in rows and columns with the exception of the first row and column) of binary elements, (0s) and (1s) or (+1s) and (-1s). Walsh matrices for any orders can be generated as follow (Angelis, 2010):

$$W_N = 0\ ,\ W_{2N} = \begin{pmatrix} W_N & W_N \\ W_N & \overline{W}_N \end{pmatrix} \quad (2)$$

$$W_0 = 0,\ W_2 = \begin{pmatrix} W_0 & W_0 \\ W_0 & \overline{W}_0 \end{pmatrix}, W_4 = \begin{pmatrix} W_2 & W_2 \\ W_2 & \overline{W}_2 \end{pmatrix}, W_8 = \begin{pmatrix} W_4 & W_4 \\ W_4 & \overline{W}_4 \end{pmatrix}, W_{16} = \begin{pmatrix} W_8 & W_8 \\ W_8 & \overline{W}_8 \end{pmatrix}$$

$$W_{32} = \begin{pmatrix} W_{16} & W_{16} \\ W_{16} & \overline{W}_{16} \end{pmatrix}, W_{64} = \begin{pmatrix} W_{32} & W_{32} \\ W_{32} & \overline{W}_{32} \end{pmatrix}, W_{128} = \begin{pmatrix} W_{64} & W_{64} \\ W_{64} & \overline{W}_{64} \end{pmatrix}, W_{256} = \begin{pmatrix} W_{128} & W_{128} \\ W_{128} & \overline{W}_{128} \end{pmatrix}$$

.

In this work the length Walsh matrix is (256×256), and the transmission rate of this sequence is 1.2288 Mbps that means the sequence has a repetition rate of 4800 times per second [1228800 /256 = 4800 times/s]. However, CDMA2000 systems use Walsh codes of variable lengths, for addressing the data.

2.3 Short Code Design ($PN_I$and PN_Q)

The short code is generated by a 15-stage shift-register circuit ($2^{15}-1$) chips arranged to produce the polynomials given by equations (3) and (4). Each of the circuits generates 32767 chip long sequences (2^N-1) composed of 16384 '1s' and 16383 '0s'. However, an external circuit inserts an additional chip '0' into each sequence after reading a set of 14 consecutive 0s, which happens only once on a complete set of 32767 chips. The transmission rate of these sequences is 1.2288 Mcps and that the sequence is 32768-chip long, the sequence has a repetition rate of 37.5 times per second (1228800/32768 = 37.5 times/s). Figure (2) shows complex spreading by using short code PN_I and PN_Q(Xia,2005).

$$PI(x) = x^{15} + x^{13} + x^9 + x^8 + x^7 + x^5 + 1 \quad (3)$$

$$PQ(x) = x^{15} + x^{12} + x^{10} + x^6 + x^5 + x^4 + x^3 + 1 \quad (4)$$

PN_I and PN_Q sequence modulate all logical channels in the forward link, therefor serving as time reference for synchronization acquisition between base station (BS) and mobile station (MS) these sequences, also, are used to identify all BSs within the network.

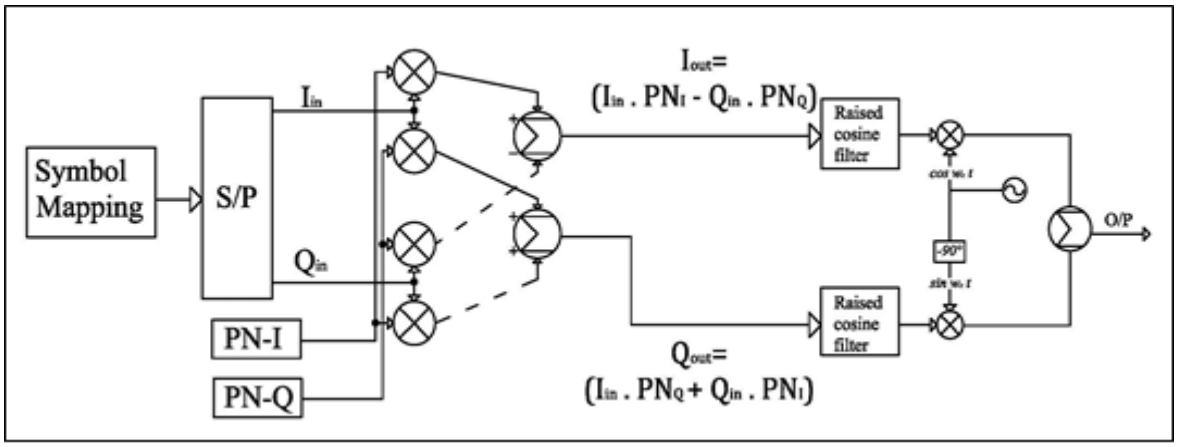


Figure (2): Complex spreading.

2.4 Digital Arm Filter Design

The raised-cosine filter is a filter frequently used for pulse-shaping in digital modulation due to its ability to minimize Inter Symbol Interference (ISI). Its name stems from the fact that the non-zero portion of the frequency spectrum of its simplest form (β=1) is a cosine function, raised up to sit above the *f* (horizontal) axis. The raised-cosine filter is an implementation of a low-pass Nyquist filter. This means that its spectrum exhibits odd symmetry about, 1/2T where T is the symbol period of the communications system. The impulse response of the filter is given by:

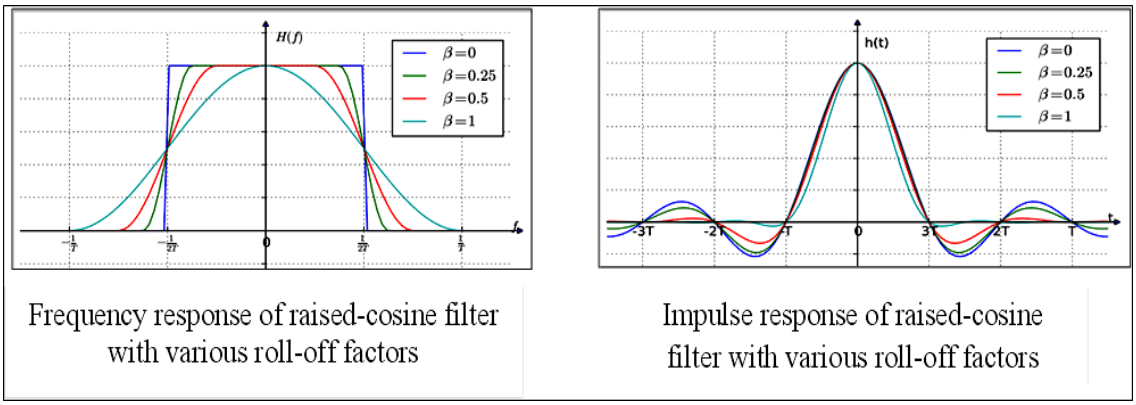
$$h(t) = \text{sinc}\left(\frac{t}{T}\right)\frac{\cos\left(\frac{\pi\beta t}{T}\right)}{1-\frac{4\beta^2t^2}{T^2}} \quad (5)$$

The roll-off factor (β) is a measure of the excess bandwidth of the filter, i.e. the bandwidth occupied beyond the Nyquist bandwidth, the excess roll-off factor as:

$$\beta = \frac{\Delta f}{(\frac{1}{2T})} = \frac{\Delta f}{R_s/2} = 2T\Delta f \qquad (6)$$

whereR_s is the symbol rate andΔf is the bandwidth, figure (3) shows the amplitude response as is varied between 0 and 1, and the corresponding effect on the impulse response. As can be seen, the time-domain ripple level increases as decreases. This shows that the excess bandwidth of the filter can be reduced, but only at the expense of an elongated impulse response (Goldsmith, 2005).

Figure (3): Amplitude response of the raised cosine filter.



Frequency response of raised-cosine filter with various roll-off factors

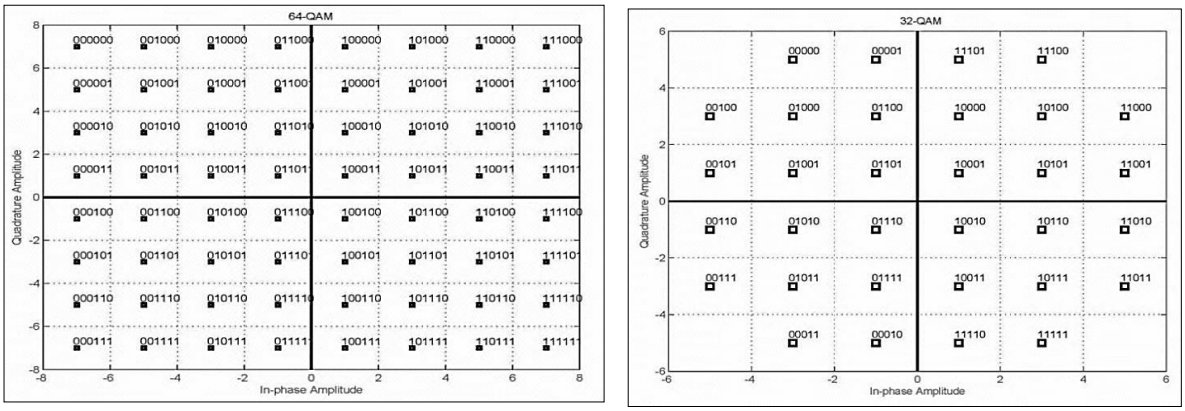
Impulse response of raised-cosine filter with various roll-off factors

2.5 M-QAM System Design

Multilevel Quadrature Amplitude Modulation (M-QAM) is used to obtain higher spectral efficiency, which potentially results in higher throughput of packetized data. In QAM modulator both the amplitude and the phase of the bandpass signal will be changed, thus QAM can be considered as the combination of PSK and ASK occur at the same time (Jain, 2002).

QAM transfer data by changing some aspects of a carrier signal, or the carrier wave, in response to a data signal. In the case of QAM, the amplitude of two waves, 90 degrees out-of-phase with each other (in quadrature) is changed (modulated) to represent the data signal. The variable constellation size means that the number of bits per symbol is also variable. The number of bits that can be sent per symbol is given by N, in a constellation is related to total levels (M) as N = log (2) M. Figure (4) shows constellation of 32QAM and 64QAM (Jain, 2002). Figure (5) shows M-QAM transmitter block diagram in CDMA2000 and figure (6) shows M-QAM receiver block diagram in CDMA2000.

Figure (4): Constellation diagram of 32 and 64QAM.



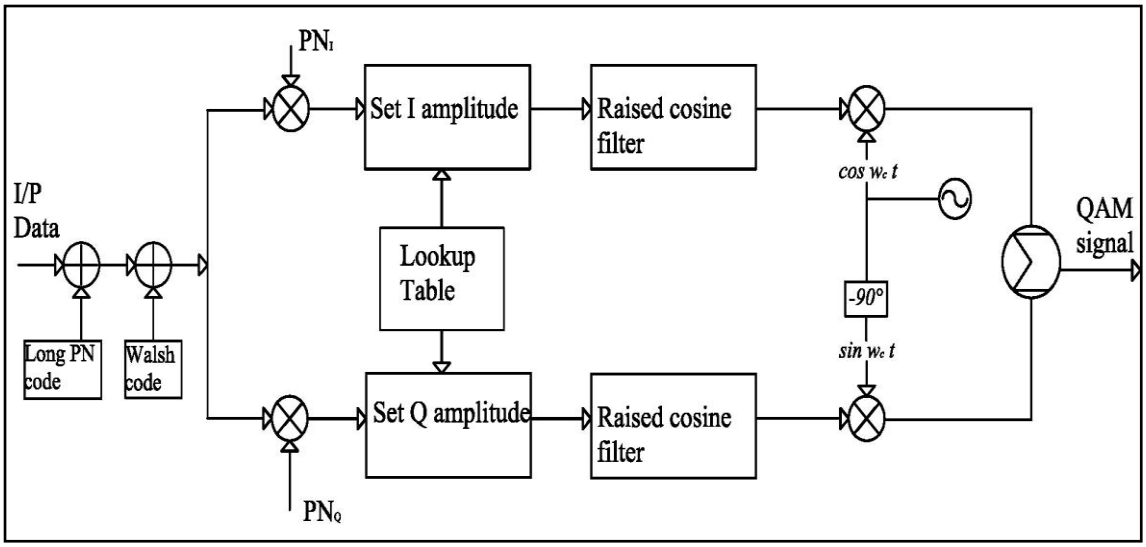


Figure (5): Block diagram of M-QAM transmitter with spreading code.

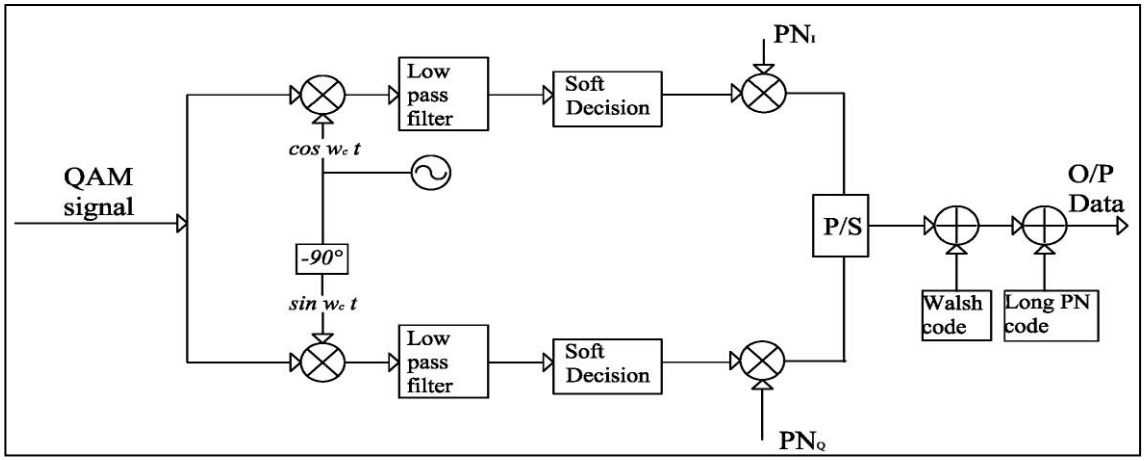


Figure (6): Block diagram of M-QAM receiver with de-spreading code.

2.6 Decision Circuits

The probability of error depends on the characteristic of decision circuit. There are two types of decision circuit hard and soft. In Hard Decision Decoding (HDD) each coded bit is demodulated as 0 or 1, the demodulator detects each coded bit (symbol) individually. The received symbol is decoded as 1 if it is closer to $\sqrt{E/2}$ (Eis energy per bit) and as 0 if it is closer to $-\sqrt{E/2}$. Soft decision is the second method of implementation in which the detector outputs a multilevel voltage and the channel decoder bases its output on these inputs. Soft decision provides about 2-3db coding gain over hard decision but increases the system cost because it requires an error correction code which means more complication and more cost(Naif,2009). Soft decision is chosen for detection M-QAM signals.

3. Simulation Results

In this work the performance simulation of the proposed CDMA2000 system was established in the presence of Additive White Gaussian Noise (AWGN) and Rayleigh fading channel. Different modulation types are used (32QAM and 64QAM) in the proposed system to increase the data rate up to 2Mbps. A MATLAB (2009) is

used in the simulation and performance evaluation of the proposed system. Figure (7) shows the flowchart of the designed system.All blocks in the flowchart are presented in the object oriented program,in order to select each block separately according to the requirement.

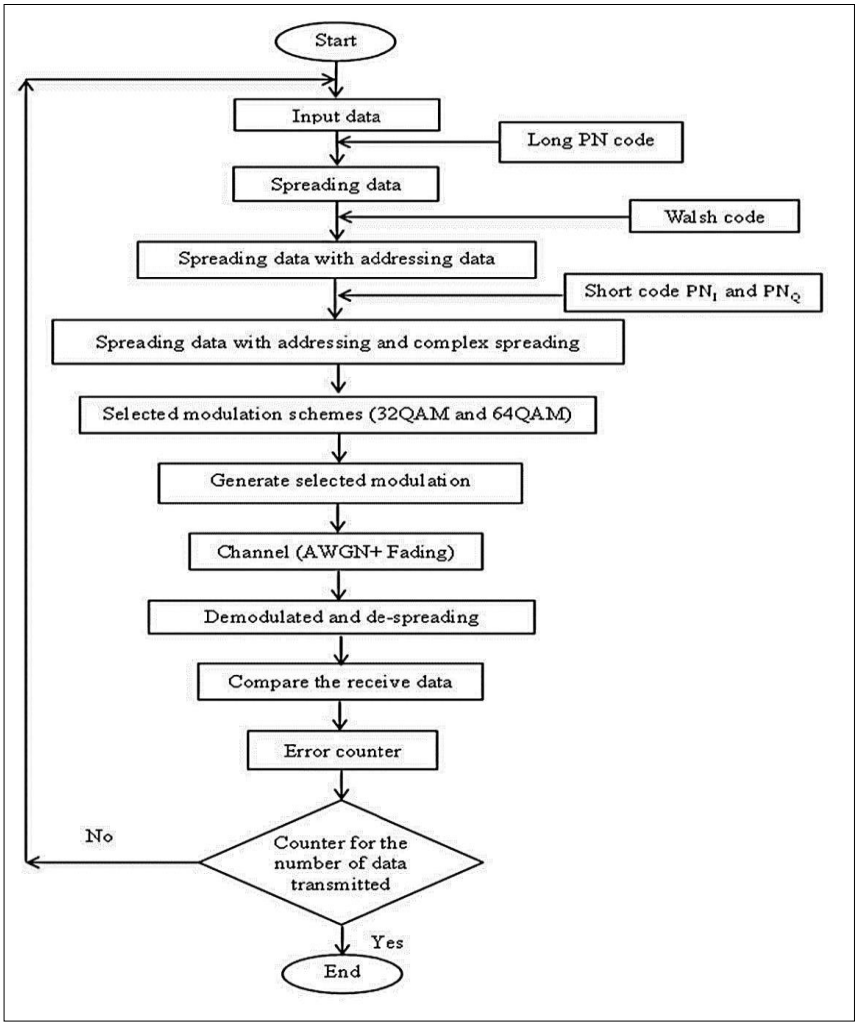


Figure (7): Flowchart of the designed system.

3.1 Simulation Results for the Proposed System without Codes

This simulation includes the performance evaluations of the different modulation / demodulation schemes which are used in the proposed system (32QAM and 64QAM) with AWGN and Rayleigh and all programs are written in (m-file). In this stage of the simulation and the variation of the Bit Error Rate (BER) with variation ratio for energy of data bit to the power spectrum density (E_b/N_o) are performed. Figure (8) shows the performance of modulation over AWGN and figures (9 and 10) show the performance of modulation with (32QAM and 64QAM) over AWGN and Rayleigh fading channel with different values of Doppler Frequencies.

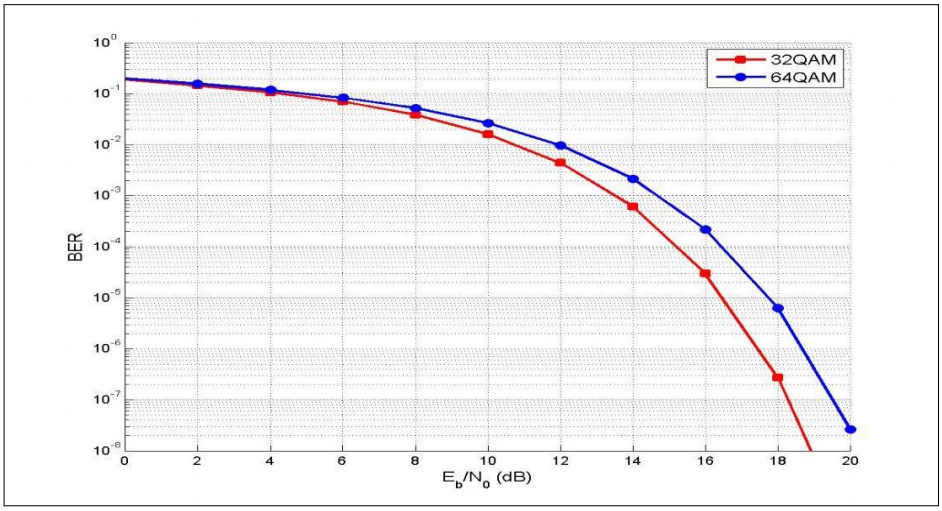


Figure (8): Performance of different modulation schemes over AWGN.
Figure (9): Performance of 32-QAM over AWGN and Rayleigh fading.

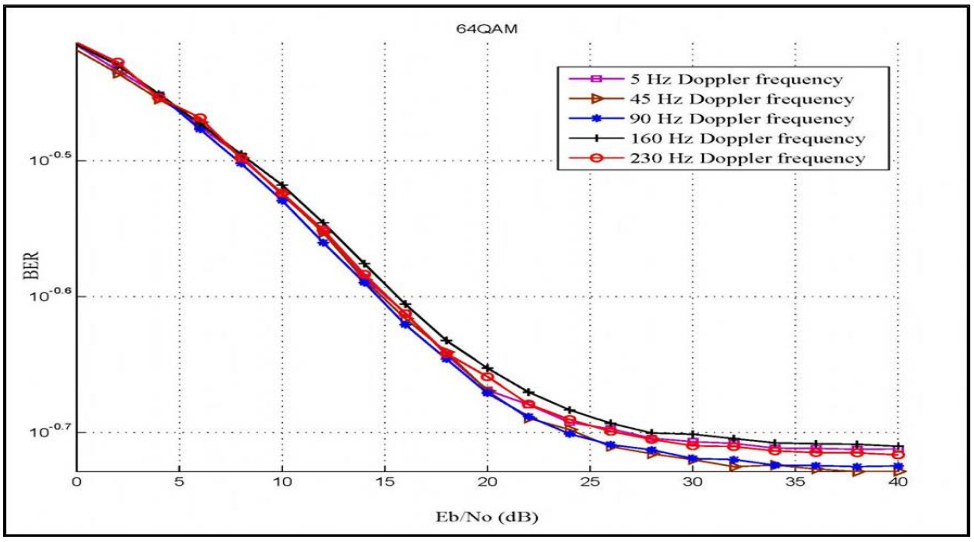


Figure (10): Performance of 64-QAM over AWGN and Rayleigh fading.

3.2 Simulation Performance of CDMA2000 with 32-QAM in the Presence of AWGN and Rayleigh Fading Channel.

The performance of CDMA2000 using 32-QAM modulation system will be evaluated by plotting the BER versus the (E_b/N_o) in the presence of AWGN and Rayleigh fading for different values of Doppler frequencies. Figure (11) shows the effect of AWGN over 32- QAM modulation and figure (12) shows the effect of AWGN and Rayleigh fading channel on the system.

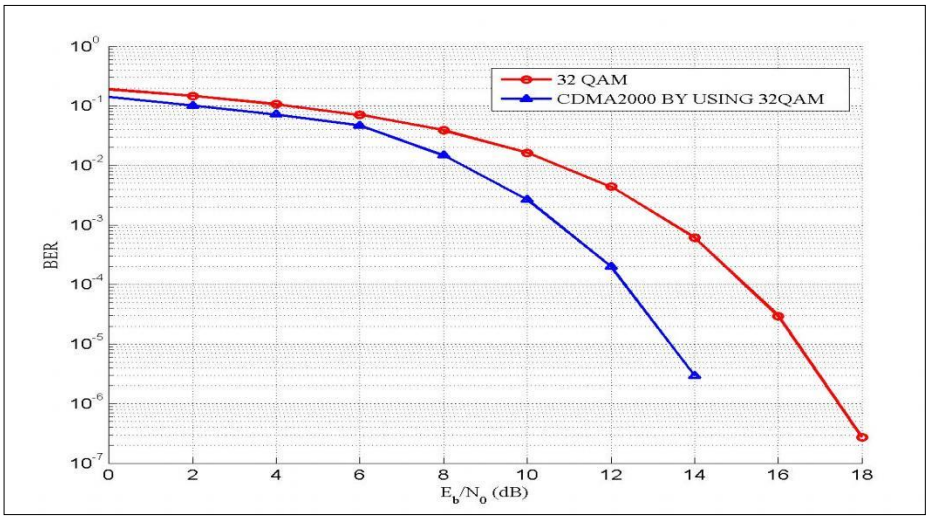


Figure (11): Simulation results of CDMA2000 over AWGN with 32QAM

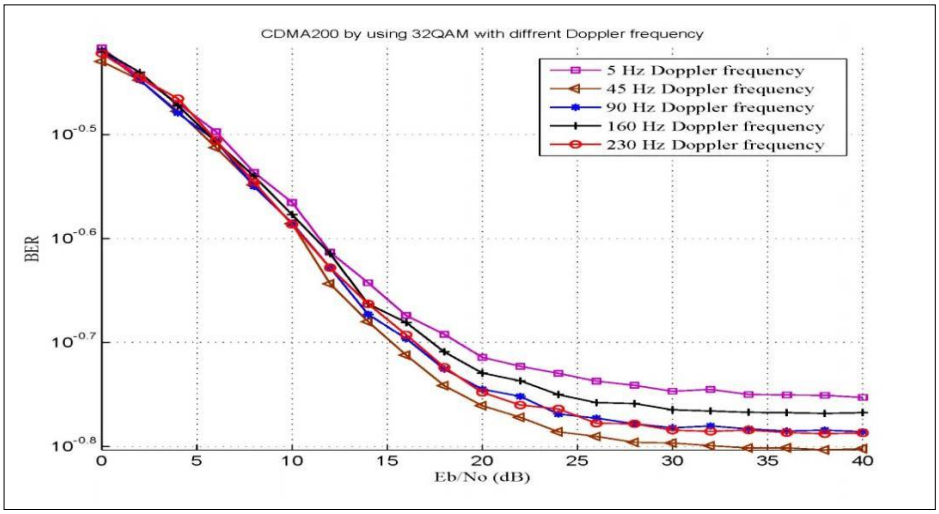


Figure (12): Simulation results of CDMA2000 by using 32-QAM over AWGN and Rayleigh fading.

3.3 Simulation Performance of CDMA2000 with 64-QAM in the Presence of AWGN and Rayleigh Fading Channel.

The performance of CDMA2000 using 64-QAM modulation system will be evaluated by plotting the BER versus the (E_b/N_o) in the presence of AWGN and Rayleigh fading for different values of Doppler frequencies. Figure (13) shows the effect of AWGN over 64-QAM modulation and figure (14) shows the effect of AWGN and Rayleigh fading channel on the system.

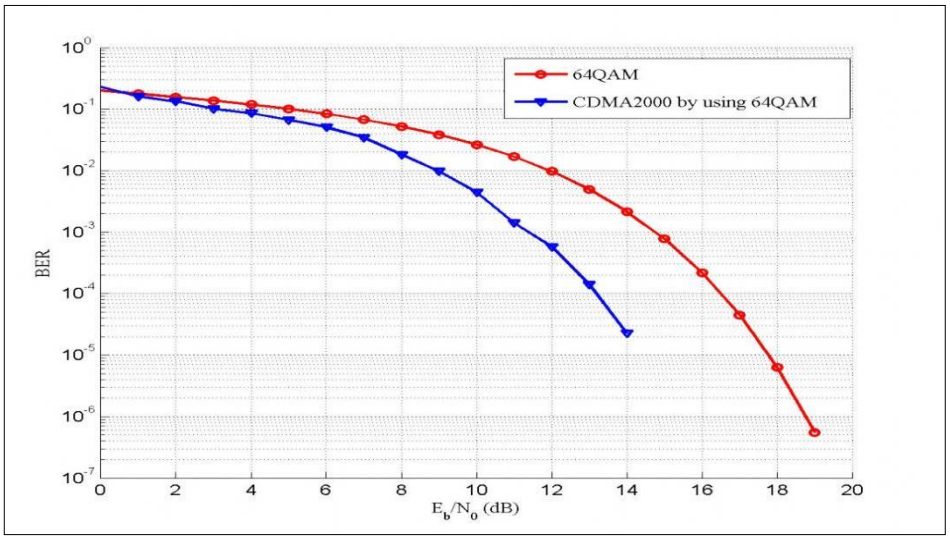


Figure (13): Simulation results of CDMA2000 over AWGN with 64QAM.

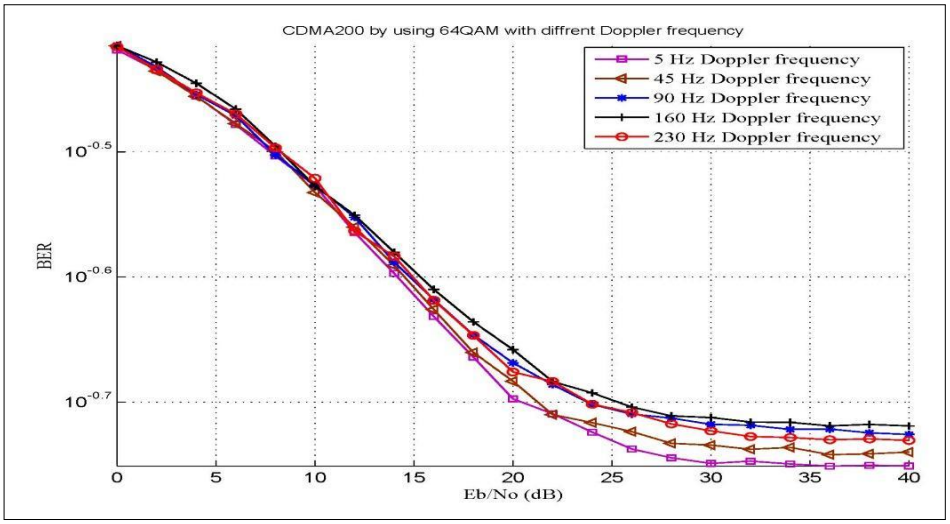


Figure (14): Simulation results of CDMA2000 by using 64-QAM over AWGN and Rayleigh fading.

4. Implementation of FFCh-DS-CDMA2000-1x

The proposed system has been designed and implemented based on SDR using FPGA. MATLAB-Simulink is used as an attractive simulation tool which provides the designer with many facilities such as fast design, and procedure test. Also, it gives the designer a clear imagination of the system parameters required to complete the design. MATLAB-Simulink of MATLAB (2009) is used in this work. Simulink HDL coder is a tool, which comes with MATLAB-Simulink software package and can be used to generate Hardware Description Language (HDL) code based on Simulink models and Stateflow finite-state machines. Figure (15) shows the flowchart of design and implementation of the proposed system steps according to the following steps:

1 - Setting Parameters

To start the implementation of the proposed system, the parameters of the proposed system should first be set, system parameters setting include specification of

the different types of codes, modulation/demodulation and other related system operations that the SDR could handle.

2 - Verifying Design Functionality

Some MATLAB-Simulink blocks, especially those that contain complex functions could not be converted to VHDL codes. To solve this problem, these blocks are redesigned using their basic components such that they could be converted to VHDL codes.

The modulations and demodulations are designed using embedded MATLAB functions (m-files), while other blocks are designed by MATLAB-Simulink blocks supported by Simulink HDL coder.

3 - Generating VHDL Codes for MATLAB-Simulink Using Simulink HDL coder.

Simulink HDL Coder compatibility checker utility can be run to examine MATLAB-Simulink model semantics and blocks forHDL code generation compatibility, then by invoking the coder, using either the command line or the graphical user interface. The coder generates VHDL or Verilog code that implements the design embeddedin the model. Usually, a corresponding test bench can also be generated. The test bench with HDL simulation tools can be used to drive the generated HDL code and evaluate its behavior. The coder generates scripts that automate the process of compiling and simulating the code in these tools.

As a result of using *makehdl* command in MATLAB, the following files would be generated:

- SDR.vhd: VHDL code. This file contains an entity definition.
- SDR_quartus.tcl: Quartus synthesis script.
- SDR_compile.do: Mentor Graphics ModelSimprogram compilation script to compile the generated VHDL code.
- SDR_map.txt: Mapping file. This report file maps generated entities (or modules) to the subsystems that generated them.

4 - Verifying Design Functionality Using (ModelSim tool)

The correct functionality of SDR is verified using Altera / Mentor Graphics ModelSim (6.5b) simulation tool. For this purpose, the test bench codes are compiled and simulated using the generated compilation and simulation scripts by the HDL coder.

5 - Designing Synthesis Using Quartus II

Designing Synthesis is a process that starts from a high level of logic abstraction (typically Verilog or VHDL) and automatically creates a lower level of logic abstraction using a library of primitives (Abdullah, 2009).

In this work, Quartus II 9.1 software has been used, providing a complete design environment for the System On a Programmable Chip (SOPC) design, which ensures easy design entry, fast processing, and straightforward device programming. Altera-Cyclone II FPGA family boards are used as target devices for implementation purposes.

6 - Downloading Bit Stream File to FPGA Boards

The synthesis process would also produce a bit stream file that can be downloaded in the FPGA board. The bit stream file of the SDR has been successfully downloaded to Altera-Cyclone II FPGA family boards, which is Cyclone II DE2-70. The test operation of the physical functionality of the SDR has been done by simply interfacing a function generator to apply input data and oscilloscope to monitor the recovered data.

The practical waveforms obtained from hardware implementation of the proposed SDR using Cyclone II FPGA boards, have been presented.

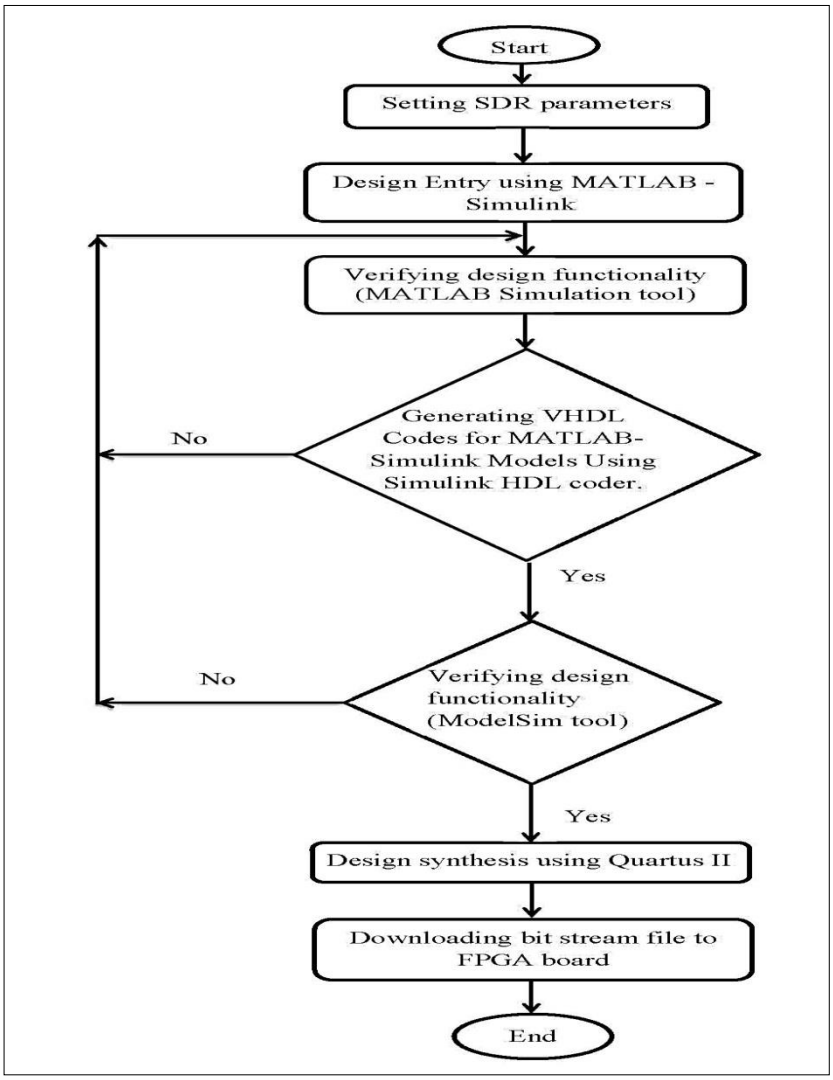


Figure (15): Flowchart of design and implementation system.

4.1 Implementation of FFCh-DS-CDMA2000-1x with 32-QAM

Figure (16) shows the input and outputwaveformsofthe proposed CDMA2000 system with 32-QAM modulation by using ModelSimprogram and figure (17) shows these input and output data.

Figure (16): Input and output waveforms of the CDMA2000 system with 32-QAM in ModelSim.

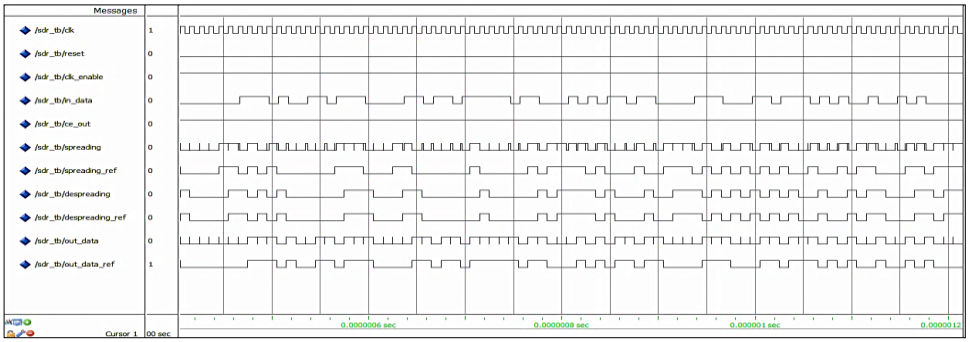


Figure (17): Input and output signal from an oscilloscope with 32-QAM.

4.2 Implementation FFCh-DS-CDMA2000-1x with 64-QAM

Figure (18) shows the input and outputwaveformsofthe proposed CDMA2000 system with 64-QAM modulation by using ModelSimprogram andfigure (19)shows these input and output data.

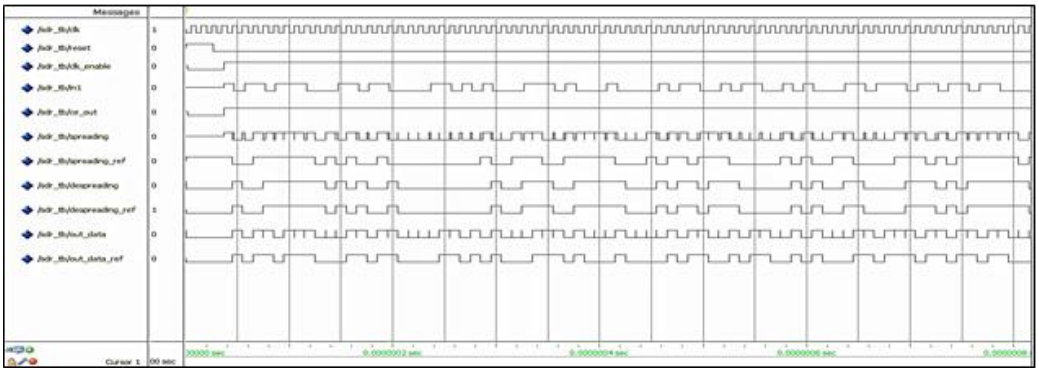


Figure (18): Input and output waveforms of the CDMA2000 system with 64-QAM in ModelSim.

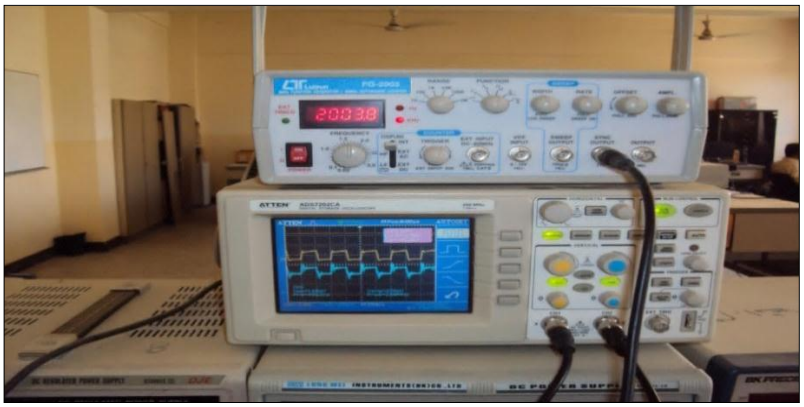


Figure (19): Input and output signal from an oscilloscope with 64-QAM.

5. Discussions of Results

The performance of the proposed system in the presence of AWGN and Rayleigh fading channel shows improvements compared with the system without long-PN code, Walsh code and complex system as follows:

1) For 32 QAM:

- For BER 10^{-3} with AWGN, the system performance is improved by (2.6) dB.
- For BER 10^{-4} with AWGN, the system performance is improved by (2.8) dB.

- For BER 10^{-5} with AWGN, the system performance is improved by (2.9) dB.
- For BER with different DFs (Doppler Frequencies) = (5, 45, 90,160 and 230) Hz the system performance is improved by (0.5) dB.

2) For 64 QAM:

- For BER 10^{-3} with AWGN, the system performance is improved by (3.1) dB.
- For BER 10^{-4} with AWGN, the system performance is improved by (3) dB.
- For BER 10^{-5} with AWGN, the system performance is improved by (3.2) dB.
- For BER with different DFs = (5, 45, 90,160 and 230) Hz the system performance is improved by (0.5) dB.

3) The experimental results obtained from the implanted system using HDL coder show the flexibility of implementing the forward channel CDMA2000 system.

4) The problem of implementing complex multiplication was solved during this work by converting the complex multiplication to the ordinary multiplication by using m-file. This problem is considered the main difficulty in the published literature.

6. Conclusions

The following points represent the main conclusions obtained from this work:

1) The results show that the FFCh-DS-CDMA2000-1x with 32QAM and 64QAM is a suitable technique to increase the data rate up to 2Mbps in the presence of AWGN and Rayleigh fading channel.
2) The simulation results of FFCh- DS-CDMA2000-1x system show improvements when using three levels of codes (LPNC, Walsh code and complex coding) within (0.5-3.2) E_b/N_o in (dB) in the presence of AWGN andRayleigh fading channel.
3) The implementation of the forward link channel using Simulink HDL coder shows feasibility and flexibility of solving the problem of complex multiplication of complex spreading code also the practical results were close to that obtained from ModelSim program.
4) Simulink HDL coder is very helpful for system engineers since the coder automates the hardware implementation process. Simulink HDL coder does not support all MATLAB-Simulink blocks, so to generate VHDL codes for such blocks they must be redesigned according to their basic design blocks supported by Simulink HDL coder.

7. References

Abu-RgheffM. A., 2007 “Introduction to CDMA Wireless Communications”, 1st edition, Elsevier Ltd.

Abdullah, H. N. and others, 2009“Design and Implementation of FPGA Based Software Defined Radio Using Simulink HDL Coder”, Eng. & Tech. Journal, Vol. 28, No. 23.

Angelis, G. De, and others, 2010,“Parallel PN Code Acquisition for Wireless Positioning in CDMA Handsets”, 5th Advanced Satellite Multimedia Systems Conference and the 11th Signal Processing for Space Communications Workshop, IEEE, pp. 343-348.

Goldsmith, A., 2005, “Wireless Communications”, Cambridge University Press.

Jain, R. and others, 2002 “Implementation of Adaptive Modulation on the Sunrise Software Radio”, Circuits and Systems, IEEE, Vol. 3, pp. 405-408.

Khan, R. and others, 2005, “Evolution of CDMA one and Development of CDMA

2000 Convergence and Harmonization", Asian Journal of Information Technology, Grace Publication, pp. 935-939.

Mathwork Inc., 2011 "Simulink HDL Coder".

Naif,Z.T.,2009, "Performance Analysis of Communication Systems with Variable Data Rate and modulation technique by Using Software Defined Radio (SDR)", M.Sc. thesis, Department of Electrical and Electronic Engineering, University of Technology, Iraq.

Xia, B.and others, 2005, "Analytical Study of QAM with Interference Cancellation for High-Speed Multicode CDMA", IEEE Transactions on Vehicular Technology, IEE/IEEE, Vol. 54, No. 3, pp. 1070-1080, May.