Journal of Babylon University/Engineering Sciences/ No.(1)/ Vol.(22): 2014

Quantum Dot Cellular Automata models using VHDL-AMS

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Abstract

Transistor is reaching to its physical limits. The search for another technology is full of options. Quantum dot cellular automata among other nanotechnology approaches are strongly nominated to replace the transistor in the digital applications. In this paper we present a Library for the QCA components using VHDL-AMS on the behavioral level. This library will give researchers the required flexibility with building digital circuits for different applications because they can use different types of clocking signals also using the VHDL-AMS environment help to extend the behavioral modeling to dynamical modeling. الخلاصة

الترانزستور هو الوصول إلى حدوده المادية. البحث عن تكنولوجيا أخرى غير كاملة من الخيارات. يتم ترشيح الكم نقطة الآلي والخلوية بين النهج تكنولوجيا النانو أخرى بقوة ليحل محل الترانزستور في التطبيقات الرقمية. في هذه الورقة نقدم مكتبة للمكونات QCA باستخدام AMS VHDL-على المستوى السلوكي. وسوف تعطي هذه المكتبة الباحثين المرونة المطلوبة في بناء الدوائر الرقمية لمختلف التطبيقات لأنها يمكن استخدام أنواع مختلفة من قطع مسافة السباق أيضا باستخدام إشارات مساعدة البيئة AMS VHDL-تمديد النمذجة السلوكية إلى النمذجة الديناميكية.

1. Introduction

The current chips integration technology is reaching to its physical limits. So, there are a lot of proposed technologies that can be used at the nano scale. one of these are quantum dot cellular automata (QCA). The theory of QCA was proposed by Lent et al. in 1993 (Lent et al. 1993). QCA encodes binary information in the charge configuration within a cell. Coulomb interaction between cells is sufficient to accomplish the computation in QCA arrays-thus no interconnect wires are needed between cells. No current flows out of the cell so that low power dissipation is possible.

A simple QCA cell consists of four quantum dots arranged in a square, shown in Figure (1).



Figure (1) Schematic of a QCA cell. (a) Two states "1" and "0" in a single cell;(b) Coulomb interactions couple the states of neighboring cells.

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Dots are simply places where a charge can be localized. There are two extra electrons in the cell that are free to move between the four dots. Tunneling in or out of a cell is suppressed. The numbering of the dots in the cell goes clockwise, starting from the dot on the top right. A polarization P in a cell, which measures the extent to which the electronic charge is distributed among the four dots, is therefore defined as Eq.(1)

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4} \quad \dots \dots (1)$$

Where P_i denotes the electronic charge at dot i. Because of Coulomb repulsion, the electrons will occupy antipodal sites. The two polarized charge configurations P = i1 and P = 1 correspond bit value of 0 and 1 respectively. These two states are used to encode the binary information. When a polarized cell is placed close to another cell in line, the Coulomb interaction between them will force the second cell switch into the same state as the first cell, minimizing the electrostatic energy in the charge configuration of the cells. Based on the Coulomb interaction between cells, fundamental QCA devices can be built.

In this paper, a computer modeling of QCA automata basic blocks is presented using VHDL-AMS.

The rest of the paper is organized as follows. In section 2 a background of the QCA clocking presented, In section 3 the blocks modeling are presented, and finally the conclusions and future works in section 4.

2. QCA clocking

Since there is no current flow in QCA wire so to control signal flow direction and for Timing control, to restore the lost signal energy to the environment, creating pipelines if multiple clock signals could be used ,Forcing the circuit to stay in the quantum mechanics ground state and other reasons discussed by Hennessy et al. in 2001 (Hennessy *et al.* in 2001) the QCA wire should be clocked. A lot of methods were proposed for clocking and all of them had four phases with different timing for each phase.



Figure (2) (Hennessy *et al.* in 2001). The four phases of the QCA clock (switch, hold, release ,relax) and the transition of phase in order to move a bit in a wire left to right.

The clocking field with four phases shown in Figure (2) cannot be changed with the usual clock signal with two phases (high and low) because if abrupt switching is used The Input is changed suddenly to the QCA circuit and the circuit would be in some excited state and

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try to relax to ground state by dissipating energy to the environment, The relaxation will be inelastic and uncontrolled, and The circuit may enter a metastable state that is determined by local and not global ground state .

While for the four phase switching the clock signal is designed to ensure adiabatic switching (four phases signal), the relaxation is controlled by the switch and release phases of the clock signal, and the circuit is always kept in its instantaneous ground state.

To control the energy barrier of the tunneling device in the cell for QCA, the clock signals are generated through an electric field, which is applied to the cells to either raise or lower the tunneling barrier between dots within a QCA cell. This electric field can be supplied by CMOS wires buried under the QCA circuitry as shown in Figure (3) (Lent, C. S. and P. D. Tougaw 1997). When the barrier is low, the cells are in a non-polarized state; when the barrier is high, the cells are not allowed to change state. Adiabatic switching is achieved by lowering the barrier, removing the previous input, applying the current input and then raising the barrier. If transitions are gradual, the QCA system will remain close to the ground state. Two common versions of these clocking four phase signals are the Landauer clocking waveform and Bennett clocking waveform shown in figure 4 which contain four clocking signals with a phase shift to accomplish the pipelining on the cell level.



Figure (3) (Lent, C. S. and P. D. Tougaw 1997) The CMOS wires buried under the the QCA circuitry to generate the clocking field



Figure(4) (Hennessy *et al.* in 2001) Landauer clocking waveform with 90° phase shift and Bennett clocking waveform.

3. QCA modeling

There are several software for working with QCA. The most common tool is the QCADesigner (Walus, K., *et al.* 2003) but the problem with this software and others is their inability to deal with multi types of clocking signals. They are all using the Landauer clocking.

This problem made these software not useful when we manipulate the clocking signal to get a certain performance from QCA circuit where a lot of designs depend on changing the type of the clocking signal as the ones reported in (Vamsi Vankamamidiand *et al.* 2008, Christopher R and *et al.* 2005, Niemier, M. T. and *et al.* 2002).

M. Ottavi et al (M. Ottavi *et al.* 2006) in 2006 used Verilog HDL to build the QCA library, but he couldn't expand this library to include the dynamic behavior of the cell because Verilog is unable to deal with continues differential equations therefore his library could not be used for practical modeling of QCA. So, we decided to start building a QCA library using VHDL-AMS where we have the required flexibility to simulate and model different types of QCA circuits with different clocking schemes. Therefore, in this paper we start with behavioral description of the major QCA blocks, which are shown in figure 5 and listed below:

2. QCA wire

3. QCA L shape wire

- 4. QCA Fan out
- 5. QCA Inverter
- 6. QCA Majority Voter

From the behavioral point of view the first and second components (strait and L shape wires) are the same.



In our library we define the clock as a state variable with four states and the timing for the transition between states can be controlled with the clock cycle also this state vector could be extended to state matrix of multiple state vectors to achieve the multi zone clocking presented by Landauer or Bennett for pipelining.

Each block response is depends on the current state of the clock state vector. For the blocks output we used the IEEE STD_logic type and since the output will be valid only if the clock is in the (Hold) state we define the output for the other three states as follows:

Clock state 'relax'

Output= 'w' regardless the input value (weak unknown as given in IEEE Std_logic type) because when the clock is in the relax phase the cell barriers are in their lowest state and the cell is unpolarized.

Clock state 'switch' or 'release'

Output = 'x' regardless the input value(unknown as given in IEEE Std_logic type) because when the clock is in the 'switch' or 'release' phases the barriers are being increased or decreased to enable electron switching and cell polarization will unknown.

Clock state 'Hold'

This is the only phase in which the cell state is valid and for each block the output is calculated depending on the input state. The code for each block is given in the Appendix.

4. Conclusions and future works

In this paper a library for the basic QCA blocks was written using VHDL-AMS. This library can adopted for building a wide range of digital circuits with any type of adiabatic clock. The expanding of this library to include the dynamical behavior of the

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QCA cell and the coherence and correlation between cells is easy since we are working in AMS environment. If this expansion achieved it would an advanced step for calculating the power dissipation of the QCA digital circuits from the simulation an advantage that left for the future works.

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