EFFECTE OF THERMAL ANNEALINEG ON THE ELECTRCAL PROPERTIES OF PbS/Si HETEROJUNCTION

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Abstract

In this research the electrical properties for heterojunction devices have been improved by process of simple annealing temperature about one hour period. The results have been explained that the influential of analysis process on electrical properties during the clearest improve for devices properties at special temperature .

1. Introduction

The process of simple annealing temperature represents is one of the essential and publical ways for solve the special problems that happened during the growths subtraction[1]. The process of annealing temperature has several uses. It is used for improving the value of detectors and transistors which is made from semiconductors thin films and integrated circuits[2]. Heterostructure devices are receiving now considerable interest because of their potentially high performance per unit cost, where low technological complexity and low temperature (as compared with homojunction devices) can be employed. A substantial amount of work has been published on heterojunctions[3-6]. The last decade witnessed an increasing competitive attention on the narrow- bandgap/wide-bandgap heterojunctions [7-10]. In this combination , efficient IR photodetectors can be obtained when the wide-bandgap semiconductor acts as an window layer and the narrow- bandgap semiconductor acts as an absorber. Foremost in those heterojunction detectors is the PbS/Si heterojunction[12-14]. This hetero-pair was prepared by depositing PbS films onto Si in many routes, such as thermal evaporation[15] or chemical-solution growth[16]. However, the fabrication PbS/Si heterojunction by chemical spray pyrolysis technique is not found . this note prompted us to fabricate PbS/Si heterojunction by utilizing chemical spray pyrolysis technique.

2. Experimental Procedure

2.1. Sample preparation

By chemical spray pyrolysis Lead-supplied has been deposited on to monocrystalline P-type silicon wafer (111) orientation to prepare PbS/Si heterodiode. The deposition procedure was achieved by pyrolytic spray of 0.2 M of aqueous solution of $Pb(NO_3)_2$ and thiourea on the mirror-like surface of the wafer. The temperature analysis of the deposited films which estimated approximately from the gravimetric method was varied between. The substrate temperature was maintained during spraying at 350°C. This optimum temperature was selected from five different temperatures. Ohmic contacts were made as the following :frontal metal contact was done after PbS deposition by evaporating 250nm pure Al through a special mask , while the deposition of back metal contact was done before PbS deposition.

2.2. The process of annealing

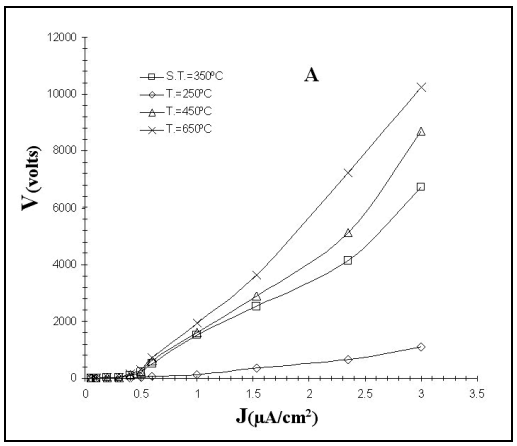
The essential way of annealing temperature has been used by oven at temperature between (250-650 °C) for one hour.

2.3. Electrical properties

I-V and C-V characteristics were measured after wiring the fabricated diodes. The main parameters were extracted from these measurements viz; ideality factor n and built-in voltage V_{bi}. Four-point probe method was used to determine the conductivity of PbS deposited films.

3. Results and Discussion

Results of four probe measurements revealed that the conductivity of PbS films is n-type. Thus, it is anticipated that PbS/Si heterojunction will take the form of an iso type heterodiode. Fig.(1) shows J-V curves for the heterodiodes prepared in different annealing temperatures of PbS thin films (as shows in the legend). From this figure, it is shown that the behavior of J-V curves is similar to that proposed by Anderson[14]. It can be seen that the diodes exhibit good rectification factor with value approaches 20.7 at 1V bias for samples 450 °C annealing temperature as shown in fig. (2). A semi-log J-V plot at the forward bias is demonstrated in Fig. (3) and the reverse saturation current density J_{sat} represents the intersection of



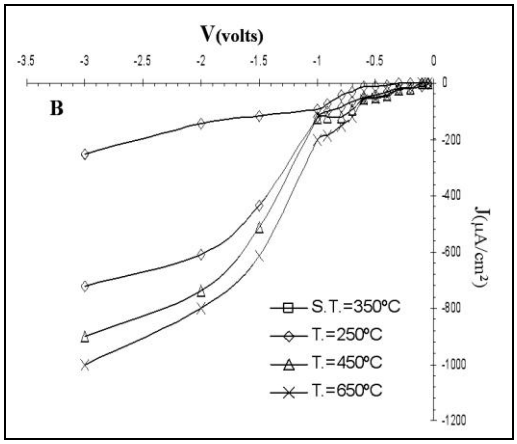


Figure 1. J-V Curves, a-Forward, b-Reverse

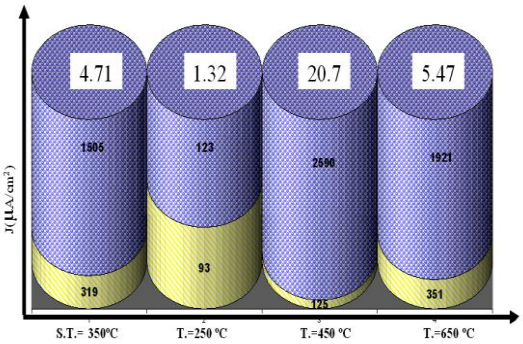


Figure 2. Forward and Reverse Current As afunction of annealing temperature

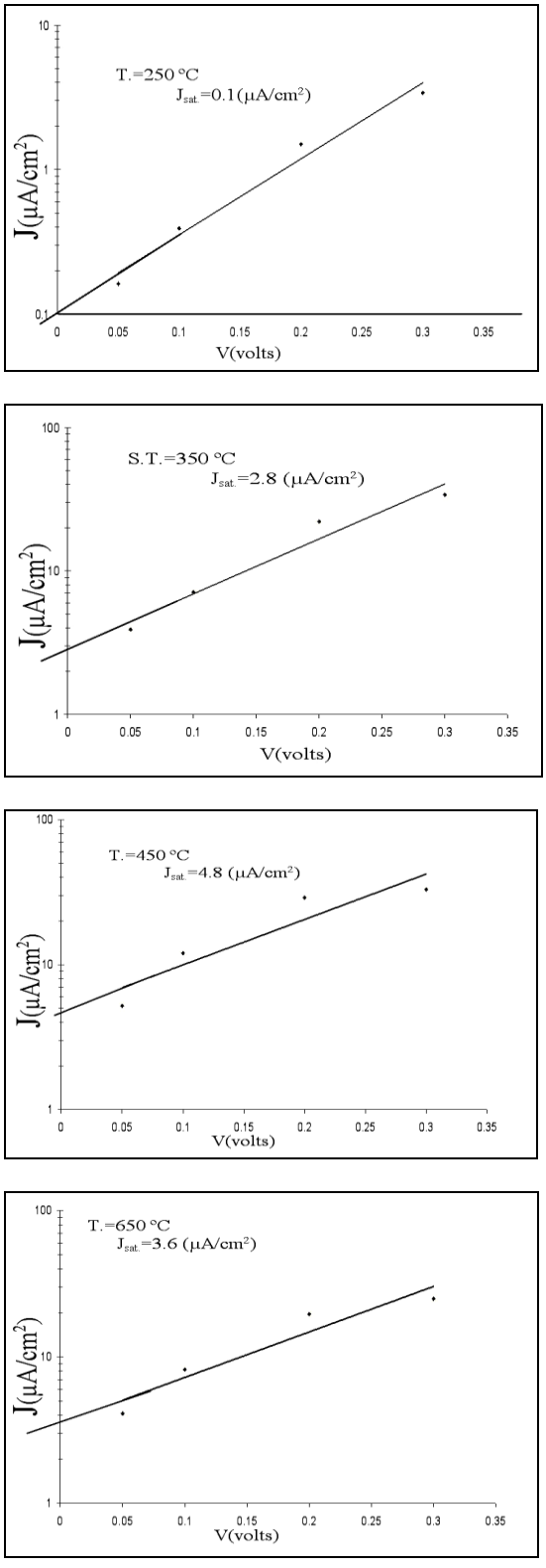


Figure 3. Semi-log J-V Characteristics

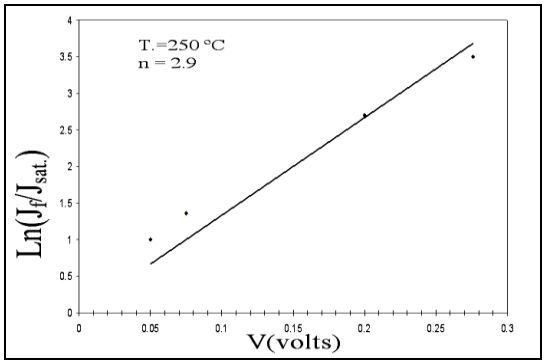
the straight line with current axis. At large, J_{sat}. decreases when T.=450 °C .This can be attributed as following; The junction will be located near to surface which leads to high leakage current (J_{sat} is high), The junction will be located far from the surface which leads to decrease in leakage current. At high annealing temperature 650 °C, strains taken place due to lattice mismatch effect would cause substantial amount of dislocations[18] which in turn will produce a great deal of recombination centers, hence recombination current component will be added to the diffusion current component i.e., J_{sat} will be increased.

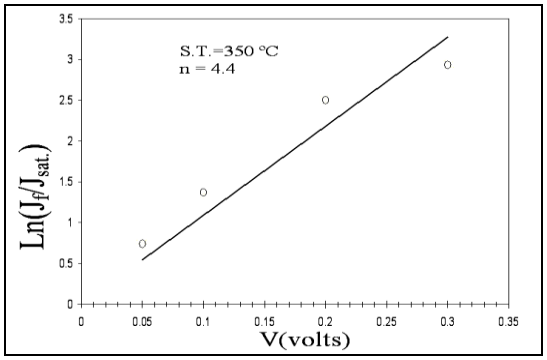
fig.(4) is the $\ln(J_F/J_{sat})$ – V plot. The slop of this plot is the direct method to calculate ideality factor n. From this figure, it can be seen that the diodes prepared at 250 °C annealing temperature has a better ideality factor .

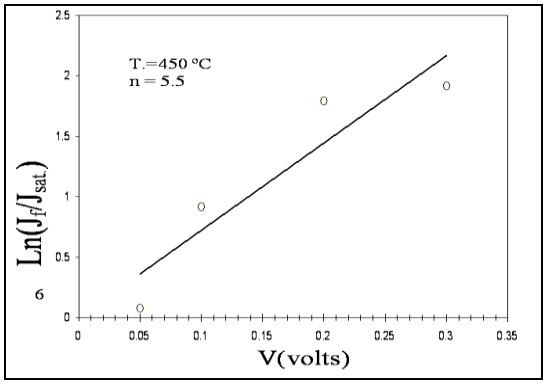
Fig.(5) is the reciprocal of square capacitance against reverse bias voltage will form a straight-line plot. The extrapolated straight-line intercepts the voltage axis at the point of built-in voltage.

4.Conclusions

Extracted from the above mentioned , we can draw the following :low-cost CSP technique is suitable to fabricate PbS/Si heterojunction diodes. This heterojunction will be anisotype when silicon substrate is p-type. annealing temperature of PbS thin films greatly affects the device characteristics. There are specific border for annealing temperature inorder to be positive effect in improving electrical properties orelse it be come negative effect . An essential properties that we have getting during annealing temperature about 450**°C** has abetter results **.**







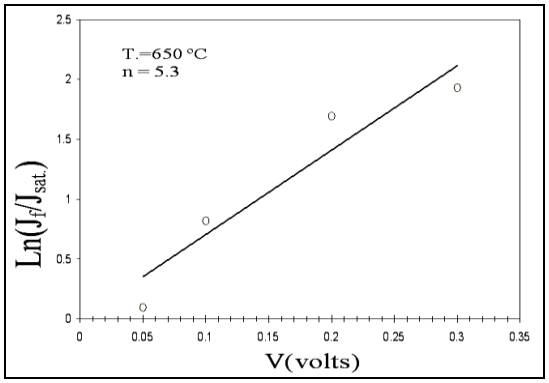


Figure 4. $\ln(J_F/J_{sat})$ against Forward Voltage for Ideality Factor calculations

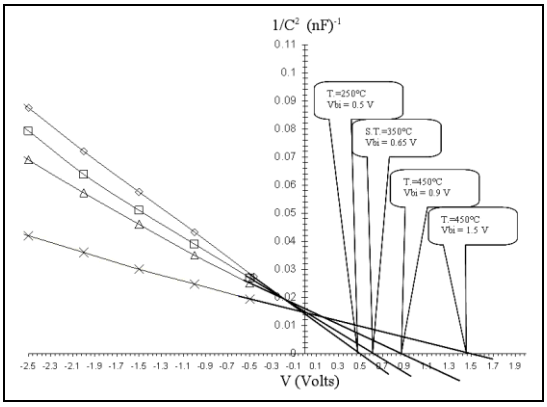


Figure 5. Reciprocal of Square Capacitance with Bias Voltage

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