Data Weighted Averaging (DWA) Technique with 1st order Noise-shaping to Improve 6 bit Digital-to-Analog Convertor (DAC) Performance

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Abstract

A first order of DWA (data weighted averaging) technique is proposed to improve 6-bit digital-to-analog convertor (DAC). In addition, this paper discusses the impact of mismatch between DAC unit elements. The simulation results show the effectiveness of the DWA technique in reduction of inband tones, also DWA technique proves its ability to solve DAC unit elements mismatch. The element mismatch noise is converted into a broadband. The mismatch elements noise is improved 9 dB if σ =0.01 with proposed DWA, thus improving the DAC performance if compared with DAC performance without using DWA circuit.

***Keywords*:** Digital/Analog Converter (D/C), DAC mismatch, Dynamic Element Matching (DEM), Data Weighted Averaging (DWA) technique.

الخلاصة

يتضمن هذه البحث مقتراح لأستخدام خوارزمية (البيانات المتوسط المرجح) من الدرجة الاولى لتحسين أداء محول الاشارة الرقمية الى الكمية (6–Bit DAC) . اضافة الى ذلك تم مناقشة مشكلة عدم التوليف بين عناصر محول الاشارة الرقمية الى الكمية . نتائج المحاكاة بينت فعالية تقنية البيانات المتوسط المرجح في تقليل مستوى نغمة داخل الحزمة وكذلك التغلب على مشكلة عدم التوليف بين عناصر (DAC). تم تخفيض قيمة ضوضاء عدم التوليف بين عناصر المحول بمقدار (9dB)عندما يكون قيمة عدم التولي σ = 0.01 .

1. Introduction

High-resolution digital-to-analog converters (DACs) are increasingly used for direct digital synthesis, arbitrary waveform generation, and video signal processing. The main requirement of DACs for these applications is good linearity, which implies high spectral purity and small output errors. To maintain good linearity, trimming and calibration have been used to directly decrease element mismatches that result in high spurious-free dynamic range (SFDR) and small maximum output errors. Another technique called dynamic element matching (DEM) has been successfully applied to reduce the correlation of DAC noise to the input signal for achieving high SFDRs. Randomization, which is one of the DEM techniques, is mostly used for Nyquist-rate DACs to spread the harmonics as white noise over the output spectrum. However, the possible maximum output errors of randomization are still large because the elements are selected randomly [*Da-Huei Lee, etc.*, 2006].

The DEM schemes are implemented with unitary elements steering DACs. The way the elements are selected gives the name to the algorithm, and this result in a given characteristic of dynamic matching. Some of the most important are: Individual Level Averaging (ILA), Clocked Averaging (CLA), Random Averaging, and Data Weighted Averaging (DWA). One of the simplest DEM scheme is the DWA which selects the unitary elements cyclically. The main characteristic of the DWA is the capability to shape the spectrum of the mismatch error as a first order high-pass filter [*Ramón, etc., 2007*].

2. Principle of DWA Algorithm

Mismatch in the DAC unit elements causes distortion in the signal band which reduces the obtained signal to noise plus distortion ratio (SNDR). To solve this problem, DAC uses DEM techniques. The functional principle of all DEM techniques is to transfer distortion that occurs due to the fixed step-size errors into a noise signal

that is spread over the whole frequency band up to half of the sampling frequency, then shaping to high frequency [*Bach E.,1999*]. The components of the quantization noise and the DAC noise outside of the signal band in Figure (1a) will be removed by the filter but much of the DAC noise will be in band. Using noise-shaping DEM techniques results in DAC noise that pushes DAC noise outside the signal band as illustrated in Figure (1b).

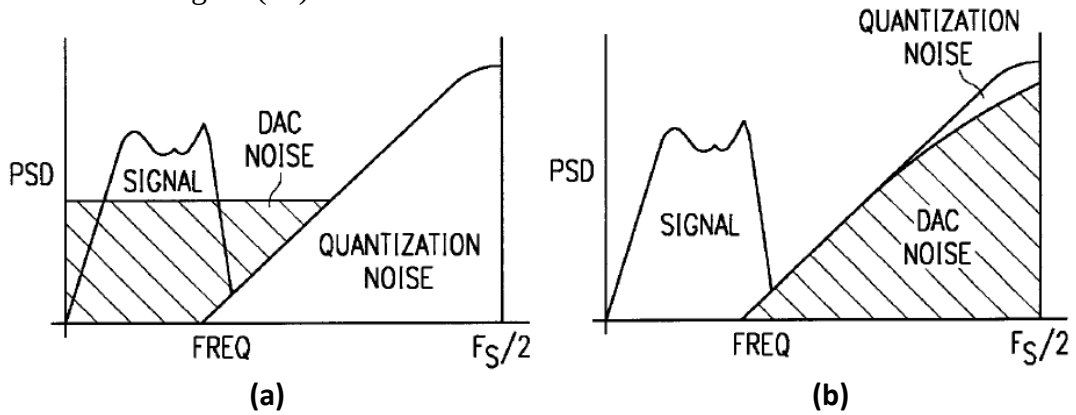
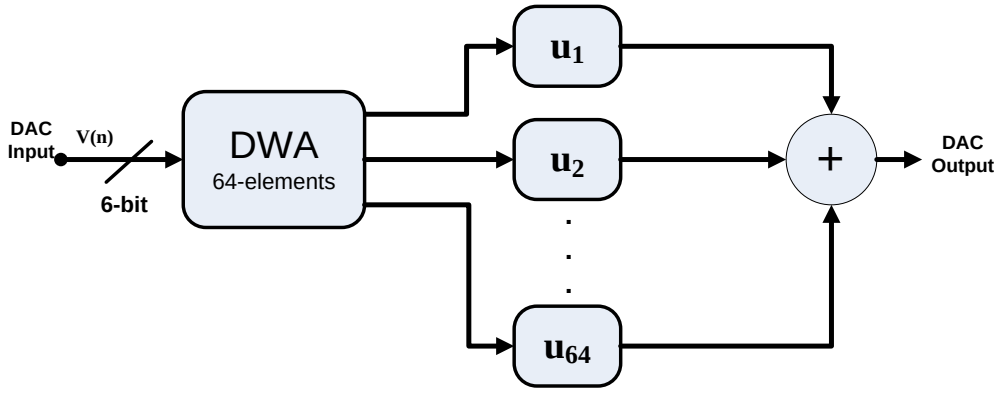


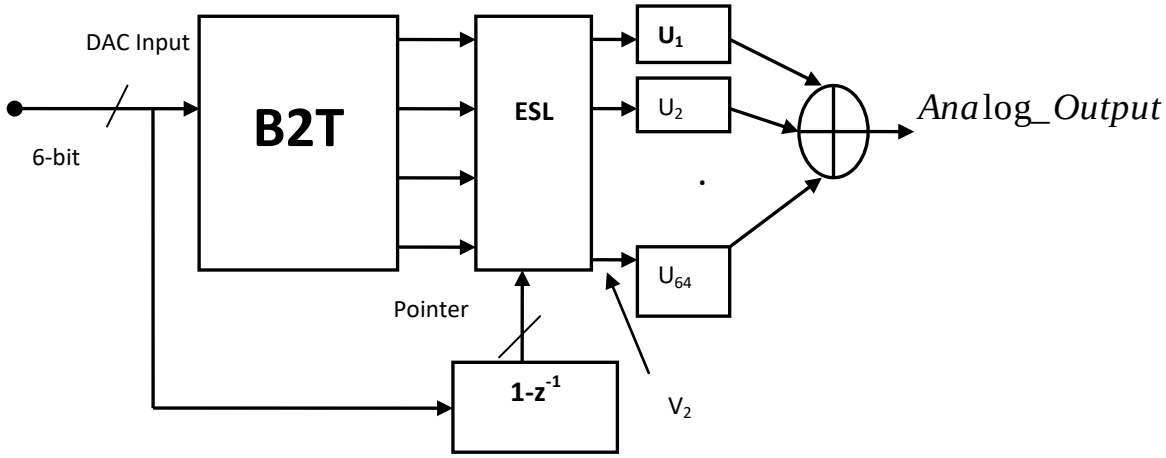
Figure (1): Typical power spectral densities at the output of the DAC (a) Without DEM, (b) with DEM algorithm

3. Proposed of DWA circuit

The DWA for a 6-bit DAC is illustrated in Figure (2a). The counter is used to create pointer (***Ptr***) that shows the point of first unused unit element. The code is converted to thermometer code (Binary-to-Thermometer code (B2T) = (2^B)) [*Kuan, etc., 1999*]. The algorithm cycles through the DAC elements by sequentially selecting the elements based are upon the input data [*Kuan, etc., 1999*]. The proposed DWA for a 6-bit DAC as shown in figure (2b), DAC cells (U_1, U_2... U_{64}) must be selected circularly based its consecutive input value (***v(n)***). From one period to another, the status of selected cells is simply memorized by a pointer ***Ptr(n)***.



(a)



(b)

Figure (2): (a) 6-bit DAC, (b) Proposed 1st DWA Circuit for 64 DAC unit elements.

The DAC inputs produces an **M**+1 level signal ***v(n)***, which is fed into the element select logic (ESL) block. The ***v2(n)*** output of the block contains **M** bits, each of which enables a particular unit element in the subsequent unit-element DAC. The number of elements enabled at each instant is equal to ***v(n)***.The ESL of figure (2) selects elements in such a way that the mismatch error existing between those elements is noise shaped

The key point is that the error due to element mismatch is shaped by the H(z) = $(1-Z^{-1})^1$.

Mathematically, the nonlinear part of DAC mismatch error on its output can be estimated as follow [*Esmaeil etc.,2009*]:

$DAC_{error} = (1 - z^{-1})$ *IM (Ptr (Z))*…….**(2)**

Where:

IM (Ptr (Z)) = Integral mismatch,

$(1-z^{-1})$ = First order noise-shaping

$$IM(Ptr) = \sum_{n=0}^{n=Ptr-1} (V(n) - V_{mean})/V_{mean} \text{ …..(3)}$$

$$V_{mean} = \frac{1}{N}\sum_{n=0}^{N-1} v(n) \text{ ……..(4)}$$

Nonlinearity errors for a DAC derived by DWA element selection scheme can then be analytically calculated using equation (3).

As shown in figure (3), DAC input codes of (32,34,36,37,41,40,…… ,54) are used as an example. In the beginning, the value of ***Ptr*** is 0. For an initial input of 32 the elements $\{u_1,u_2,u_3,u_4,u_5,u_6,u_7,\ldots,u_{32}\}$ are selected according to the value of ***Ptr***. At the same time, the value of ***Ptr*** becomes 33. For the second input of 34 the elements $\{u_{33},u_{34},u_{35},u_{36},u_{37},\ldots\ldots\ldots,u_{64},u_1,u_2\}$are selected, the value of ***Ptr*** becomes 3, and so on.

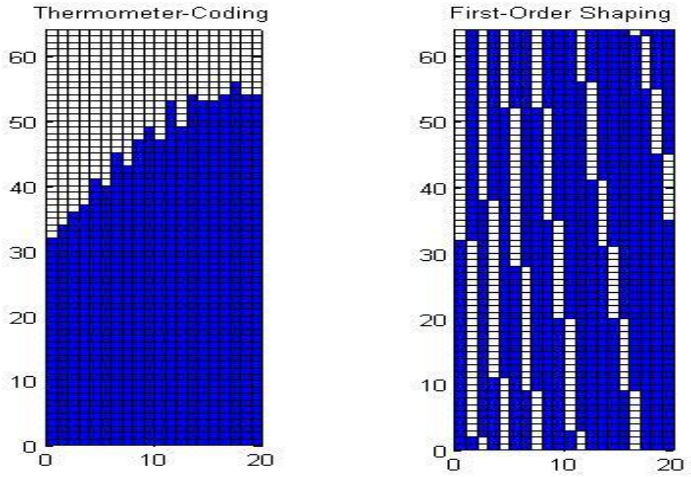


Figure (3): Simulation of DWA operation.

4. Simulation Results

The proposed 1st order DWA Circuit is used in 6-bit DAC circuit, the DAC is composed of (1 to 2^B) unit elements, where B is the number of bits in the DAC. In order to match the unit elements, the DWA algorithm is used. Without DWA enabled, the unit element mismatch leads to a large amount of tones feed-through. Figure (4) present the result of simulation for 6-bit DAC with 0.01 unit element mismatch (σ) without using proposed DWA. Simulation show high tones at the output of the DAC. Figure (5) shows the result of simulation of proposed 6-bit DAC/1st order noise shaping DWA with (σ =0.01). In order to evaluate the impact of increase of DAC unit elements current sources mismatch on DAC performance, a suite of simulations was run with the DAC mismatch error set to 0.06, as shown in figure (6). Simulation results show that the high tone appears at the output of DAC if DWA circuit is not used.

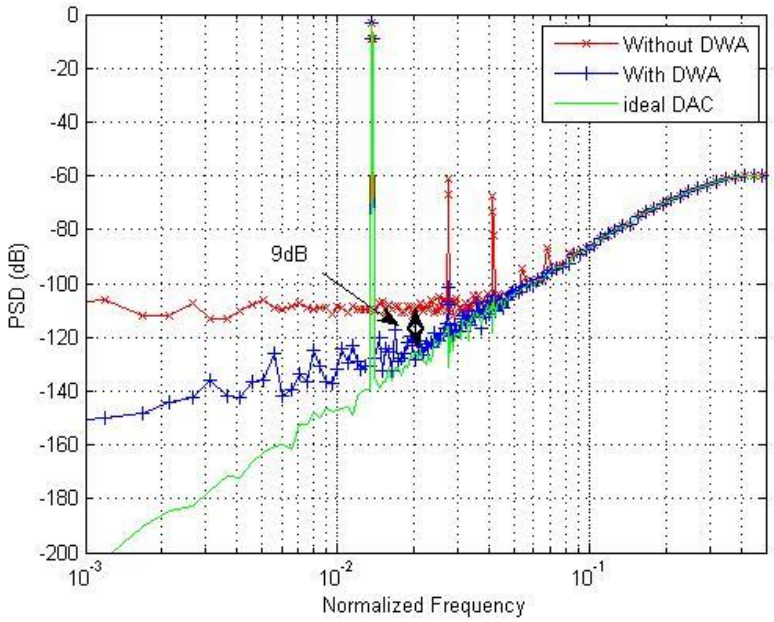


Figure (4): Simulation showing the impact of unit element mismatch (Elements mismatch error (σ) = 0.01).

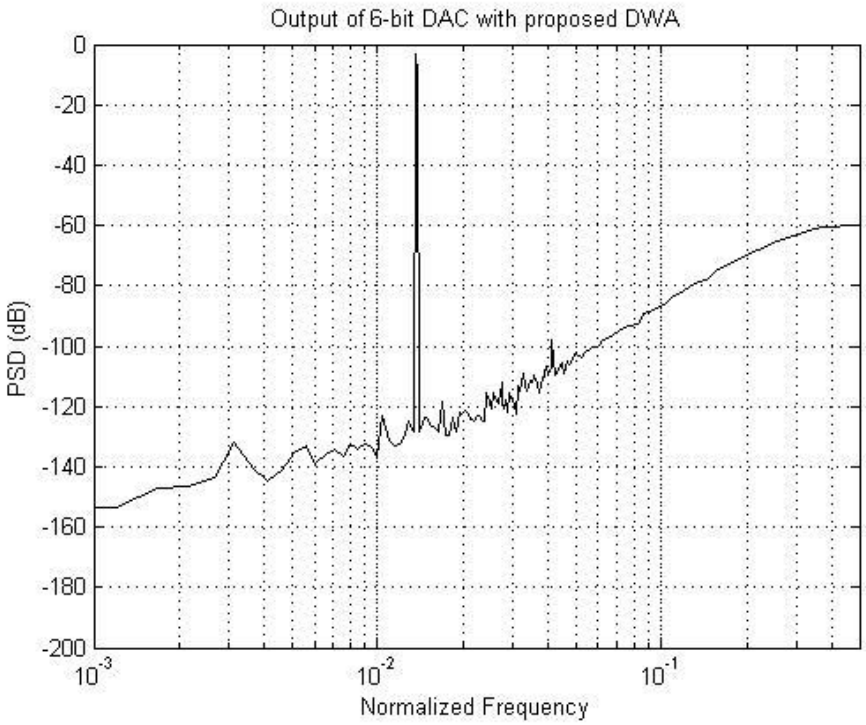


Figure (5): Simulation showing the output of 6-bit DAC with DWA (Elements mismatch error (σ) = 0.01).

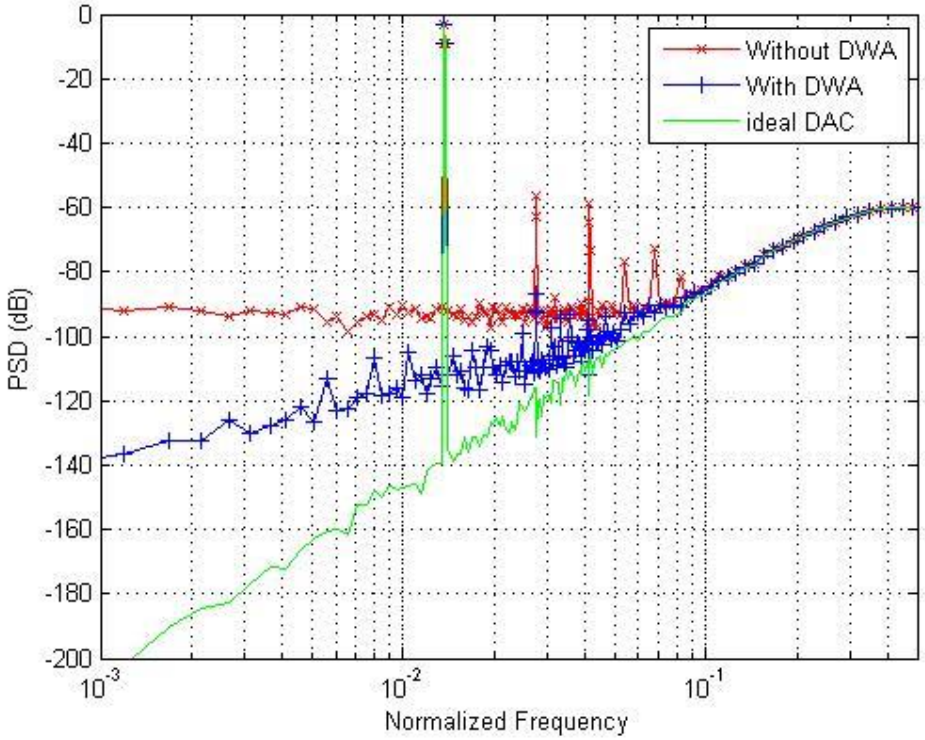


Figure (6): Simulation showing the impact of DWA on the quantization noise spectrum for 6-bit DAC (σ = 0.06).

To matching between the unit elements and suppressing tones of DAC, the proposed DWA is used. The DWA technique proves its ability to solve DAC unit elements mismatch. The element mismatch error is converted into a broadband,

shaped noise that appears to have the same profile as the quantization noise spectrum. Table (1) shows the final result of simulation.

Table (1) shows the final result of simulation for 6-bit DAC.

	σ =0.01	σ =0.06
Psd(db)	9	4

5. Conclusions

DAC mismatch elements are studied and show that the tones level increase with increasing the mismatch between DAC elements. It was found that DWA algorithm proves its ability to solve this problem. DAC mismatch noise (σ =0.01) with DWA is founded 9 dB maximum inband tone reduction thus improving the DAC performance if compared with DAC performance without using DWA circuit.

6. References

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