High Level Implementation Methodologies of DSP Module using FPGA and System Generator

Dr. Majid S. Naghmash
Technical College, Foundation of Technical Education/Baghdad
Email: msnengb99@yahoo.com
Dr. Mousa K. Wali
Technical College, Foundation of Technical Education/Baghdad
Email: musawali@yahoo.com
Amar A. Abdulmajeed
Technical College, Foundation of Technical Education/Baghdad
Email: aljobori_2005@yahoo.com

Received on: 4/2/2015 & Accepted on: 17/9/2015

ABSTRACT

This paper presents the high level implementation methodologies of Digital Signal Processing (DSP) module by using the Field Programmable Gate Array (FPGA) and integrated software environments (ISE) with the System Generator programs. The shortest and efficient paths to design a Xilinx Vertix-4 FPGA using MATLAB, ModelSim, synplify Pro software tools is introduced. The floating point design in MATLAB has been moved to fixed point values using Xilinx DSP system generator software a model based approach associated with assistance software from Mathworks and Synplicity. The obtained result shows an important utilization in FPGA area.
Keywords: DSP, FPGA, MATLAB, System Generator, ISE

طريقة تنفيذ عالية المستوى لمعالج الاشارة الرقمية باستخدام مصفوفة البوابات المبرمجة ومولد النظام

الخلاصة

هذا البحث يقدم طريقة تنفيذ عالية المستوى لمعالج الاشارة الرقمية باستخدام مصفوفة البوابات المبرمجة ومولد النظام. استخدمت طرق قصيرة وكفوءة لتصميم مصفوفة البوابات المبرمجة باستخدام مجموعة برامجيات حديثة لتغيير تصاميم القيم المثالية الى القيم الحقيقية بمساعدة برامجيات مساعدة من مجموعة ماثوورك . النتائج تبين اختزال مهم في مساحة البوابات المبرمجة .

INTRODUCTION

The device capability to process a signal by digital meaning is so called Digital Signal Processing (DSP). Though, several DSP processers exist are mostly implemented with the same few basic operations. The basic characteristics of DSP are the high speed, data transfer to and from real word, and multiple access memory architectures. The development of DSP module with respect to other devices such as Application-Specific Integrated Circuit (ASIC) and FPGA

https://doi.org/10.30684/etj.34.2A.9
2412-0758/University of Technology-Iraq, Baghdad, Iraq

have many advantage such as faster developing time and more suited for prototyping purposes. Currently, the classes of DSP available are fixed point and floating point devices with large variety of arithmetic precision [1]. The two dimensions array of flip flop and logic blocks connected electrically and programmable controlled are so called Field Programmable Gate Arrays (FPGA's). The programmable interconnection between logic blocks are implemented using multiple gates and user configuration which is interconnection between the logic blocks and function of each block [2]. The project processing could be implemented at a given time and dynamically replaced in the name of reconfiguration of FPGA [3]. Xilinx logic block in term of lookup table (LUT) is used to implement different functionality of in hand project as hardware platforms for reconfigured applications resulting in talented hardware solution [4]. The salesperson of FPGA has multiple device production and available recourse. Now days Xilinx has feed many FPGA recent familiars spartan-8 and Vertex-8 [5].

Every new Xilinx FPGA generation is capable to run more speed and fast sampling signal to follow the rapid growth in all communication field and other laser and satellite communication [6]. The Xilinx target is to provide low power, highest performance, and global time reducing and gate density. The register transfer language (RTL) could be synthesized into any device with specific logic resources in hardware description language (HDL) for FPGA [7]. The real or register unit delay throughout circuit can be reduced the number of combinational logic level by an internal correlation between the largest number of logic level and its frequencies [8].In the surrounded applications of communication systems, the Field Programmable Gate Array is extensively used due to its re-configurability. The level of investment an entire system is FPGA developed on a single chip, while permit in platform testing and correcting of the system. Additionally, it presents an opening of utilizing hardware-software co-design to extend a high performance system for unusual applications by excluding processors for definite software functions [9]. The digital design of FPGA can be realize by using hardware description languages (HDL) which involve more information and skills in the tools such as VHDL and Verilog. The environment for model-based design in MATLAB/simulink is almost covering all industrial and scientific areas [10]. Many researcher has been implemented the FPGA platform. A methodology for implementation DSP applications on FPGA using system generator is presented by [11]. The logic programming of multichannel pulse compression system based FPGA with high speed transmission module is introduced by [12]. The methodology of designing the model for useful communication technique, namely MIMO using system generator and AcceLDSP has been presented by [13]. The design and implementation of image processing applications on FPGA is presented by [14]. The designs were implemented on Spartan 3A DSP and Virtex 5 devices. Synthesis of VHDL Code for FPGA Design Flow Using Xilinx Plan Ahead Too was proposed by [15]. In this paper, the Xilinx digital signal processing (DSP) tool in system generator is investigated with graphical interface environments based MATLAB/ simulink and block set of DSP cores is used to model the DSP system. The model based SDR system is designed and implemented using FPGA vertex-4 platforms.

BasicVertex-4 FPGA Architecture

The FPGA of Vertex-4 device with many configuration parts showing in Figure 1and Figure 2 [15] optimized for high density and performance system design. The FPGA functionality of each element could be summarized as follow.

1. The Input-Output (I/O) block provides the interface between encloses pins and the internal configurable logic which will enhance the source synchronous applications.

2. The Configurable Logic Blocks (CLB) represents the basic logic elements for FPGA which provide combinational and synchronous logic with distributed memory shift register capability.
3. The Block RAM offer flexible bit dual-port RAM cascaded from larger memory blocks. The block RAM contains optional programmable FIFO logic to increase the device utilization in implementation terms.
4. The DSP Slices, dedicated multipliers, integrated adder and accumulator.
5. The digital clock manager offer self-calibration and clock multiplication/ division process.
6. General routing matrix (GRM) offer array of routing switches between all components.

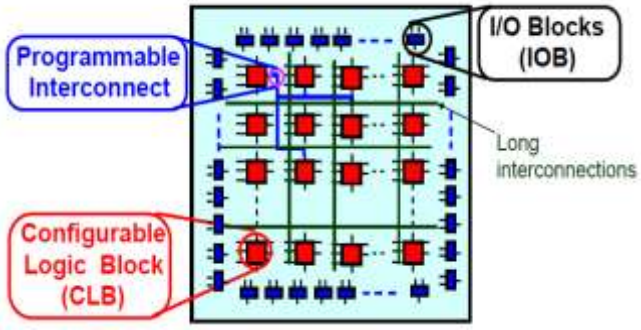


Figure 1: General FPGA Architecture [15]

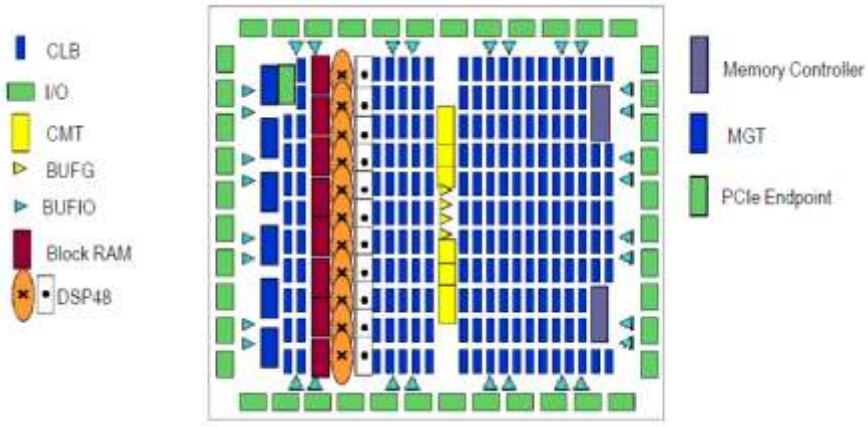


Figure 2: FPGA architecture elements [15]

FPGA Optimization and Flow Chart Design

In this section, the optimized design flow of configurable Vertex-4 FPGA is developed and described in detailed. In general, the flow of design and implementation can be divided into 2 parts specifically software and hardware, as shown in Figure 3. In the software part, the proposed model is designed and simulated using MATLAB/ Simulink block set with floating point numbering values. The HDL Netlist of DSP model is then designed in system generator with fixed point numbering values. The HDL module of activation system and HDL Netlist is integrated using ModelSim software programs to generate the integrated HDL. The synplify Pro software is used to synthesis the integrated HDL into FPGA pin assignments. In the hardware part, the ISE software is

used to implement the proposed model in three process called translate, map, place & route. The verification of hardware output with software simulation output is done to verify the exact correlation between the waveforms.

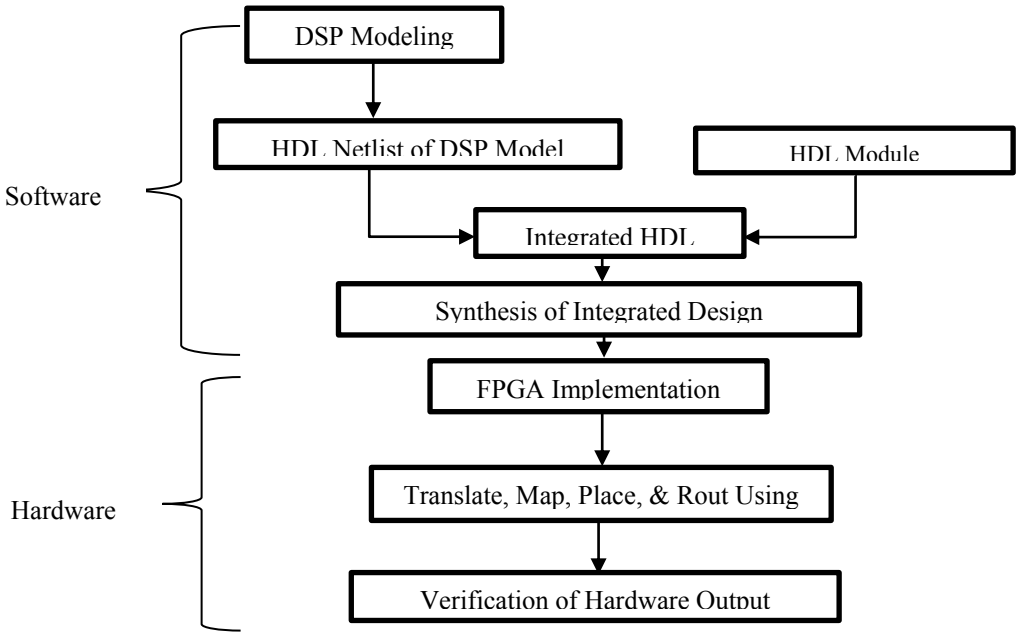


Figure 3: Proposed FPGA design flow

HDL of Integrated Design

Consider the implementation of the DSP models integrated with setup configuration module using FPGA and P240 Analog Module in real time. The main clock enable of DSP model is disabled during the transfer of SPI codes to ADC and DAC in P240. Controlling the main clock enable would be easier than clock enable clear which requires additional logics to adjust sampling phase of all the multi-sampled data when de-asserted. The software part can be viewed as a composition of processes run by each software tool. The details development flow of design and implementation of FPGA is observed in Figure 4. The first stage in the general flow of design and implementation is modeling the configurable modeling using digital signal processing (DSP) algorithms in high level graphical user interface (GUI). The generated files used for the following processes in the ModelSim, Synplify Pro and Xilinx ISE environments are listed in Table 1.The high level GUI is Simulink environment contained in MATLAB software with add-in of Xilinx System Generator software is used in this research. All DSP models contained in the proposed flow are built by connecting the blocks provided by libraries of Simulink Block set and Xilinx Block set in this GUI. The Generate button on the GUIs of System Generator blocks represent the first step in HDL design of the proposed model as compiled of HDL netlists written in Verilog codes including the respective test-benches, and stored in the folders called “netlis” under the current project directory.

Table 1: Requirements File of System Generator Block

Descriptions	Type	Name	Simulation
HDL netlists of DSP core designs	Verilog(.v)	Dsp	ModelSim, Synplify Pro
HDL netlists Clock		dsp_cw	ModelSim, Synplify Pro
Test-bench file. Generate clock signals, acquire inputs.		dsp_tb	ModelSim
List of binary words stored in Block RAM.	Memory interface file (.mif)	single_port_block_memory	ModelSim, Synplify Pro, Xilinx ISE
Netlists function of multiplier, BRAM and FIFO created by CORE Generator program.	electronic design interchange format (EDIF) netlist(.edn)	Multiplier single_port_block_memor, FIFO	Xilinx ISE
Constraints of multiplier and FIFO created by CORE Generator program.	native generic constraint(.ngc)	Multiplier…, FIFO…	Xilinx ISE

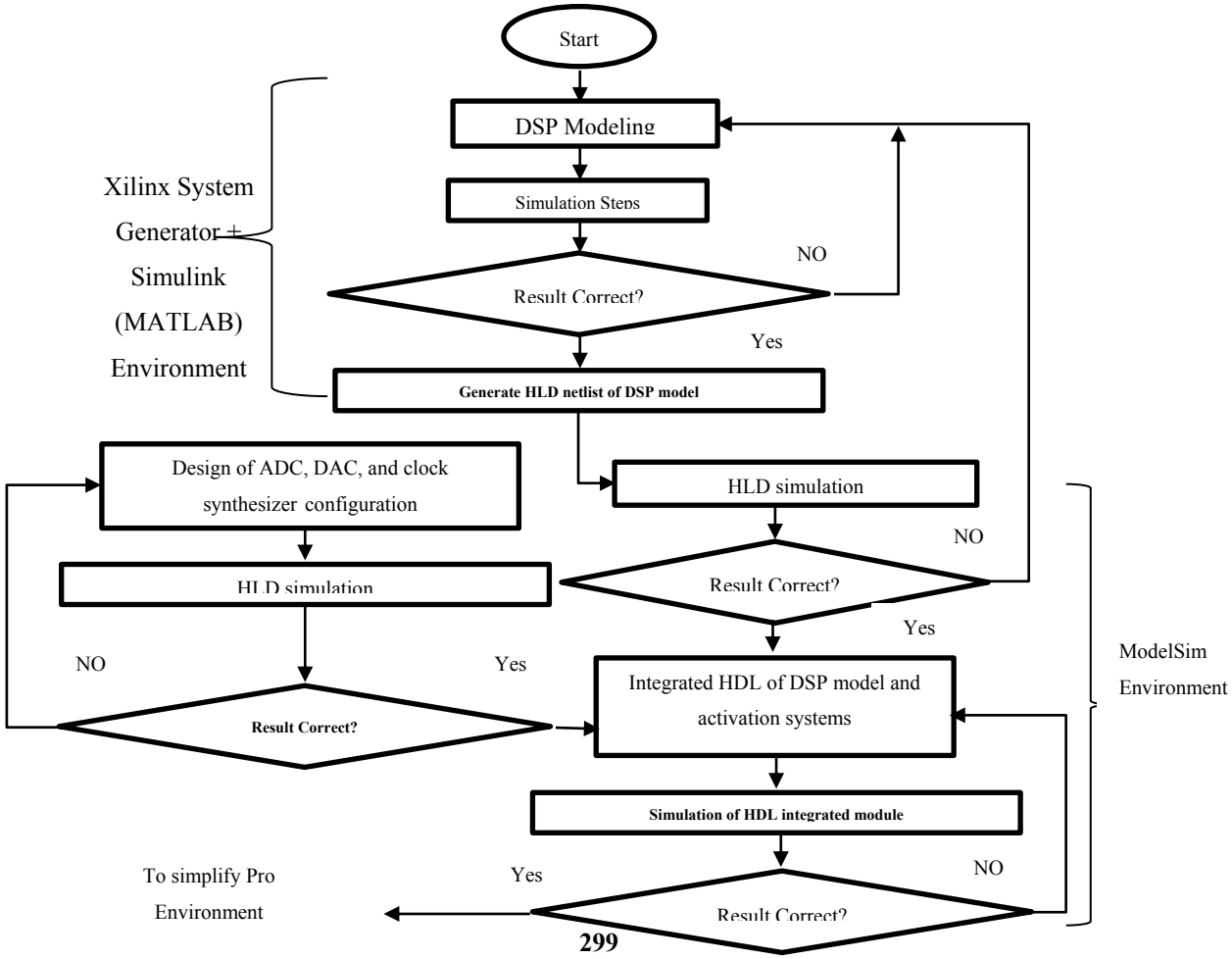


Figure 4: HDL code design of integrated module

Synthesis of HDL Code

Xilinx ISE software contains a Xilinx Synthesis Technology (XST) program could be used to synthesize the HDL netlist generated from System Generator only. Though, the synthesis of HDL integrated modules of DSP model with setup configuration can be performed by using Synplify Pro software, in two stages. The first stage, represented by HDL integrated module compiled to Xilinx FPGA structural elements and then optimized to be as small as possible to improve circuit performance. The second stage is the optimized integrated module and mapped to Xilinx FPGA logic components using architectural-specific techniques. The synthesis process of integrated module is error free in terms of functionality and timing, FPGA pins locations are assigned accordingly by referring to Avnet Memec Company as show in Figure 5.

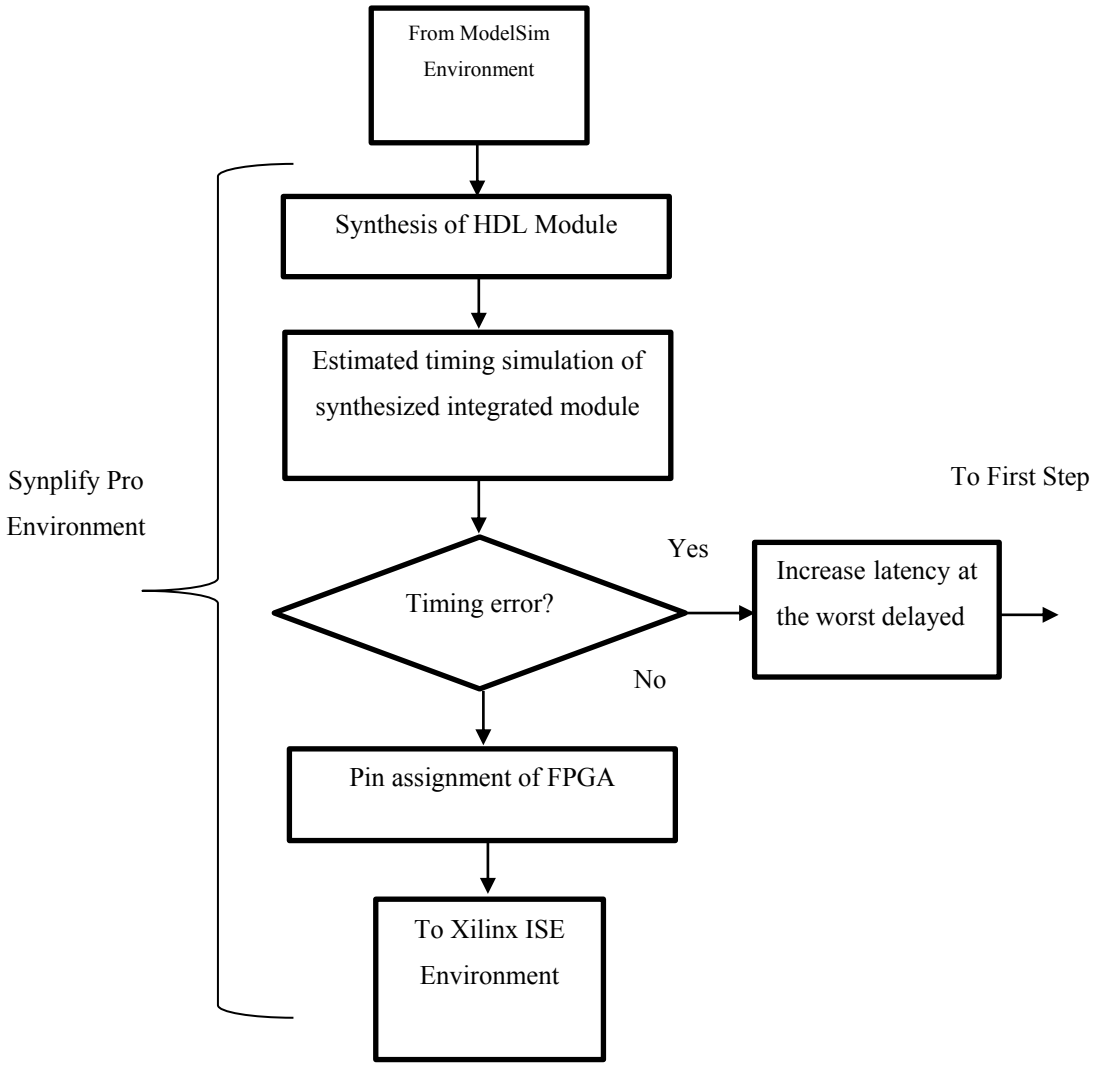


Figure 5: Synthesis and pin assignment of integrated module

Implementation steps

The synthesis output files required by Xilinx ISE software are in electronic design interface file (EDIF) and user constraints file (UCF) formats, representing the optimized netlist of synthesized integrated module, and timing constraints with FPGA pin assignment. The synthesized integrated module of DSP is implemented into Xilinx Virtex-4 FPGA by using ISE program which consist translate, map, place & route process as illustrated in Figure 6 and Figure 7.The fully routed NCD file is converted to configuration bit-stream file using BitGen program, and then downloaded into Virtex-4 FPGA via JTAG program cable using iMPACT program. Before performing the last step of Bit Generation and Program Download, the results of Translate, Map and PAR processes should indicate no errors in order to ensure the validity of implementing the synthesized integrated module of DSP model into the Virtex-4 FPGA.

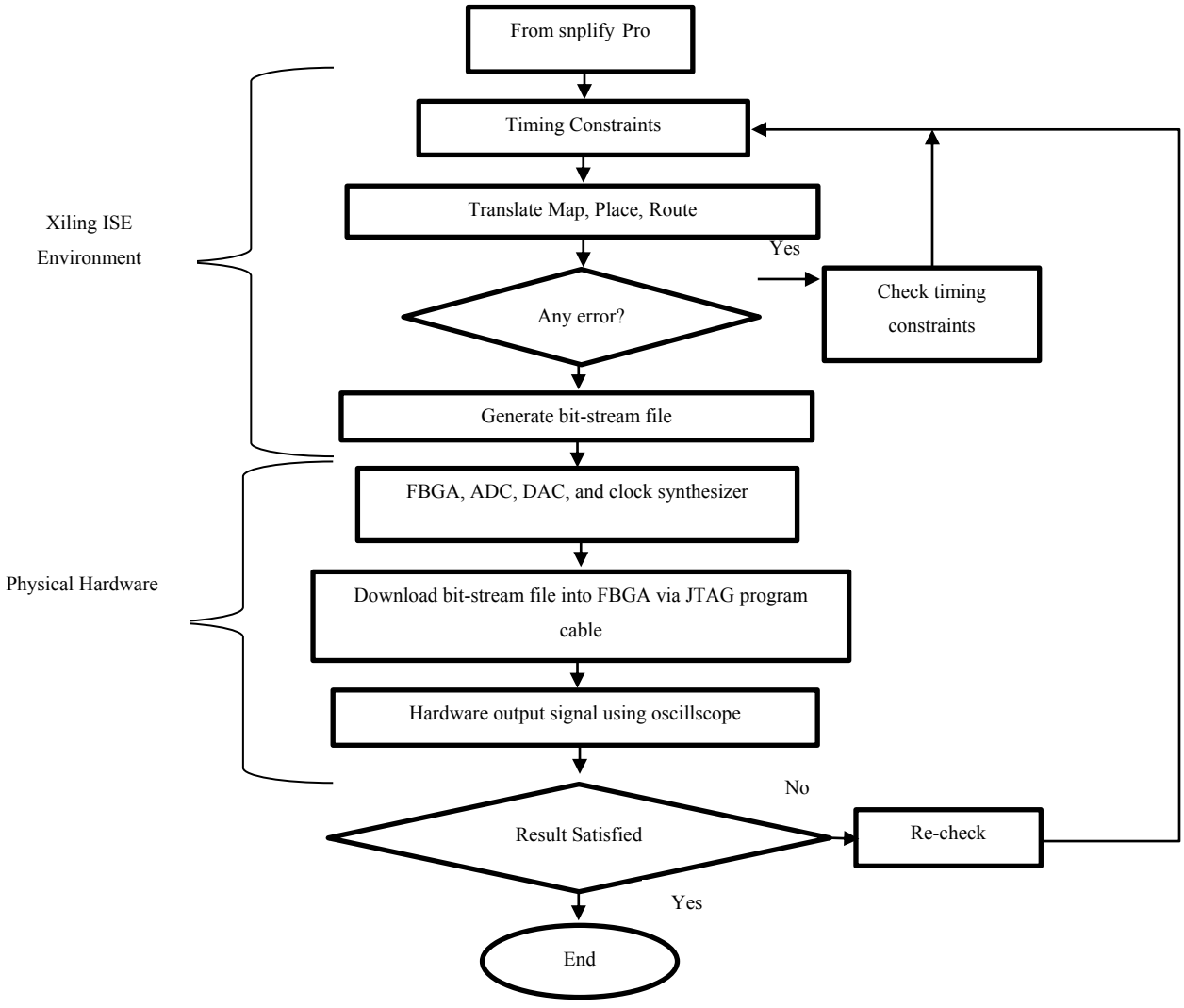


Figure 6: Translate, Map, Place &Route and Bit generate step

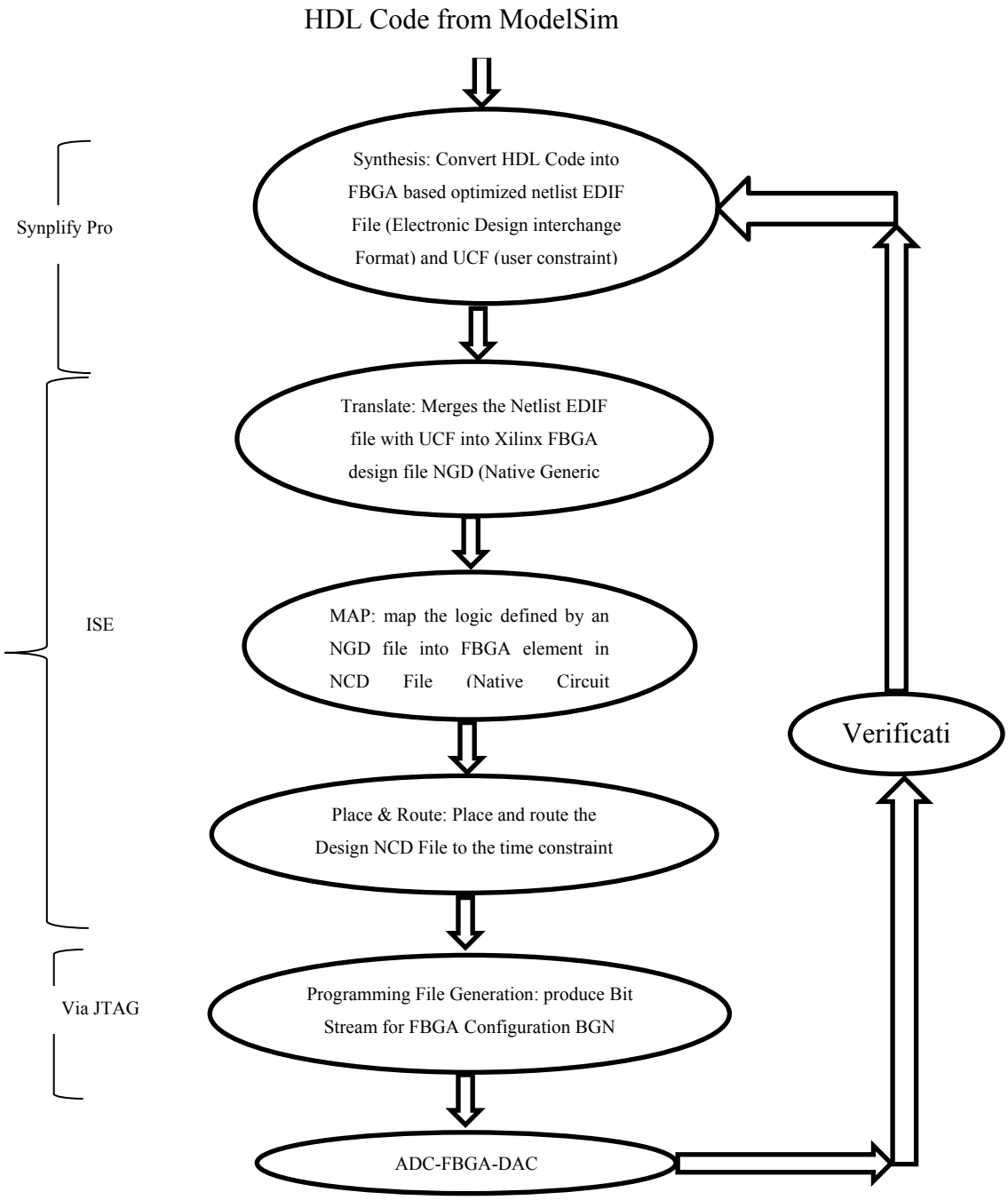


Figure 7: Synthesis file and ISE generated electronic file

FPGA Interfacing with ADC and DAC

Interfacing FPGA with ADC and DAC should be taken into account to avoid undesired data losses before and after FPGA processing. Consequently, this section presents the design of setup configuration module for all the configurations required by ADC, DAC and FPGA onboard ICS8442 clock synthesizer. The setup configuration module is written in Verilog codes as HDL module ("ADC_DAC_ICS.v") and simulated in ModelSim environment. The configurations of ADC and DAC contained in P240 Analog Module, timing characteristics of serial programming interface (SPI)for two Texas Instruments (TI) ADS5500 (14-bit, 125 MSps) ADCs and single TI DAC5687 (16-bit, 500 MSps) dual-channel DAC, have to be satisfied.

To synchronize the ADC_SCLK and DAC_SCLK, clock for both SPI processes must not exceed 20 MHz. Therefore, 100 MHz clock signal from FPGA onboard, the Low Voltage Transistor-Transistor Logic (LVTTL) oscillator is divided by 5 frequency divider in Verilog codes to generate 20 MHz clock signal. Subsequently, the 20 MHz clock signal is further divided by 2 to become 10 MHz which equals to the values of ADC and DAC SPI Clock. The FPGA onboard ICS8442 clock synthesizer is set to parallel mode and it is simpler than that of P240 Analog Module in order to reconfigure FPGA board.

The DSP model starts running with 100 MSps sample rate after completing setup configuration module. Consequently, manually setting the input Select using FPGA onboard red DIP switch, the DSP models will perform baseband, for 16-QAM modulator. The 100 MHz differential clock signal for DAC5687 DAC at CLK1/C pins is used as input data capturing rate, while the 400 MHz differential clock signal at CLK2/C pins is used as DAC sample rate, thus resulting in interpolation rate of 4, for both DAC Channel A and B. The digital in-phase and quadrature signals for transmitter or digital smoothed bit and 0 for the receiver, will be sent from Data Out A and B to DAC_DA[15:0] and DAC_DB[15:0] pins (referring to of DAC respectively, and converted to a pair of analog output signals by single DAC5687 DAC, and 2 sets of low-pass 5th order Bessel re-construction filters and 50 Ω coupled transformers.

To display the real-time results, the analog output signals are connected to oscilloscope for verifying system functionality of the integrated DSP module through testing and measurements, as illustrated in Figure 8. The input reset of the DSP Model of transmitter is activated by pressing push button on the first Virtex-4 MB board to capture initial real-time results of the configurable DSP model. While the input reset of the DSP Model of receiver is activated first and hold until the input reset of the DSP Model of transmitter is finished activating, by pressing push buttons on the second and first Virtex-4 MB Board respectively, to capture initial real-time results of the configurable receivers.

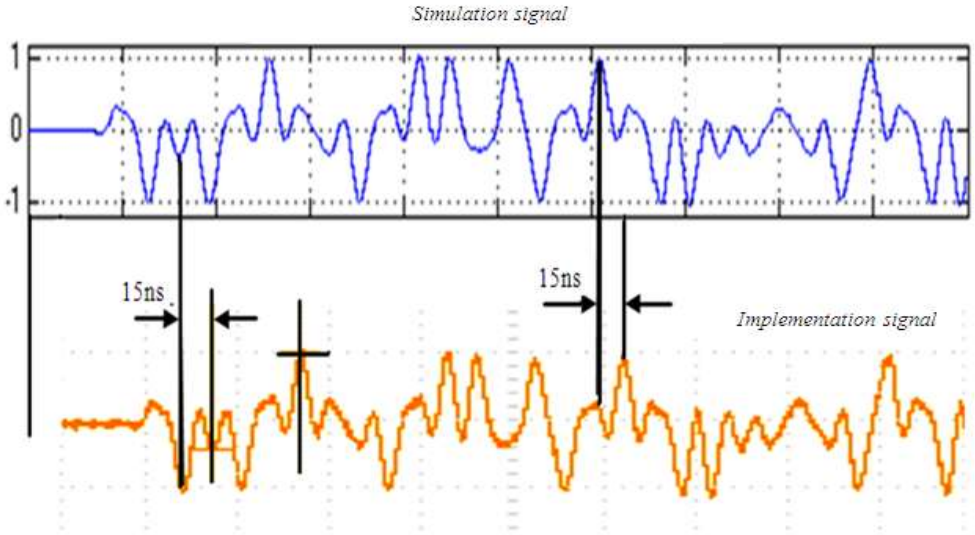
Simulation and Implementation Results

The simulation and implementation results of DSP transceiver 16-QAM in-phase and quadrature signals shows an identical in the time and amplitude with 15 ns difference due to printed circuit board (PCB) nevertheless, these errors are acceptable as shown in Figure 8.

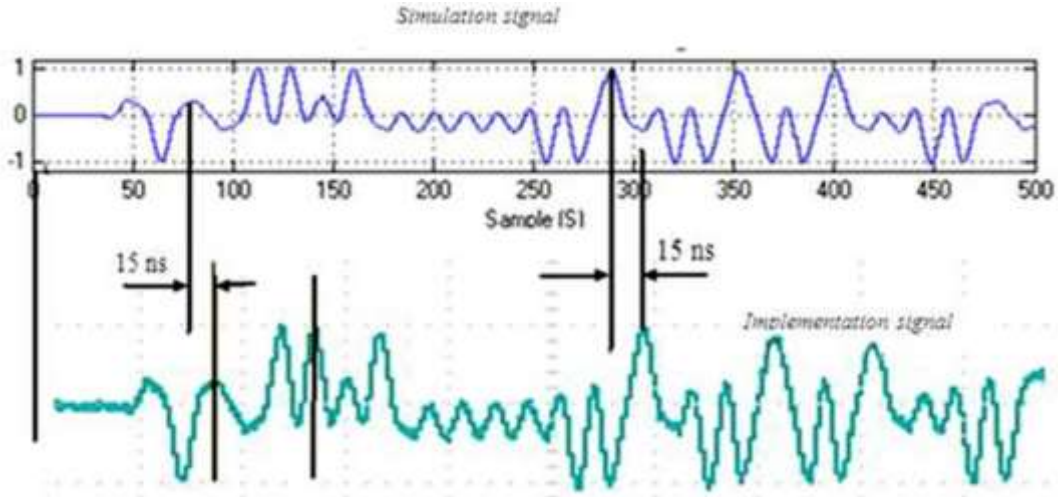
The project status and device utilization summary of proposed transceivers is reported by the ISE program, as shown in Table 2. These tables provide the total number of slices and LUTs used in this design, which represent the total area used in FPGA. Depending on the number of devices used in FPGA, the total power consumption in the proposed model implementation can be seen, according to the number of slices and LUTs. The percentage of used logic elements to the available logic elements is calculated as follow:

Utilization % = $\frac{\text{used logic elements}}{\text{available logic elements}} X\ 100$, for examples:

Utilized number of Slice Flip Flop = (14436/30720) x 100 = 46%
Utilized number 4-input LUTs = (8322/30720) x 100 = 27%
Utilized number of occupied Slices = (7326/15360) x 100 = 47%
Utilized number of bonded IOBs = (93/448) x 100 = 20%



(a) Inphase signal



(b) quadrature signal

Figure 8: Real-time and simulation Results of16-QAM DSP transceiver.

Table 2: Device Utilization Summary of 16-QAM transmitter

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	14,436	30,720	46%	
Number of 4 input LUTs	8,322	30,720	27%	
Logic Distribution				
Number of occupied Slices	7,326	15,360	47%	
Number of Slices containing only related logic	7,326	6,187	100%	
Number of Slices containing unrelated logic	0	6,187	0%	
Total Number of 4 input LUTs	10,290	30,720	26%	
Number used as logic	8,733			
Number used as a route-thru	210			
Number used for Dual Port RAMs	42			
Number used as Shift registers	176			
Number of bonded IOBs	93	448	20%	
Number of BUFG/BUFGCTRLs	6	32	12%	
Number used as BUFGs	6			
Number used as BUFGCTRLs	0			
Number of DSP48s	6	192	2%	
Number of RPM macros	1			
Total equivalent gate count for design	198			
Additional JTAG gate count for IOBs	6,474			

CONCLUSIONS

This paper present the developments of FPGA design methodologies for DSP transceiver model with configurability of multi digital modulation such as expanding multi functionalities applicable for more advanced wireless communication systems. A novel technique has been used to reduce hardware size (FPGA area) for implementing the configurable DSP model, by incorporating the universal features common by two or more single-modulation structures of baseband modem functions, such as mapper and pulse shaping filter in baseband modulator, matched filter, timing recovery and demapper in baseband demodulator. The new methodologies is incorporated with superposition principle of digital linear modulation, poly-phase interpolator architecture with optimization, and acquisitions of timing error and optimum sampling instant, to compress the structures of symbol mapper and demapper. The design methodologies development of DSP models are designed and simulated in Xilinx System Generator /Simulink, ModelSim, Synplify Pro and Xilinx ISE environments. Although in hardware development, the configurable DSP transceiver is implemented using Xilinx Virtex-4 FPGA MB board and P240 Analog Module (ADC and DAC) for testing and measurements. The FPGA utilization of the proposed configurable design flow has been reduced by 46% in slices and 27% in LUTs, as compared to the current design. Simply, baseband processing segment of DSP model has been implemented in this paper, therefore future researches would be focusing on source processing, bit-stream processing, IF processing and RF alteration, for a complete transceiver implementation. The projected configurable design flow can be more modified and enhanced for superior performance of FPGA design.

REFERENCES

[1] C Dick, et al., "Architecture and Simulation of Timing Synchronization Circuits for the FPGA Implementation of Narrowband Waveforms", Proceedings of Software Defined Radio Technical Conference and Product Exposition, 13-16 , pp. 1-6, IEEE explorer, USA, 2009

[2] Hatai, I.and Chakrabarti.,"Parameter Controlled Reconfigurable Baseband Modulator for SDR Architecture", Proceedings of the 2nd International Conference on Mechanical and Electronics Engineering (ICMEE), vol. 1, 1-3, pp. 29-33, IEEE explorer,Japan, 2010

[3] Popescu, S.O, et al.,"Review of PSK and QAM – Digital modulation techniques on FPGA", in the Proceedings of International Joint Conference on Computational Cybernetics and Technical Informatics (ICCC-CONTI), 27-29, pp. 327-332, IEEE explorer, Romania , 2010

[4] Rouphael, T. J. RF and Digital Signal Processing for Software-Defined Radio: A Multi-Standard Multi-Mode Approach. MA: Newness, Elsevier, 2009

[5] Amrita Sahaand Amitabha Sinha, "An FPGA Based Architecture of a Novel Reconfigurable Radio Processor for Software Defined Radio", in the Proceedings of International Conference on Education Technology and Computer (ICETC), 17-20, , pp. 45-49, Singapore, 2009

[6] Song, W., and Yao, Q., Design and Implement of QPSK Modem Based on FPGA, in the Proceedings of 3rd IEEE International Conference on Computer Science and Information Technology (ICCSIT), vol. 9, 9-11, pp. 599-601, China, 2010

[7] Tachwali Y. , et al.,"Configurable symbol synchronizers for software-defined radio applications". Journal of Network and Computer Applications, 32(3), pp. 607-615, 2009

[8] Xuan-Thang Vu, et al.,"16-QAM Transmitter and Receiver Design Based on FPGA", in the Proceedings of 5th IEEE International Symposium on Electronic Design, Test and Application (DELTA), 13-15, pp. 95-98, Vietnam, 2010

[9] Wali, M. k., Al-shakarchi, Q. M., AL -Shamma, N. K., "Design and Implementation of Electronic Board Advertisement Based on Microcontroller PIC16F887and Multi Character Button Keypad" Eng. & Tech. Journal, Vol. 31 , No. 1 , 2013.

[10] Dr. Majid S. Naghmash, "Design and Implementation of Programmable Multi-Mode Digital Modulator for SDR Using FPGA", Eng. & Tech. Journal, Vol, 32, Part (A), No. 7, 2014

[11] Yahia Said, et al.,"Real Time Hardware Co-simulation of Edge Detection for Video Processing System", IEEE Explore, 978-1-4673-0784-0/12/, 2012

[12] Xiaojing Zhang, et al., "Design and Implementation of a Multichannel Pulse Compression System Based on FPGA" journal of computers, vol. 8, no. 1, january 2013

[13] Sparsh Mittal, et al. " System Generator:The State of-art FPGA Design tool for DSP Applications", Indian Institute of Technology Roorkee, Department of Electronics and Computer Engineering, India 2005

[14] Yahia Said, et al., "FPGA-based Architectures for Image Processing using High-Level Design", wseas transactions on signal processing, Volume 11, 2015

[15] Md. Abdul Latif Sarker, Moon Ho Lee, " Synthesis of VHDL Code for FPGA Design Flow Using Xilinx PlanAhead Tool", Journal of Electronic Systems Volume 2 Number 4, PP. 165-175, December 2012