Systolic Digital Filter Architecture for Signal Identification

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Abstract

The concern of the paper is to use novel approach to identify the signal. The approach represents the relation ship between the input and output through the systolic array structure, and drivers the relation directly from the transfer function of the digital filter, so that signal identification can be effectual in real-time. The paper proposes a one-dimension (1-D) systolic array architecture of infinite and finite impulse response (IIR &FIR) digital filters. The proposed architecture is employed in real-time signal identification .This was verified after the identification process of the signal in real-time by applying the proposed structure in simulink.

الخلاصة

ينصباهتمام البحث في استخدام تقريب حديث العهد لتعريف الاشارة في التقريب المقترح تم ايجاد علاقة بين الدخل والخرج بواسطة المصفوفات الانقباضية ، حيث تمت عملية الاشتقاق مباشرة من دالة التحويل الخاصة بالمرشح الرقمي بنوعية الاستجابة النبضية المنتهية والامنتهية ، ومن خلال هذا التقريب تم تعريف الاشارة في الزمن الحقيقي 0 في البحث تم اقتراح المصفوفة الانقباضية احادية البعد لتعريف الاشارة في الزمن الحقيقي 0 تم التحقيق من التقريب المقترح بمحاكاة السيميلنك 0

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1- Introduction

Recently, digital filters have been widely researched in a variety of digital signal processing (DSP) applications, such as signal identification [1-4]. Although 1-D digital filters can be simulated on a general-purpose computer, it seems unlikely to process input signals in real-time due to a large amount of computation. Therefore, a specific application integrated circuit realization of 1-D digital filters appears. One of the designs that play an important role for the most attractive structures for a VLSI design is the systolic array architecture [5-6]. It is characterized by synchronization, a high degree of modularity and regularity, local broadcast/communication, concurrency, and extendibility. When a large number of processing elements (PEs) work together, data communication becomes more significant. In recently developing VLSI technologies, the global broadcast makes a

significant impact upon speed in the circuit level. Therefore, the local broadcast of systolic arrays is advantageous in reducing the global broadcast impact. Systolic architectures for digital filters have existed in [7]. It is observed here that the input and the output signals globally broadcast among the existing structure. The paper is organized as follows: The 1-D systolic digital filter architecture with global broadcast is proposed in section 2. The results are tabulated in terms of global broadcast, the input data are fed in one value at a time, and broadcast to all the processing elements in row-wise. At the end of each derivation, concisely is shown the Simulink diagram that shows the presentation of the signal identification process.

2- The Systolic architecture design of IIR

The general transfer function of a 1-D IIR digital filter can be represented as [8]

$$H(z)=\frac{\sum_{i=0}^{N} a_i z^{-i}}{1-\sum_{i=0}^{N} b_i z^{-i}} \qquad (1)$$

where $b_0 = 0, a_i$ s well as b_i are filter's coefficients. To demonstrate the design procedure, the order of the IIR digital filter will be assumed to be (2). The 1-D filter is given by Eq.(1), which can be expressed in recursive form as:

$$y(n)=\sum_{i=0}^{N} a_i x(n-i)-\sum_{i=1}^{N} b_i y(n-i). \qquad (2)$$

The realization procedure is as given below:

1- Referring to Eq.(2), it can be rewritten for N=2 as follows:

$$y(n) = a_0 x(n) + a_1 x(n-1) - b_1 y(n-1) + a_2 x(n-2) - b_2 y(n-2) \quad (3)$$

2- The expression for $y(n)$ can be realized as shown in Fig.(1). The structure of the processing element (PE) is shown in Fig.(2).

3- Assuming the sequence of input data is as follows:

$x_0, x_1, x_2, ..., x_M$. (where M is the row size of the 1-D input data).

after each clock.

At time

$$1: y_0 = a_0 x_0 , y' = a_1 x_0 , y'' = a_2 x_0 \quad (4)$$

At time 2: $y_1 = a_0 x_1 - b_1 y_0 + a_1 x_0$,

$$y' = a_1 x_1 - b_2 y_0 + a_2 x_0 , \quad y'' = a_2 x_1 \quad (5)$$

At time 3: $y_2 = a_0 x_2 - b_1 y_1 + y'$,

$$= a_0 x_2 - b_1 y_1 + a_1 x_1 - b_2 y_0 + a_2 x_0 ,$$

$$= (a_0 x_2 + a_1 x_1 + a_2 x_0) - (b_1 y_1 + b_2 y_0) \quad (6)$$

etc.

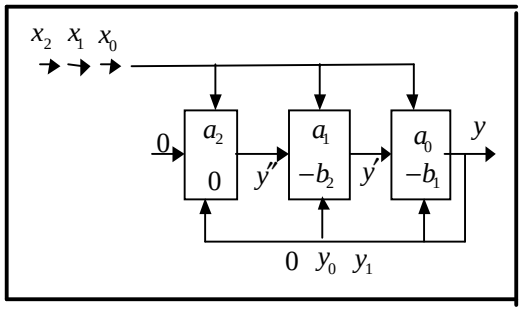


Fig.(1)Realization of 1-Dsecond order IIR filter.

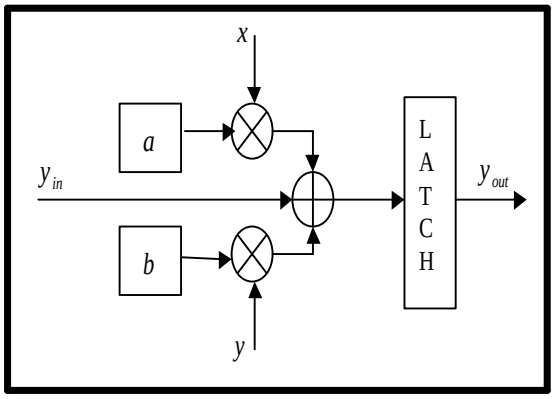


Fig.(2) The processing element realization

The modularity of the systolic structure is clear, since the requirement of modification to accommodate higher order filters is only an increase in the number of PE's.

The realization of the designed filter is illustrated in Fig.(3). This was achieved by using the simulink package. The result is shown in Fig.(4). The output for a sine input

from the signal generator is the same as the input. This has been obtained after suitable choosing of the coefficients of

the filter. In this case, the principle of trial and error technique was used.

The PE's in Fig.(5) are identical in the design, and the structure is highly modular. Hence, in order to help the structure accommodate higher order filters, the addition of more PE's is required.

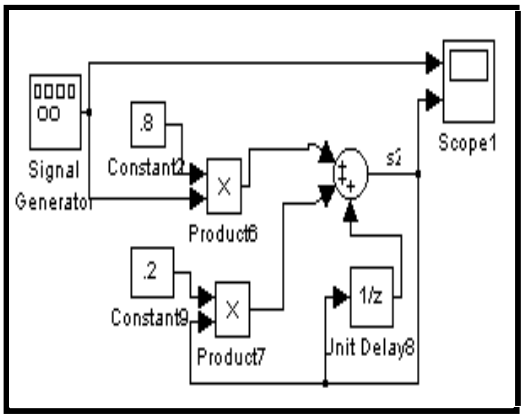


Fig.(3) Simulink realization of the systolic structure of IIR filter

3- The systolic architecture design of FIR

Now, the 1-D FIR realization procedure will be presented under systolic implementation. The general transfer function of a 1-D FIR digital filter can be represented as well.

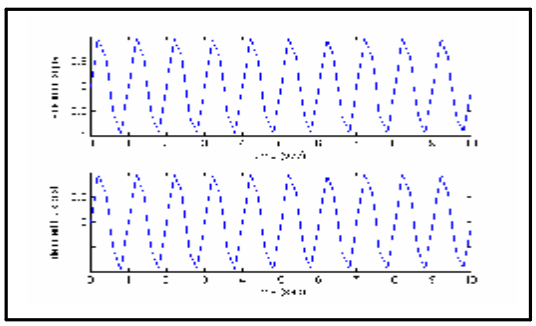


Fig.(4) The result of the IIR systolic realization

$$H(z) = \sum_{i=0}^{N} a_i z^{-i} \qquad (7)$$

The 1-D FIR digital filter given in Eq.(7) can be expressed in recursive form as follows:

$$y(n) = \sum_{i=0}^{N} a_i x(n-i) \qquad (8)$$

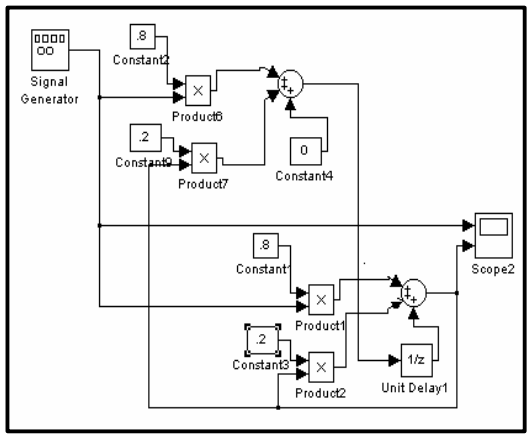


Fig.(5) The Expandable property of the systolic array implementation.

The realization of the 2nd order filter (N =2) is used to identify the signal in real-time, and it is implemented by using simulink. The realization of a 1-D 2nd order FIR filter is shown in Fig.(6). The structure of a processing element is shown in Fig.(7). Again, the sequence of input data as $x_0, x_1, x_2, ..., x_M$.,Where M is the row size of the 1-D input data, is assumed.

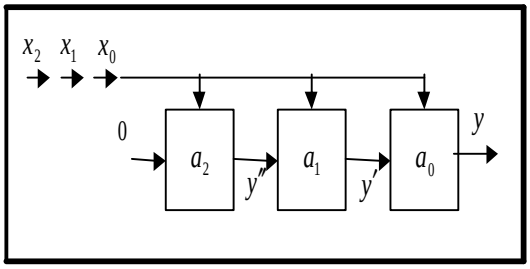


Fig.(6) Realization of a 1-D 2nd order FIR filter

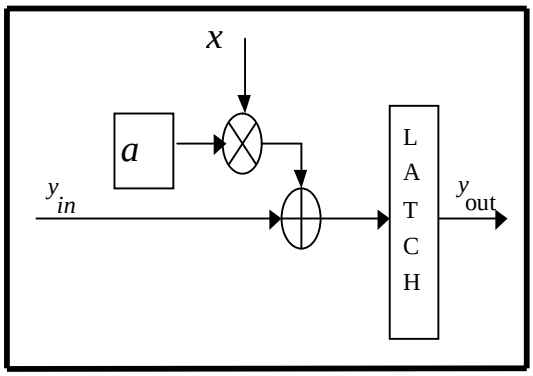


Fig.(7) The structure of the processing element of the FIR filter

The realization procedure follows the same steps as that for $y(n)$ and are given below:

TIME 1 $y_1 = a_0 x_0, y_1' = a_1 x_0, y_1'' = a_2 x_0$ (9)

TIME 2 $y_1 = a_0 x_1 + y_1' = a_0 x_1 + a_1 x_0$, $y_1' = a_1 x_1 + y_1'' = a_1 x_1 + a_2 x_0, y_1'' = a_2 x_1$ (10)

TIME 3 $y_1 = a_0 x_2 + a_1 x_1 + a_2 x_0, y_1' = a_1 x_2 + y_1'' = a_1 x_2 + a_2 x_1, y_1'' = a_2 x_2$ (11)

TIME 4 $y_1 = a_0 x_3 + a_1 x_2 + a_2 x_1, y_1' = a_1 x_3 + a_2 x_2, y_1'' = a_2 x_3$ (12)

TIME 5 $y_1 = a_0 x_4 + a_1 x_3 + a_2 x_2, y_1' = a_1 x_4 + a_2 x_3, y_1'' = a_2 x_4$ (13)

etc.

The above structure is realized under simulink as shown in Fig.(8). The output from the circuit is the same as its input signal shape after tuning the coefficients of the filter by trial and error principle, as shown in Fig.(9).

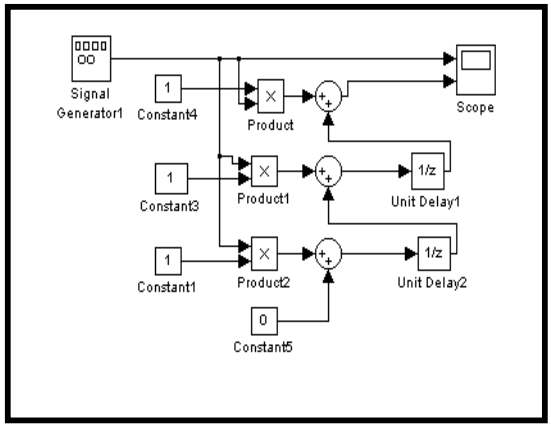
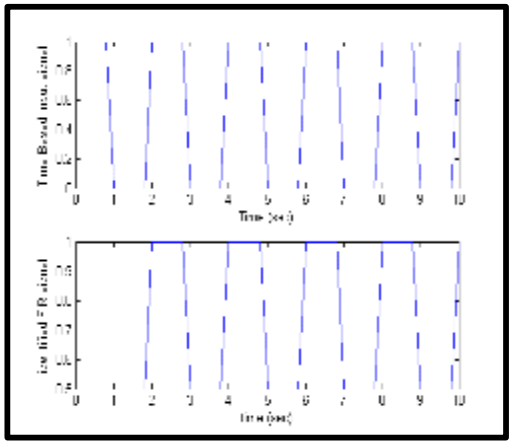


Fig.(8) Simulink implementation to the FIR filter.



Fig(9) The actual and identified response to the time based signal for FIR filter.

4- Signal Identification

As a practical example, the identification process is formulated using the state space approach in which the system is described by a set of

variables known as the state. The state contains all the information regarding the system at a certain point in time. This information should be the least amount of data that is required to know about the past behavior of a system in order to predict its future behavior. Hence, the future state outputs may be deduced given the present and future values of the input. Then, this architecture was realized by using the simulink package, together with one of the designed filter, e.g. the FIR filter. The output of the gathered system gives an identification to the systems' state. The proposed structure for both digital filters can be implemented in real time to the identification process, as well. Fig.(10) illustrates the simulink implementation of the given system. It was gathered with FIR digital filter design under systolic array structure. Fig.(11) demonstrated the resulted identified output together with the inputted state. It is clear from all these plots, that the proposed architecture gives the correct identification process to the input.

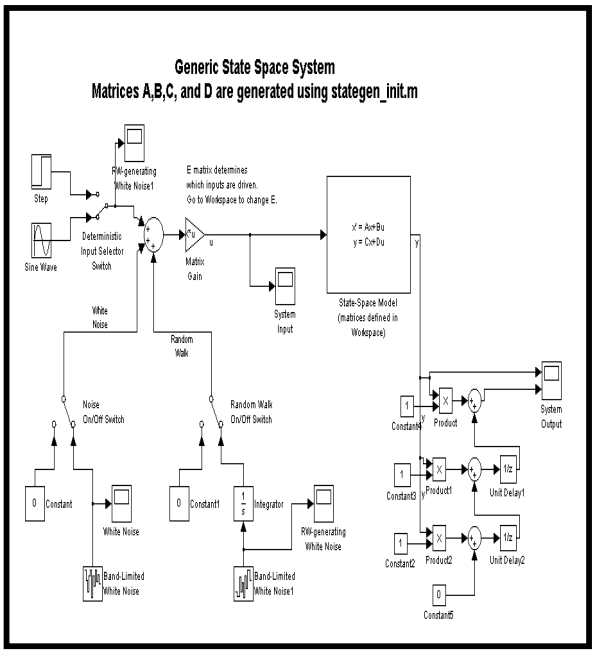


Fig.(10) An example to demonstrate the capability of the designed filter in the identification process.

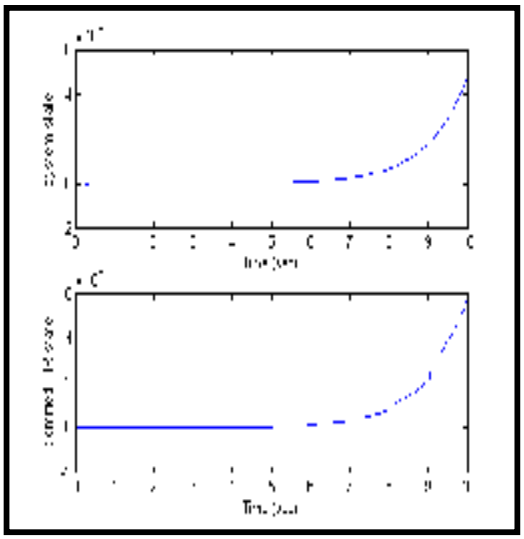


Fig.(11) The actual and the identified state of the example using the FIR systolic filter .

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