Wavelet and Wavelet Packet Transform Realization Using FPGA

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Abstract

This paper provides a new algorithm for the evaluation of WAVELET TRANSFORM (WT) and the WAVELET PACKET TRANSFORM (WPT) using Field Programmable Gate Array (FPGA).

FPGA realization is the most recent category, which takes the place in the implementation of DSP applications, and it had proved the capability to handle such jobs and supports the necessary needs of scalability, speed, size, cost, and efficiency.

The WT & WPT coefficients are depend upon the multi resolution analysis approach using HAAR or DUBCHIES2 bases functions. Next, coefficients are evaluated in the FPGA card through its implementation using logical circuits using a specified electronic library kit.

الخلاصة

يتناول هذا البحث خوارزمية من اجل تحليل تحويل المويجه و كذلك المويجه كاملة التحويل باستخدام تقنية الـ (FPGA) .

إن هذه التقنية تستطيع تمثيل الكثير من تطبيقات معالجة الاشاره الرقمية و لها القابلية لتحقيق وظائف و دعم احتياجات مثل هذه اللوحات من حيث السرعة و الحجم و الكلفة و الكفاءة .

لقد تم الاعتماد في حساب معاملات تحويل المويجة و تحويل المويجة الكامل بالاعتماد على عملية التحليل المتعدد المستويات باستخدام دوال القاعدة نوع (Haar) او (db 1) ثم تم تحليل و تمثيل هذه المعاملات على لوحة الـ(FPGA) و استخدام دوائر منطقية قياسية مبنية في أجهزة مكتبية إلكترونية .

Keywords

FPGA, Wavelet Transform, Wavelet Packet Transform.

1: Introduction

The advent of Field Programmable Gate Array (FPGA) technology has enabled rapid prototyping of digital systems. Even though the principles of good logic design are very much relevant to any FPGA- based design, the need to rapidly prototype a large- scale digital system necessitates new design methodologies and the use of computer aided design (CAD) tools.

There is a wide variety of Field

Programmable Gate Array as shown in table (1), some of these devices are actually programmable logic devices (PLD's) with specific expansion that make them larger and more flexible than traditional PLD's. [14]

Table (1): - Examples of FPGA

Production	Capacity	Architecture	Basic cell	Programming method
Actel	2000-8000	Gate array	MUX	Antifuse
Algotronix	5000	Sea-of-gates	Functional	SRAM
Altera	1000-5000	Extended PLA	PLA	EPROM
Concurrent	3000-5000	Matrix	XOR-AND	SRAM
Cross point	5000	Gate array	Transistor	Antifuse
Plessey	2000-40000	Sea-of-gates	NAND	SRAM
Quick logic	1200-1800	Matrix	MUX	Antifuse
Xilinx	2000-10000	Matrix	RAM block	SRAM

As it can be seen from the table the differences between product specifications gives wide variety in use according to the need of the user. The differences in the basic cells made the implementation of the logic modules and functions differ from one type to another to achieve certain task. [15]

The first stage in programming devices was the Mask Programmable Field Array (MPGA) and improved to form the FPGA, therefore the architecture of the MPGA is very similar to FPGA, it consist of logic blocks that can be programmable interconnected to realize different designs. The major different is that MPGA is programmed using integrated circuit fabrications to form interconnections. While FPGA is programmed via electrically programmable switches and its programming is done by end users at their site, much the same as traditional PLD's.[14]

2: Wavelet & Wavelet Packet Transform

In practical, the wavelet transform is of interest for the analysis of the non-stationary signals because it provides an alternative to the classical STFT [3,4].

For some applications its desirable to see the wave let transform as a signal decomposition onto a set of basis functions, in fact basis functions called ***wavelets*** always under lie the wavelet analysis. They are obtained from the same prototype wavelet called ***mother function*** by dilation and contraction (scaling) as well as shifting. Though the prototype wavelet can be of as a BPF of constant Q property of the other BPF's (wavelets) follows because they are scaled versions of the prototype. So, the notion of scale introduced in WT represents an alternative to frequency, leading to so call time – scale representation where this means that the signal is mapped in the time scale

plain. [2,7,8]

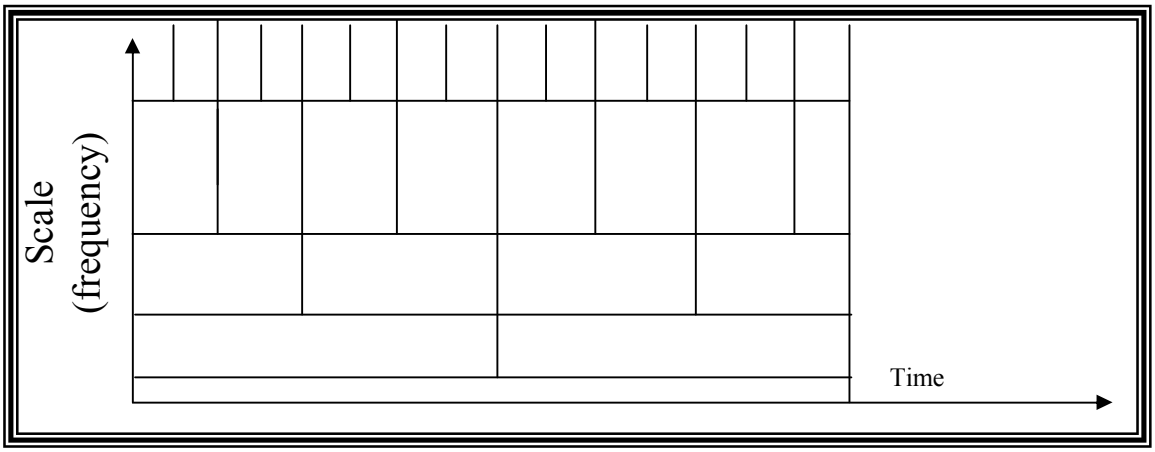

Fig. (1): -the time – scale representation in the wavelet plane

The Fourier transforms and hence the STFT use the sine and cosine as basis functions for analyzing since they are orthogonal (there is no correlation between them). The same must be applied in WT, which means that we are in need for the basis functions, which they must be orthogonal. And one more condition must be applied is the orthonormality condition in order to get a perfect reconstruction. [9,10]

For ***orthogonality*** property, the condition: -

$$\int \Phi(t)\Phi(t-m)\,dt = 0 \qquad \ldots..(1)$$

Must hold.

Where $\Phi(t)$ is the bases function.

M: is the amount of shifting one interval at a time where M not equal 0.

For the ***orthonormality*** property the condition: -

$$\int \Phi(t)\,dt = 1 \qquad \ldots..(2)$$

Must hold.

The orthonormal bases are good in localization for time and frequency and they are related to special filters for the sub band coding. These filters are lead to exact waveform reconstruction without aliasing and without amplitude and phase distortion. [9,10]

In the practical situation the filters approach is the used way for analyzing the signal frequency components. This way consists of decomposing the signal into high frequency components and low frequency components depending upon MRA. As shown in Fig. (2)

In each level the I/P information is separated into approximate information: -

$$A(j-1)(n) = \sum fj(k)\, h(k-2n) \qquad \ldots(3)$$

And into detail information: -

$$D(j-1)(n) = \sum fj(k)\, g(k-2n) \qquad \ldots(4)$$

Where j, j-1 denotes the decomposition level and the level follow it respectively, h(n) and g(n) are the HPF & LPF impulse response respectively. A's are the approximated information and the D's are the detailed information.[1]

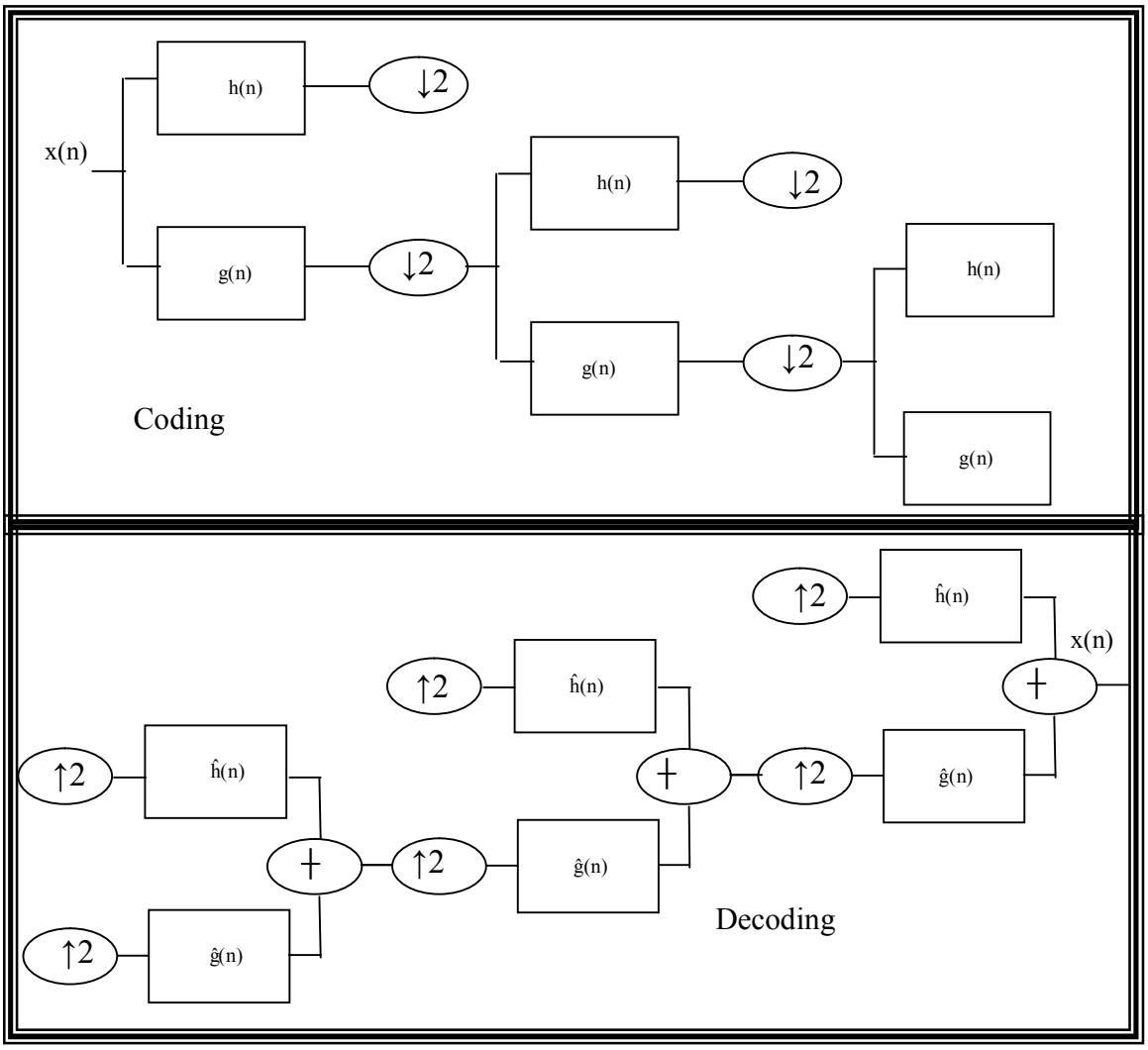

Fig. (2): - Sub-band coding scheme in terms of MRA

Inverting the above process makes the signal reconstruction. This is done by: -[11]

1) Up sampling to over come the down sampling

2) Using $\hat{h}(n)$ & $\hat{g}(n)$ which are the inverse of h (n) &g (n) respectively

Using $\hat{h}(n)$ & $\hat{g}(n)$ which are the inverse of h (n) &g (n) respectively So the reconstruction will follow the formula: -

$$Fj+1=2\{\sum fj\ (k)\ g(n-2k) + \sum fj\ (k)\ h(n-2k\ ) \quad .....(5)$$

This is called Mallat algorithm, where in this algorithm the sub-band coding scheme And since it deals with the MRA, then the filters will have constant Q factor, so the relative band width will be as shown in Fig. (3).

If we assume using FIR filters, then it tern out that the HPF & LPF are related by the formula

$$h(L-1-n) = (-1)^n g(n) \quad .....(6)$$

Where L is the filter length

$(-1)^n$ is transforming the modulation

from LPF into a HPF.[13]

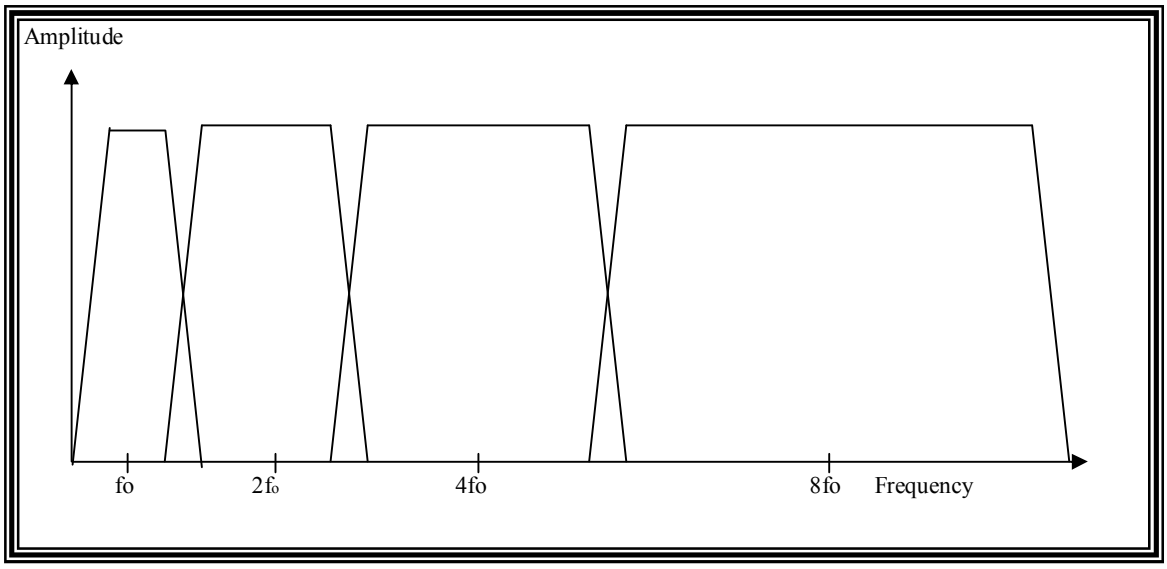

Fig. (3): - The bandwidth distribution in WT

According to Mallat MRA algorithm the classical **wavelet transform** is obtained by the decomposition (low pass filtering and down sampling). This decomposition is processed only on the low frequency branch since it is the more intelligible part as well as most of the information is in this part. This part of low frequency components with narrow bandwidth has the higher rate of information

This part takes calculation in the analyzing part of order O (N) "or its linear in complexity with the decomposition level ''. [12,13]

The complete signal decomposing both the highs as well as the low frequency branches does analyzing. Where this will make the Mallat decomposition tree to be Strictly Binary Tree (SBT) in which each branch is decomposed into two secondary branches.

In this type of decomposition we are facing complexity in the analyzing part of order O (Nlog2N) and this is result in completely evenly spaced frequency resolution, and a tree type of a logarithmic splitting and tilling of time – scale plain.

The decomposition of the high frequency components which involves wide band width is done by the same strategy (high pass filtering and down sampling) is guarantying the global view of the signal in order to diagnose the positions where the signal has or may has data in it where this kind of analysis is called the complete wavelet transform or ***wavelet packet transform***.[11,13]

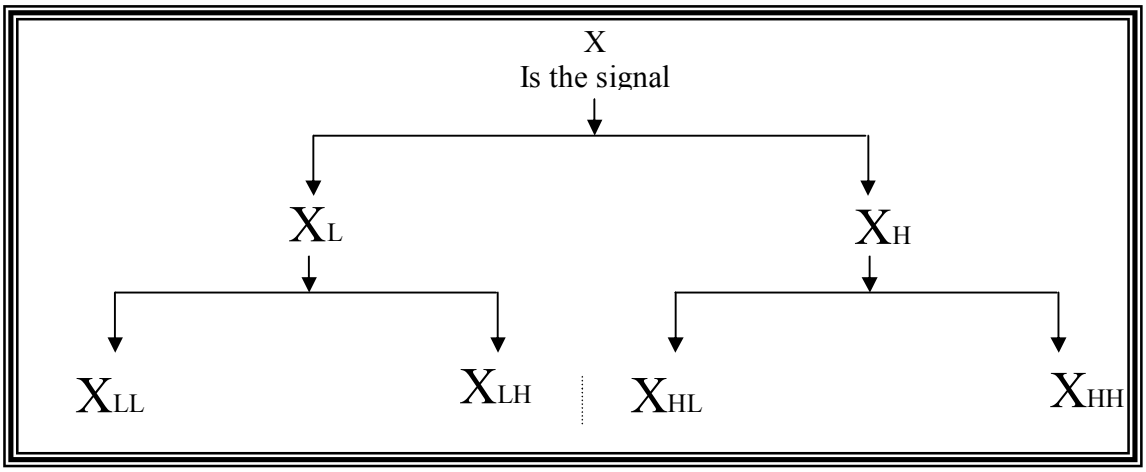

Fig. (4): - The tree representation of the WPT

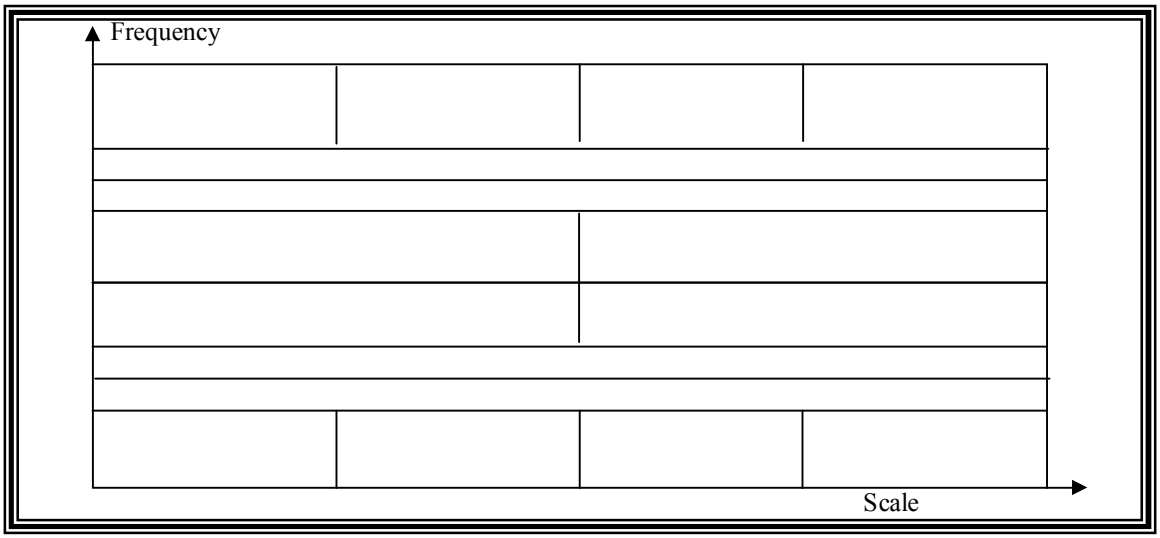

Fig. (5): - The tree representation of the WPT

3: FPGA

The Spartan FPGA family is the tremendous revolution in the electronic platforms which is made by Xilinx that gives the user high performance, abundant logic resources, and rich features set, at all an exceptionally low price. The family contains three brothers who are Spartan-II, Spartan-IIE, and Spartan-III; each production type contains many sons. This family offers very wide system gates density ranges with a system performance supported beyond 200MHz.These family devices deliver more gates, I/Os, and features per dollar than other FPGA platforms by combining advanced process technology with a streamlined architecture based on the proven Vertex-E platform. Features includes block RAM, distributed RAM, selectable I/O standards, Delay Locked Loops, Fast predictable interconnect means that successive design

iterations continue to meet timing requirements. [14,16].

Table (2) contains the main characteristics of the two brothers Spartan-II and Spartan-III. [16]

Table (2): - Features of the Spartan FPGA Platform productions

Type	Device	System Gates (Kbit)	Logic Cells	RAM (Kbit)	Delay Locked Loop(DLL)	Max User **I/O**
Spartan-II FPGA Platform productions	XC2S15	15	432	16	4	86
	XC2S30	30	972	24	4	132
	XC2S50	50	1728	32	4	176
	XC2S100	100	2700	0	4	196
	XC2S150	150	3888	48	4	260
	XC2S200	200	5292	56	4	284
Spartan-III FPGA Platform productions	XC3S50	50	1728	72	2	56
	XC3S200	200	4320	216	4	76
	XC3S400	400	8064	288	4	116
	XC3S1000	1000	17280	432	4	175
	XC3S1500	1500	29952	576	4	221
	XC3S2000	2000	46080	720	4	270
	XC3S4000	4000	62208	1728	4	312
	XC3S5000	5000	74880	1872	4	344

The Spartan family is the superior alternative to MPGA where they avoid the initial cost of length development cycle and permit upgrading in the field with no hardware replacement.

3-1: Spartan-IIE FPGA

The Spartan-IIE family contains seven members as summarized in table (3), these FPGA members have regular, flexible, programmable architecture of CLB's, surrounded by a perimeter of programmable input/output blocks (IOB). [15]

Table (3): - Features of the Spartan-IIE FPGA Platform productions

Device	Logic cells	Typical system gate range	CLB (R*C)	Total CLB's	Max available I/O	Distrib. RAM (Bits)	Block RAM (Bits)	DLL
XC2S50E	1728	23K-50K	16*24	384	182	24576	32K	4
XC2S100E	2700	37K-100K	20*30	600	202	38400	40K	4
XC2S150E	3888	52K-150K	24*36	864	256	55296	48K	4
XC2S200E	5292	71K-200K	28*42	1176	289	75264	56K	4
XC2S300E	6912	93K-300K	32*48	1536	329	98304	64K	4
XC2S400E	10800	145K-400K	40*60	2400	410	153600	160K	4
XC2S600E	15552	210K-600K	48*72	3456	514	221184	288K	4

There are four delay lock loops (one at each corner of the die). Two columns of block RAM lie on opposite sides of the die, between the CLB's and the IOB column, the XC2S400E has four column and the XC2S600E have six column of block RAM which are interconnected by a powerful hierarchy of versatile routing channels as shown in fig (6). [18]

Loading the configuration data into internal static memory cells customizes Spartan-IIE. Unlimited programming cycles are possible with this approach. Stored values in these cells are determine the logic function and interconnected implemented in the FPGA. [18]

Configuration data can be read from an external serial PROM (Master Serial Mode) or written into the FPGA in slave serial, slave parallel, or boundary scan mode that's why Xilinx offers multiple types of low-cost configuration solutions include the platform Flash in-System programmable configuration PROMs.

Spartan-IIE is typically used in high volume applications where the versatility of a fast programmable solution adds benefits. Spartan-IIE FPGA is ideal for shortening product development cycle while offering a cost-effective solution for high volume productions. [19]

In addition to the conventional benefits that the Spartan FPGA support, the Spartan-IIE also offers on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable SET and RESET on all flip-flops, fast carry logic and many other features. [20]

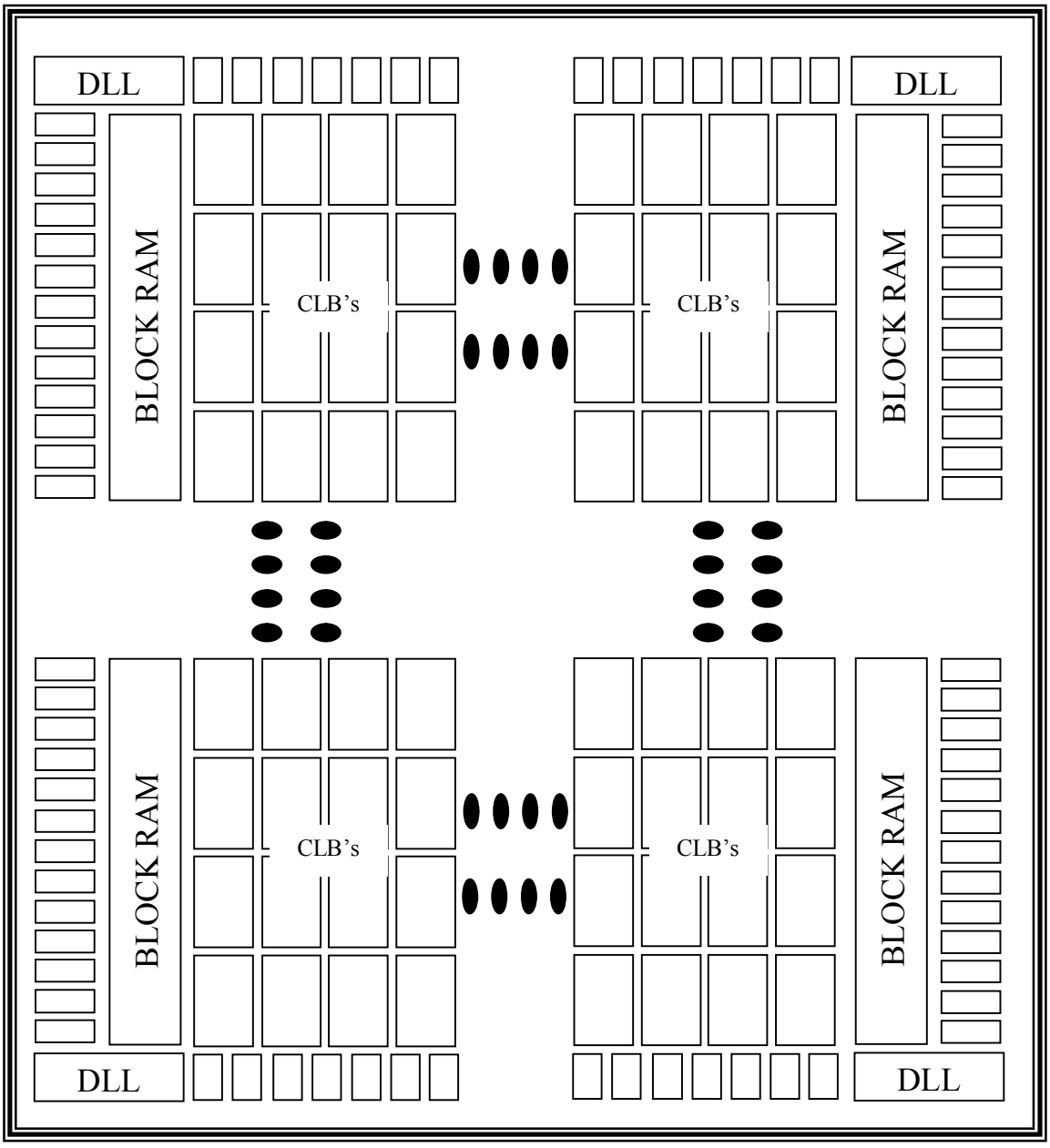

Fig (6): -The basic Spartan-IIE family FPGA block diagram

4:FPGA Simulation of One-Dimensional Wavelet and Wavelet Packet Transform

4.1:The Decomposition Circuits

The decompositions in the Wavelet Transforms are used to extract the important frequency informations from the applied data in the time domain in order to be able to take the necessary decision concerning the data.

If the Multi – Resolution Analysis is applied, then the decomposition formula for all bases functions of Haar or Debauches that is applicable to the one dimensional WPT, is as given in the

matrix and shown in fig (7).

1	1	1	1	1	1	1	1
–1	–1	–1	–1	1	1	1	1
–1	–1	1	1	–1	–1	1	1
1	1	–1	–1	–1	–1	1	1
–1	1	–1	1	–1	1	–1	1
1	–1	1	–1	–1	1	–1	1
1	–1	–1	1	1	–1	–1	1
–1	1	1	–1	1	–1	–1	1

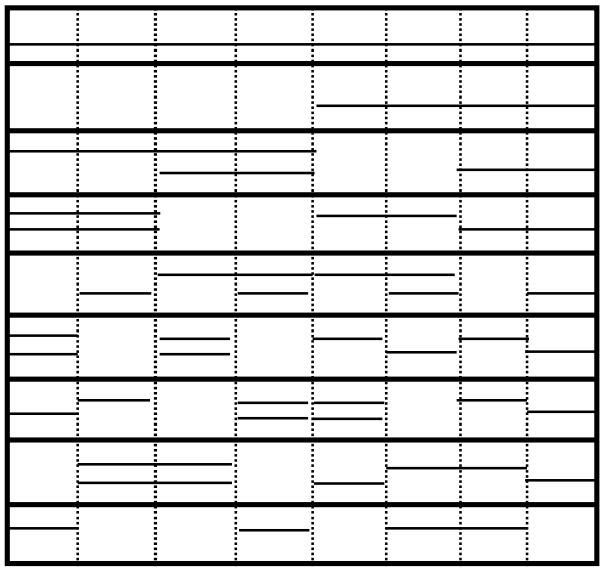

Fig (7): - The WPT decomposition matrix representation of 8 point

For the WT, the Decomposition formula for all bases functions of Haar or Debauches that is applicable if the Multi–Resolution Analysis of one Dimensional signals is used has little differences from that of the WPT. It's given in the matrix and as shown in fig (8).

1	1	1	1	1	1	1	1
–1	–1	–1	–1	1	1	1	1
–1	–1	1	1	0	0	0	0
0	0	0	0	–1	–1	1	1
0	0	0	0	0	0	–1	1
0	0	0	0	–1	1	0	0
0	0	–1	1	0	0	0	0
–1	1	0	0	0	0	0	0

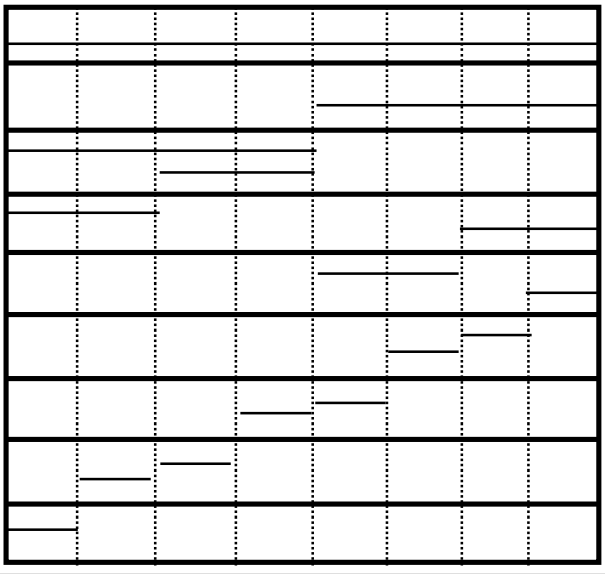

Fig (8): - The WPT decomposition matrix representation of 8 point

The decomposition circuits design shown below depends upon using only the main instruments needed in implementing the circuit. In this kind of design for each (2^N) point we are in need for (2^N) Full Adder/Subtractor to perform the decomposition circuit. In this type the die area is reduced very much with less complexity but it's slow in performance.

Storage devices are needed in this type as shown in fig (9) to store the behavior of the circuit and hence specifying the way of operation. The data in the memory is represented just like the data in the decomposition matrix, but in the logical representation, each (1) will be turned to logic zero to indicate addition and each (-1) will be turned to logic one to indicate subtraction.

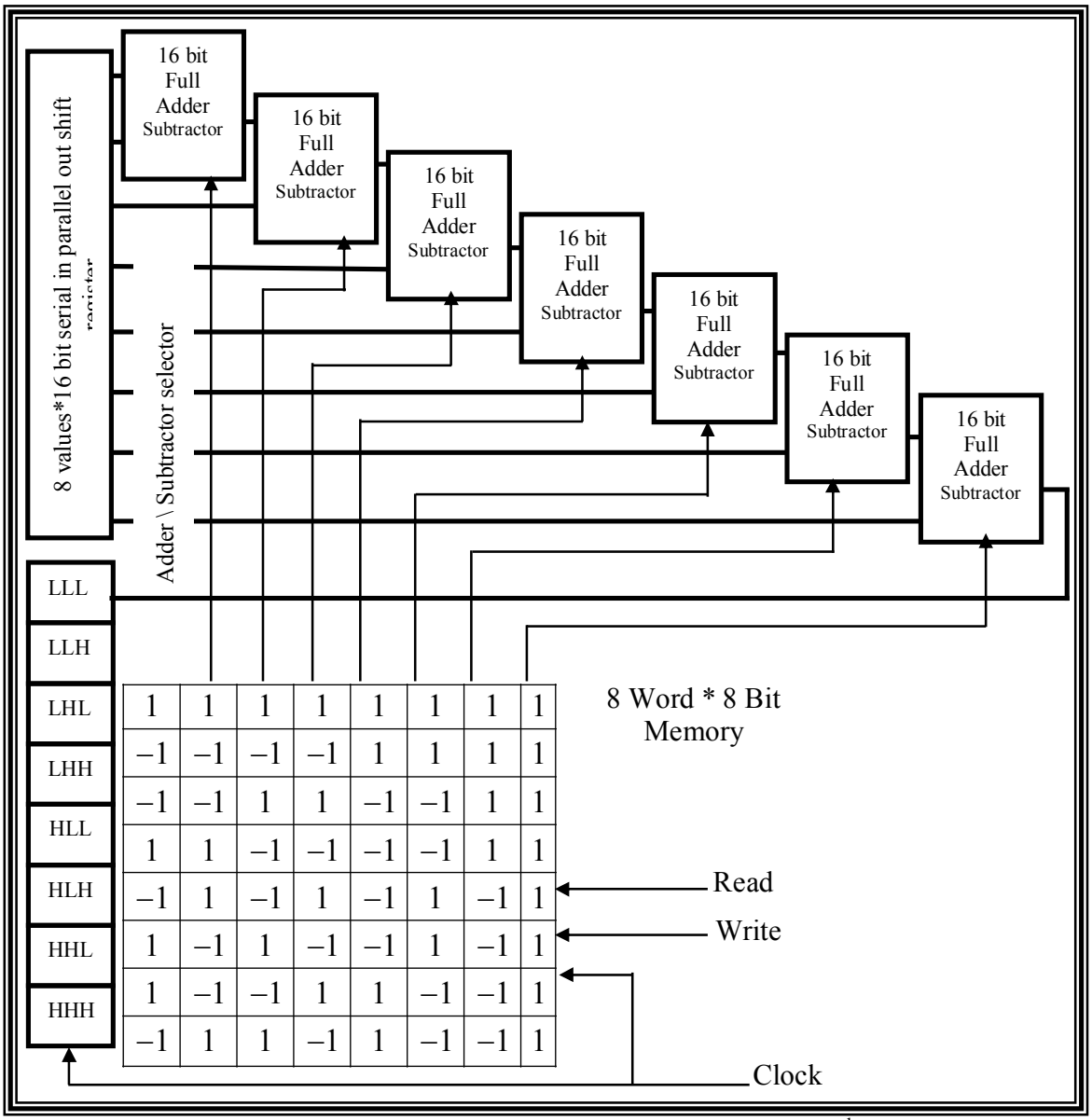

Fig (9): - the decomposition circuit of eight point WPT "3 rd design"

4.2:The Reconstruction Circuits

The general reconstruction formula for all bases functions of Haar or Debauches that is applicable to the WPT, if the Multi – Resolution Analysis of one Dimensional signals is used, is as given in the matrix and as shown in fig (10). The output values of the decomposition are multiplied one by one correspondly by the values in the matrix to give the output values, which are the same as the input values before the decomposition.

1	–1	–1	1	–1	1	1	–1
1	–1	–1	1	1	–1	–1	1
1	–1	1	–1	–1	1	–1	1
1	–1	1	–1	1	–1	1	–1
1	1	–1	–1	–1	–1	1	1
1	1	–1	–1	1	1	–1	–1
1	1	1	1	–1	–1	–1	–1
1	1	1	1	1	1	1	1

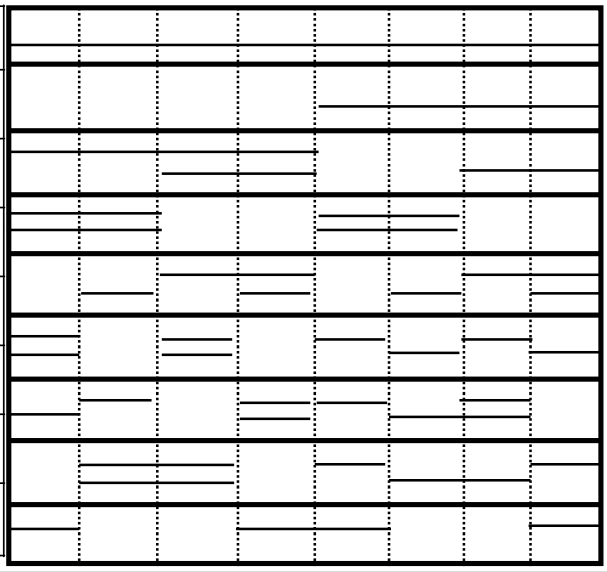

Fig (10): - The WPT reconstruction matrix representation of 8 point

For the WT the reconstruction formula for all bases functions of Haar or Debauches that is applicable if the Multi– Resolution Analysis of one Dimensional signals is used have little differences from that of the WPT. It's given in the matrix and as shown in fig (11).

1	–1	–1	0	–1	0	0	0
1	–1	–1	0	1	0	0	0
1	–1	1	0	0	–1	0	0
1	–1	1	0	0	1	0	0
1	1	0	–1	0	0	–1	0
1	1	0	–1	0	0	1	0
1	1	0	1	0	0	0	–1
1	1	0	1	0	0	0	1

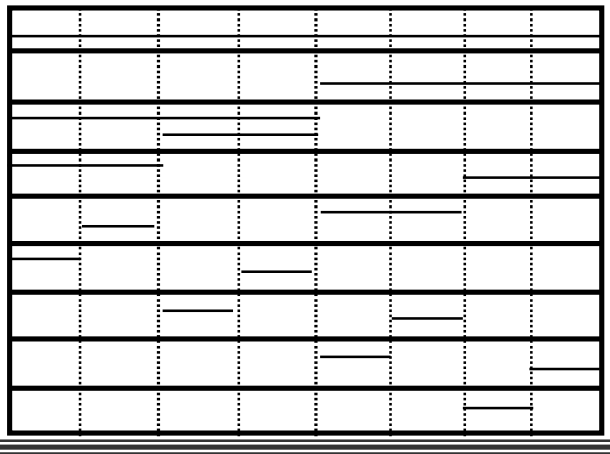

Fig (11): - The WPT reconstruction matrix representation of 8 point

The third design for the reconstruction circuits is depending upon using only the main instruments needed in the design. In this kind of design we are in need for (2^N) Full Adder/Subtractor to perform the reconstruction circuit for (2^N) point. This type reduces the die area to the quarter with less complexity but it's slow in performance.

In this type we are in need for a storage device to store the behavior of the circuit and hence specifying the way of operation. The data in the RAM is represented just like the data in the reconstruction matrix, but in the logical representation, each (1) will be turned to logic zero to indicate addition and each (-1) will be turned to logic one to indicate subtraction. Fig (12) represents the memory design of 8-point reconstruction one-dimensional WPT circuit.

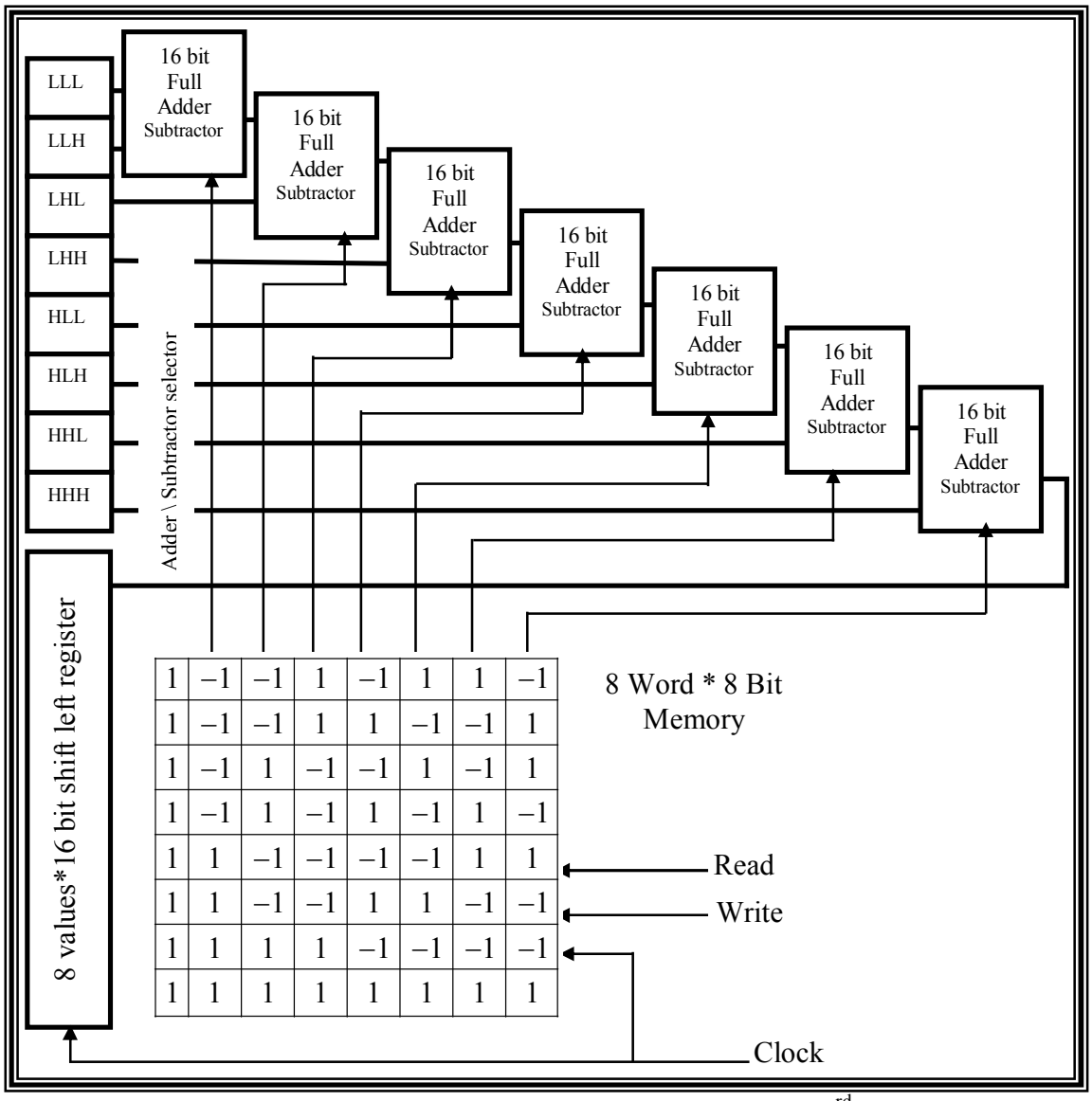

Fig (12): - the reconstruction circuit of eight point WPT "3 rd design"

5:Demonstrated Example

An example of a one-dimension signal of eight values vector will be demonstrated fully with its logical circuit representation and its corresponding results.

In this example the full tree decomposition of the one-dimensional wavelet and wavelet packet transform is evaluated. Taking in the consideration the arrangement of the input and output data.

The data entered vector by vector. The output data obtained as an eight-value vector, arranged as HHH, HHL, HLH, HLL, LHH, LHL, LLH, and LLL each result is represented in sixteen-bit width.

The type of the operation is specified from the value that is to be taken from the memory where the value of –1 represents the subtraction operation. So the value of 1 represents the addition operation.

The value of 0 represents the tri-state operation for the specified value, where the input will be the same as the output since one of the inputs will be represented as zeros. So the addition will be with zeros.

The input vector is: - [7 -5 -2 -3 6 10 5 -7]

The output vector is: - [11 17 -25 -11 -21 5 -5 -27] where they are arranged in the form of high frequency values down to low frequency values [HHH HHL HLH HLL LHH LHL LLH LLL].

Table (4): -Third design Result evaluation of the eight point's decomposition circuit

0000000000000111 (7)	First value	Second value	Third value	Fourth value	Fifth value	Sixth value	Seventh value	Eighth value
1000000000000101 (-5)	0000000000000010 (2)	1000000000000010 (-2)	1000000000000010 (-2)	0000000000000010 (2)	1000000000001100 (-12)	0000000000001100 (12)	0000000000001100 (12)	1000000000001100 (-12)
1000000000000010 (-2)	0000000000000000 (0)	0000000000000000 (0)	1000000000000100 (-4)	0000000000000100 (4)	1000000000001010 (-10)	0000000000001010 (10)	0000000000001110 (14)	1000000000001110 (-14)
1000000000000011 (-3)	1000000000000011 (-3)	0000000000000011 (3)	1000000000000111 (-7)	0000000000000111 (7)	1000000000001101 (-13)	0000000000001101 (13)	0000000000001011 (11)	1000000000001011 (-11)
0000000000000110 (6)	0000000000000011 (3)	0000000000001001 (9)	1000000000001101 (-13)	0000000000000001 (1)	1000000000010011 (-19)	0000000000000111 (7)	0000000000010001 (17)	1000000000000101 (-5)
0000000000001010 (10)	0000000000001101 (13)	0000000000010011 (19)	1000000000010111 (-23)	1000000000001001 (-9)	1000000000001001 (-9)	0000000000010001 (17)	0000000000000111 (7)	1000000000001111 (-15)
0000000000000101 (5)	0000000000010010 (18)	0000000000011000	1000000000010010 (-18)	1000000000000100 (-4)	1000000000001110 (-14)	0000000000001100 (12)	0000000000000010 (2)	1000000000010100 (-20)
1000000000000111 (-7)	0000000000001011 (11)	0000000000010001 (17)	1000000000011001 (-25)	1000000000001011 (-11)	1000000000010101 (-21)	0000000000000101 (5)	1000000000000101 (-5)	1000000000011011 (-27)
Output Results	0000000000001011	0000000000001011	1000000000011001 1111111111100110	1000000000001011 1111111111110100	1000000000010101 1111111111101010	0000000000000101	1000000000000101 1111111111111010	1000000000011011 1111111111100100

Table (5): -Third design Result evaluation of the eight point's reconstruction circuit

0000000000001011	First value	Second value	Third value	Fourth value	Fifth value	Sixth value	Seventh value	Eighth value
0000000000010001	1000000000000100 (-6)	1000000000000100 (-6)	1000000000000100 (-6)	1000000000000100 (-6)	0000000000011100 (28)	0000000000011100 (28)	0000000000011100 (28)	0000000000011100 (28)
1000000000011001 1111111111100110	0000000000010011 (19)	0000000000010011 (19)	1000000000011111 (-31)	1000000000011111 (-31)	0000000000110101 (53)	0000000000110101 (-53)	0000000000000011 (3)	0000000000000011 (3)
1000000000001011 1111111111110100	0000000000001000 (8)	0000000000001000 (8)	1000000000010100 (-20)	1000000000010100 (-20)	0000000001000000 (64)	0000000001000000 (64)	1000000000001000 (-8)	1000000000001000 (-8)
1000000000010101 1111111111101010	0000000000011101 (29)	1000000000001101 (-13)	0000000000000001 (1)	1000000000101001 (-41)	0000000001010101 (85)	0000000000101011 (43)	0000000000001101 (13)	1000000000011101 (-29)
0000000000000101	0000000000010010 (34)	1000000000010010 (-18)	0000000000000110 (6)	1000000000101110 (-46)	0000000001010000 (80)	0000000000110000 (48)	0000000000001000 (8)	1000000000011000 (-24)
1000000000000101 1111111111111010	0000000000011101 (29)	1000000000001101 (-13)	0000000000001011 (11)	1000000000110011 (-51)	0000000001001011 (75)	0000000000110101 (53)	0000000000001101 (13)	1000000000011101 (-29)
1000000000011011 1111111111100100	1000000000111000 (56)	1000000000101000 (-40)	1000000000010000 (-16)	1000000000011000 (-24)	0000000000110000 (48)	0000000001010000 (80)	0000000000101000 (40)	1000000000111000 (-56)
Output Results	0000000000000111 (7)	1000000000000101 (-5)	1000000000000010 (-2)	1000000000000011 (-3)	0000000000000110 (6)	0000000000001010 (10)	0000000000000101 (5)	1000000000000111 (-7)

6:Conclusions

The aim of this paper is to propose a new circuit design for the implementation and evaluation of the one-dimensional wavelet and wavelet packet transform.

In this design the DSP point of view was adapted, where nearly in all other designs the implemented circuits where from the communication point of view, where this type of designs need no wide range filter taps design which reduces the cost.

Because of the kit wide capabilities high speed, high accuracy, low cost, low power consumption, and easy to be handled where achieved.

Other privilege is achieved by the capability to expand the circuit for more than 8 values by duplicating the circuit to evaluate the WT & WPT of 16 , 32 , …value and so on. Since the kit is big enough so higher number of points can be achieved easily, or the reconstruction and the decomposition circuits may be implemented on the same kit in order to reduce the synchronization problems if two kits are use, one for each phase.

7:References

[1] Jan E. Odegard & Ivan W. Selensnick 1993 "Introduction to wavelet and wavelet transform".

[2] F.Argentini, G.Benelli, reprinted from electronic letters, vol 28, pp 513-515, 27th February 1992 "IIR implementation of wavelet decomposition for digital filter analysis ".

[3] A.Aron & E.Rosenberg, IEEE transactions, vol. 64, pp 475-487, April 1986. "Speaker verification using pattern recognition approach ".

[4] N. Rex Dixon & Thomas B. Martin 1989.A volume in the IEEE press selected reprint series "Automatic speech and speaker recognition ".

[5] L.R.Rabiner & R.W. Shafer 1982 "Digital processing of speech signal".

[6] Lawrence Rabiner & Biing – Hwang Juang 1993 "Fundamentals of speech signals".

[7] C.Cheng, Msc thesis, Rise university, department of electrical engineering, May 1996. "Wavelet signal processing of digital audio with application in electro-acoustic music ".

[8] G.R.Doddington processing of electr.76, pp 22-26, May 1976. "Personal identity verification using voice ".

[9] R.J.Mammare, X.Zhang, & Ramachadram, IEEE signal processing magazine, pp 58-71, September 1996 "Robust speaker recognition ".

[10] D.E.Newland, third addition, 1994. "An introduction to random vibration spectral and wavelet Transform ".

[11] A.Chinienti, I. Cibrario, R. Picco, DSP 1997 vol56 p.p 633-636 "Filter evaluation of wavelet Transform".

[12] Dusan Levicky, Emil Matus, Peter Kral, electrical engineering 1996 vol.47 p.p281-286 "Wavelet transform analysis-synthesis-algorithms".

[13] Mohammad N.Hussain, Msc. Thesis, University of Baghdad, department of electrical engineering, October 2000, "Speaker Recognition Based Upon Phonemes Using Wavelet Packet Transform".

[14] V.Herrero, J.Cerda, R.Gadea, M.Martinez, A.Sebestia, Group of design of digital systems, department of electrical engineering, June 2003, "Implementation of 1-D Daubechies Wavelet transform on FPGA".

[15] Piyush Jamkhandi, Amar Mukherjee, Kunal Mukherjee, Robert Franceschini, school of electrical engineering and computer science, July 2003, " Parallel H/W- S/W architecture for computation of discrete wavelet transform using RMF algorithm".

[16] Sarin George Mathen, thesis, University of Kansas ,June 2000, "Wavelet Transform based adaptive image compression on FPGA".

[17] Www.Xilinix.com, July 2003, "Spartan-IIE 1.8 V FPGA family: introduction and ordering informations".

[18] Pak K. Chan, University of California, October 2000, "Digital Design Using Field Programmable Gate Array".

[19] John E. Gilbert , September 2003, "Wavelets : theory and applications on FPGA".

[20] Miguel Figueroa , Chris Diorio, University of Washington ,September 2003,"A 200 MHz , 3mW,16-Tap Mixed – signal FIR Filter".