Design and Implementation of an Interface Unit Communicated by a Laser system Within Wireless Sensor Network

Dr. Hanan A. R. Akkar
Department of Electrical Engineering , University of Technology/Baghdad
Dr. Aied K. AL-Samarrie
Department of Communication Engineering, University of Technology/ Baghdad
Azzad Bader Saeed
Department of Electrical Engineering, University of Technology/ Baghdad
Email:azzad_bader@yahoo.com

Received on:4/2/2016 & Accepted on:18/8/2016

ABSTRACT:

In this paper, an interface unit had been designed and implemented for a wireless sensor network, which used for adapting the sensor output with input of the artificial intelligent system using an electronic control circuit, in conjunction with a Laser communication system.

The proposed unit had used a new technique of analog-to-digital conversion based on a pulse period coding system, which had made the transferring of data and key signals between the interface unit and the intelligent system device more efficient, easer, and faster.

The pulse period coding system had used a new technique of coding , it constructed from two parts, they are: The first is the pulse period coder part, which converts the characters to pulses with specific periods, and the second is the pulse period decoder part, which converts these pulses to binary data.

This system had been simulated and tested using Multisim software package, and one can see that simulation results approach to the theoretical results, so for this reason, this system possesses acceptable design and performance.

Keywords: Artificial Intelligent (AI), Interface Unit, Laser, Sensor, Networks.

INTRODUCTION

The wireless sensor networks (WSNs) are the main widely used application today that applied in many fields such as military, scientific, healthy, …, etc applications. The wireless sensor network is defined as a several or many uniformly deployed sensor nodes which they wirelessly connected to a control station called the HUB[1][2].

Each sensor node has it's own connection channel with the control station. Each sensor node consists of single or multi-sensors depended upon the type and the nature of the application. The role of the sensor node is to detect the effecting element by the sensor that is translated to analog electrical signal, then this signal will be converted to parallel digital signal, then finally, the last signal will be converted to serial digital data that will be then transmitted to the control station (HUB). The duty of the control station is to receive the data incoming from the sensor nodes and the process these data to present a specific decision, so the control satiation must have a central processing unit such as a microprocessor to perform the processing operation on the incoming data[3][4].

Generally, the sensor nodes are supplied by the batteries, so the consumption power is the essential element must be considered in designing of these systems, whereas the consumption power of the sensor nodes must be decreased as much as possible to increase the life of the batteries that leads to reduce the cost of the maintenance of these systems.

https://doi.org/10.30684/etj.34.13A.13
2412-0758/University of Technology-Iraq, Baghdad, Iraq

Various types of sensors are used with the wireless sensor networks, such as, gas, temperature, pressure, etc. Most of these sensors have internal resistance increased or decreased depending on the concentration of the affecting element. The sensor resistor can be connected in series with a fixed resistor and they fed by a power supply, to convert the variation of the sensor resistance to an analog voltage, which is driven to input of the interface unit[5][6][7].

The Wireless Sensor Network constructed from the sensors, interface units, a communication system, and Artificial Intelligent system saved in a central processing unit, as shown in Figure(1) . The duty of the interface unit is to convert the analog signal of the sensor to a parallel binary data, and then convert these parallel data to serial data . The devoir of the communication system is to transfer the data between the interface unit and the artificial intelligent system, while the duty of the intelligent system is to process these data and present a specific decision. This intelligent system must be saved in a microprocessor system or FPGA, or ASIC devices[1].

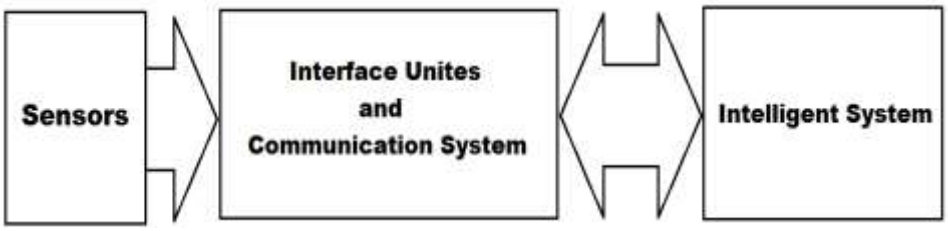


Figure (1): Block diagram of the wireless sensor network[1].

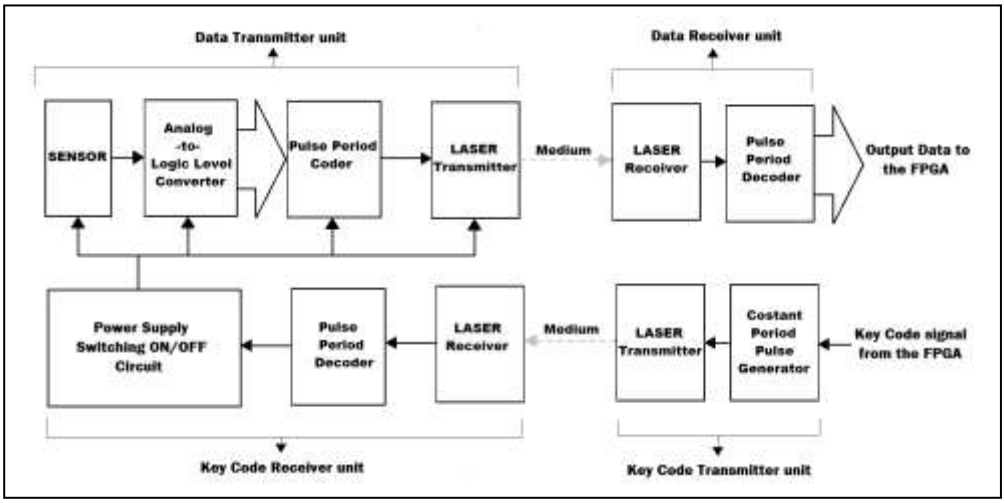
In this paper a new technique of interface unit had been designed , simulated, and implemented, the proposed unit does not use any of the traditional microcontroller, or processor or memory ICs such as in the previous related works, but it had used a laser communication system within a wireless sensor network and a new technique of Analog-to-Digital (A/D) converter circuit, this A/D converter circuit had used a new coding system called *Pulse Period Coding* system for converting the analog signal to digital form.

The proposed A/D converter circuit translate the analog signal that introduced from the sensor to a pulse with a specific period, then this pulse is transferred by the laser communication system to the pulse period decoding circuit at the FPGA side that translate this pulse to a binary data which is fed to the input of the artificial intelligent system saved in that FPGA.

In the traditional interface unit, the data is transferred as a serial pulses(bits), while in the present work the data is transferred as single pulse, therefore, the proposed technique is faster than the traditional interface units.

The Proposed System Concept

The proposed system constructed from two parts, these are: The analog-to-digital converter part, and the key code signal generator part. The analog-to-digital converter has a new technique of conversion, and it consists of two main sections, they are: The analog-to-logic level line converter, and the pulse period coding system, it is also a new technique of coding depends on the variation of the pulse width. The key code signal generator constructed from three essential circuits, they are: The constant period pulse generator, the pulse period decoder, and the controlled power switching circuit. The detailed construction of the interface unit shown in Figure (2). The sensor introduces an analog output voltage according to the concentration of the effecting element, while the analog-to-logic level line converter translates this analog voltage to three possible logic levels, they are; (LOW) level, (MEDIUM) level, and (HIGH) level, whereas, this circuit has three output lines.



Figure(2): Block diagram of internal construction of the interface unit.

The pulse period coder generates a pulse with a specific period, depending on the activation of one of the logic level lines, for example, if the sensor activates the (LOW) logic level line, a pulse with a period of (10 msec) will generate, and if the sensor activates the (MEDIUM) logic level line, a pulse with a period of (20 msec) will generate, and so on, then this pulse is modulated and transmitted through a medium by the LASER transmission system. All previous circuits construct a unit called the data transmitter unit.

The Laser receiver circuit receives and detects this Laser pulse from the medium, and then translates it to an electrical pulse. The pulse period decoder circuit converts this pulse to a two bits binary data, driven to input of the intelligent system, which may be saved in an FPGA device. One of three binary data can be presented at the output of the pulse period decoder, depends on which logic level line had been activated, for example, the pulse period decoder will present a binary data (01), if the (LOW) logic level line is activated, and will present a binary data (10), if the (MEDIUM) logic level line is activated, and will present a binary data (11), if the (HIGH) logic level line is activated.

The key code signal generator part, controlled by a signal introduced from the intelligent system that saved in the processing device, whereas, the constant period pulse generator of this part will produce pulses with constant widths. These pulses are generated if the controlled input of this generator is activated and they represent the switching key code to switch ON or OFF the power supply feeding of the data transmitter unit, then these pulses are modulated and transmitted through a medium by another Laser transmission system.

Another Laser receiving system receives these key code Laser pulses and translates them to an electrical pulses, which driven to input of the pulse period decoder, and they are converted to a binary data, whereas, these data are used as a binary code to activate the switching control circuit to switch ON the supply feeding of the data transmitter unit.

The proposed system design and calculations

The proposed system designed and implemented using, Analog comparators, Timers, and TTL logic ICs such as, Gates, Buffers, Counters, Monostables, Latches. It constructed from four main circuits, they are: Data transmitter, data receiver, key transmitter, and key receiver circuits. The data transmitter circuit consists of the analog-to-logic level line converter, pulse period coder, and Laser modulator and transmitter circuit, which had been shown in Figure (3). The

sensor connected in series with the resistor R1, they are fed by +5Volt power supply, and the bypass capacitor C1 shunted with the resistor R1 to produce a low pass filter.

The data transmitter circuit had been used for converting the analog output signal of the sensor to a logic level line signal, it constructed from dual analog comparators and a single window comparator. The input of this circuit had been connected to the sensor, while its output had been driven to the input of the pulse period coder circuit.

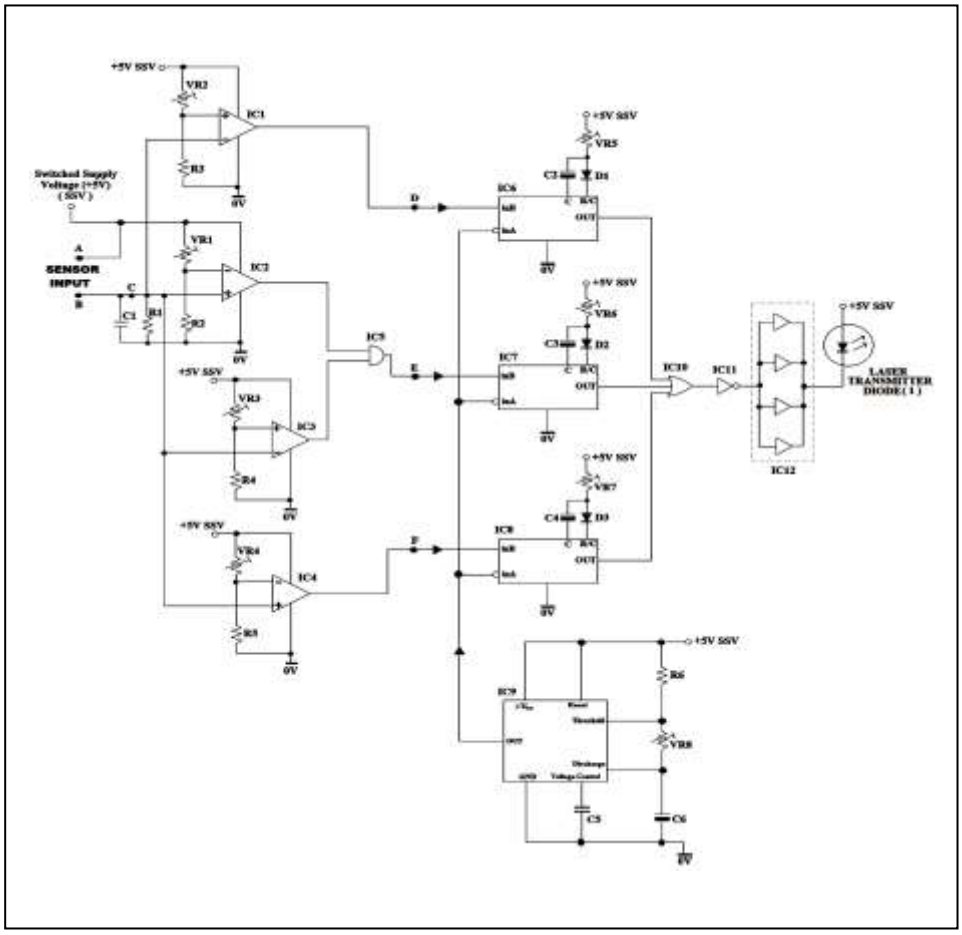


Figure (3): Circuit diagram of the data transmitter unit.

The first analog comparator is IC1, which has threshold input voltage equal to V_{th1}. When the sensor output voltage is less than V_{th1}, the output of this comparator is at HIGH state, otherwise it is LOW state as shown in Figure (3), whereas, the output of this comparator represents LOW level line (point D). The second analog comparator is IC4, which has threshold input voltage equal to $V_{th2,}$ when the sensor output voltage of this comparator exceeds V_{th2}, its output goes to HIGH state, otherwise it is LOW state, which it represents the HIGH level line (point F).

The window comparator constructed from two analog comparators IC2 and IC3, with the AND gate IC5, where the output of the two comparators is connected to the inputs of the AND gate. When the sensor output voltage is at range ($V_{th1} \leq V_{in} \leq V_{th2}$), the output of this window comparator is at HIGH state, otherwise it is LOW state, whereas, this output represents the MEDIUM level line (point E), therefore, there are three output level lines at the output of the Analog-to-Logic level line converter, they are LOW level, MEDIUM level, and HIGH level.

The threshold input voltage of IC1, IC2, IC3, and IC4 are set by the variable resistors VR2, VR1, VR3, and VR4 respectively.

The pulse period coder circuit constructed from three Monostables (IC6, IC7, IC8), the OR gate IC10, and the Timer IC9. The output pulse width of the Monostables is calculated by the following expression[9][10]:

$$T = 0.28\,(R\,.\,C) \qquad \text{..... (1)}$$

Where *R,C* are the resistor and capacitor of each Monostable.

The three output lines of the Analog-to-Logic level lines (LOW level, MEDIUM level, HIGH level) are sequentially connected to the inputs of the three Monostables (IC6,IC7, IC8). The variable resistors (VR5,VR6,VR7) are adjusted for producing pulses with widths 10ms for IC6, 20ms for IC7, and 30ms for IC8, whereas, at each time, a pulse with a specific width (10ms or 20ms or 30ms) is generated according to which output line of the Analog-to-Logic level line converter is activated. The Timer IC9 used for repetitive generation of clock pulses for the pulse period coder circuit, the clock output frequency of this Timer calculated from the following expression[11][12]:

$$f = \frac{1}{0.693(C6)\left(R6+2(VR8)\right)} \qquad \text{.....(2)}$$

Where, R6 is a constant resistor and C6 is a constant capacitor, and VR8 is used to adjust the clock frequency to 1 Hz.

The Buffer driver IC12 modulates the generated pulses of the pulse period coder, and then transmitted by the Laser transmitter diode (1)[8].

The second part of the interface unit is the data receiver circuit, it constructed from Laser pulse detector and pulse period decoder circuits, the role of this part is detecting and converting the transmitted pulses to binary data, which driven to input of the intelligent system, as shown in Figure (4).

The Laser pulse detector constructed from Laser receiver diode (1) and an analog comparator IC13, which used for converting the incoming Laser pulses to electrical pulses with same pulse widths, the sensitivity of the detector is adjusted by the variable resistor VR9.

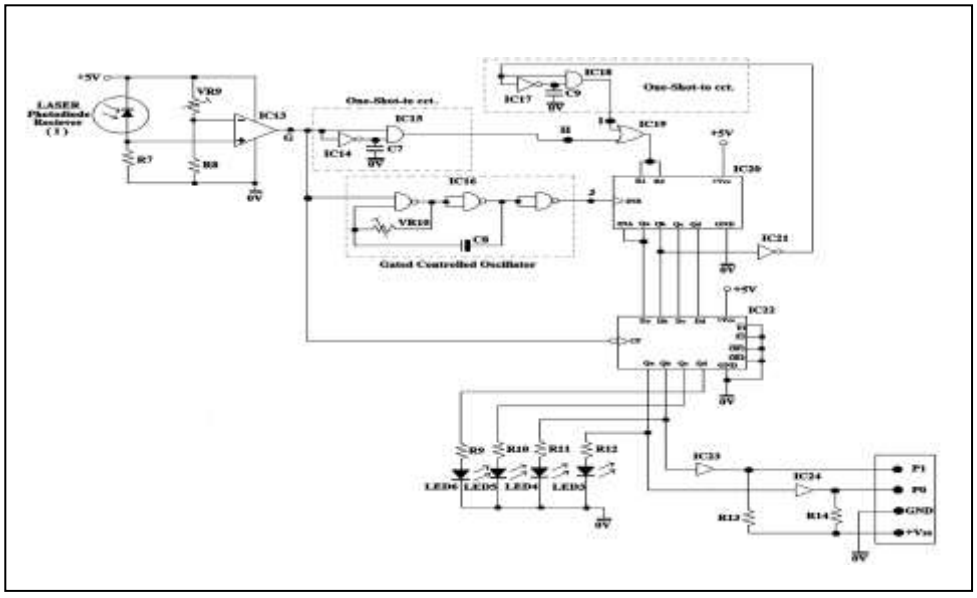


Figure (4): Circuit diagram of the data receiver unit

The pulse period decoder consists of five stages, they are: Two Monostable Multivibrators, controlled oscillator, binary counter, Latch, adapter circuit. This decoder used for converting the electrical pulse introduced from the Laser pulse detector to a binary data, the controlled oscillator used to produce a clock signal with frequency of (100Hz), whenever the input controlling signal (point G) is at HIGH state. The Monostable circuit constructed from IC14 and IC15, the role of this circuit is producing of a narrow pulse (with period of 10nsec) ,used to Reset the binary counter IC20 at the positive edge of the incoming electrical pulse from the Laser pulse detector. The second Monostable circuit constructed from IC17 and IC18, the duty of this circuit is producing a narrow pulse (with a width of 10nsec) used to Reset the binary counter at each end of full counting. The binary counter IC20 used for counting the incoming pulses from output of the controlled oscillator. The Latch IC22 used for holding the binary data of the binary counter output at each negative edge of the electrical pulse comes from the Laser pulse detector circuit. The adapter circuit (IC23 and IC24) is a buffer driver circuit used for adapting the TTL logic output of the Latch circuit to input of the processing device (such as FPGA or ASIC) that saves the intelligent system. At the positive edge of the electrical pulse that comes from the Laser pulse detector, the Monostable (IC14 and IC15) produces a narrow pulse to Reset the binary counter IC20, at the same time the controlled oscillator IC16 is activated to produce a clock signal with frequency of (100Hz), then the binary counter counts these pulses.

At the negative edge of electrical pulse of the Laser pulse detector, the controlled oscillator finishes its oscillation, and the binary counter stops its counting, while the Latch holds the binary output data of the binary counter. Whenever the LOW level line is activated, a pulse with period (10msec) will be transceived, then a binary data (01) will be presented at the output of the Latch, and when MEDIUM level line is activated, a pulse with period of (20msec) will be transceived, then a binary data (10) will be presented, and finally, when HIGH level line is activated, a pulse with period of (30msec) will be transceived, and then a binary data (11) will be presented.

The key transmitter unit constructed from: a Monostable, Timer, Buffer, Laser transmitter diode, as shown in Figure(5). This unit used for generating constant period pulses, and then transmitting them as a Laser pulses through the medium. These pulses are considered as a key signal used for switching the supply feeding of the data transmitter unit.

The Monostable IC26 used for generating the constant period pulses, with a width (30msec), which it triggered by the Timer IC25, this timer used for repetitive producing of the constant period pulses. The widths of these pulses are adjusted by the variable resistor VR12 according to expression (1),

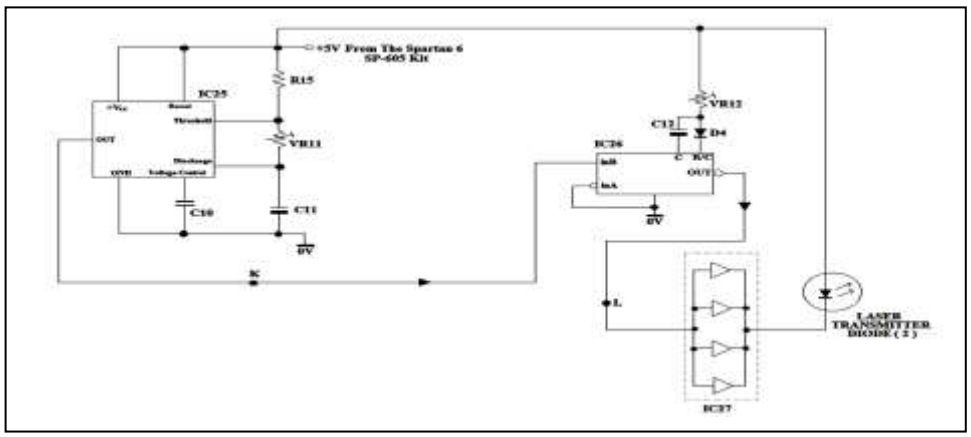
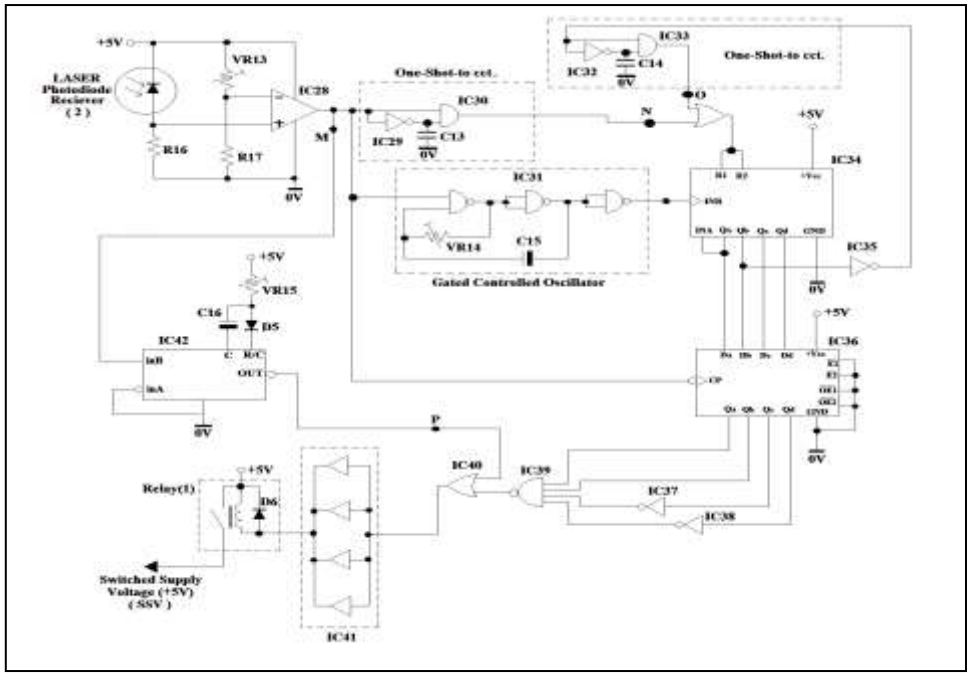


Figure (5): Circuit diagram of the key transmitter unit.



Figure(6): Circuit diagram of the key receiver unit.

While the repetition frequency is adjusted by the variable resistor VR11 according to expression (2). Theses constant period pulses are introduced to the Buffer driver IC27, which acts as a modulator to modulate these pulses with the Laser carrier signal, then these Laser pulses are transmitted by the Laser transmitter diode (2).

The key receiver unit is similar to the data receiver unit, which shown in Figure(6), it consists of: Laser pulse detector, and a pulse period decoder, but it differs by consisting of another decoder and a Buffer driver that drives Relay switch. This unit used for converting the incoming Laser pulse to a binary data which decoded to drive and activate a +5Volt Relay switch.

The circuit analysis of the laser pulse detector and the pulse period decoder is the same as used for the data receiver unit, but the output of the Latch is driven to the decoder circuit constructed from IC37, IC38, and IC39. When the key receiver unit receives a Laser pulse with width (30msec), a binary data (11) will appear at the output of the Latch, which then decoded to activate the Buffer driver IC41 to switch ON the Relay, which connect the +5Volt power supply to the feeding input of the data receiver unit.

The Monostable IC42 used for continuously activating the Buffer driver; whenever sequence Laser pulses is introduced to the detector of the key receiver unit, i.e. this Monostable inactivates the Buffer driver when no more Laser pulses are introduced to detector input of the key receiver unit.

Finally, the date transmitter and key receiver units are mounted at the sensor unit, while the data receiver and key transmitter units are mounted with the processing device that saves the intelligent system.

Results and Discussion

The four main units of the proposed system are simulated using Multisim software package, whereas, the state diagrams had been shown by the logic analyzer. The simulation state

diagram of the data transmitter unit shown in Figure (7), one can see from this figure that Monostable IC7 had been activated, while Monostables IC6 and IC8 inactivated, i.e. the sensor output voltage in the range ($V_{th1} \leq V_{so} \leq V_{th2}$) which activates the window comparator (IC2,IC3, and IC5). Term1 and term3 signals represent output of comparators IC1 and IC4 respectively, while term2 signal represents the output of window comparator, term 4 represents output signal of the Timer IC9, which had a frequency (1Hz).

Term4, term5, and term6 represent output signals of the Monostables IC6, IC7, and IC8 sequentially, and one can see that Monostable IC7 had been activated to produce a pulse with period (20msec), which triggered at each negative edge of the clock output of Timer IC9, while Monostables IC6 and IC8 inactivated. Term8 represents output signal of the OR gate IC10 which driven to the Laser transmitter diode(1).

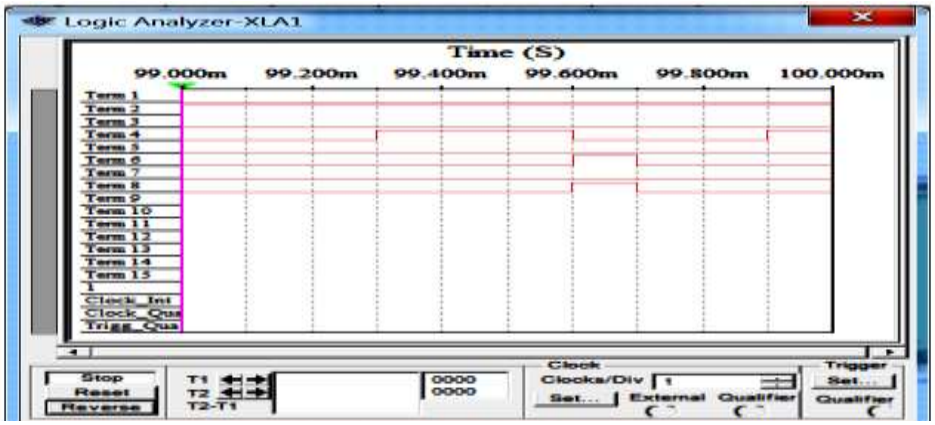


Figure (7): Simulation state diagram of the data transmitter unit.

The simulation state diagram of the data receiver unit shown in Figure(8), Term1 represents output pulse of the comparator IC13, which had a duration (20msec), term2 represents output clock of the controlled oscillator IC16, which oscillates for a period of two clock cycles, term3 represents the Reset narrow pulse of the Monostable (IC14 and IC15), which triggered at each positive edge of output pulse of the comparator IC13, term4 and term5 represent Q_A and Q_B output lines of the binary counter IC20, term6 and term7 represent Q_A and Q_B output lines of the Latch IC22, which triggered at each negative edge of output pulse of the comparator IC13.

The simulation state diagram of the key transmitter unit shown in Figure(9), term1 represents output clock of the Timer IC25, which had a frequency (1Hz) while term2 represents output pulse of the Monostable IC26, which triggered at each positive edge of the clock output of the Timer IC25, it had duration of (30msec).

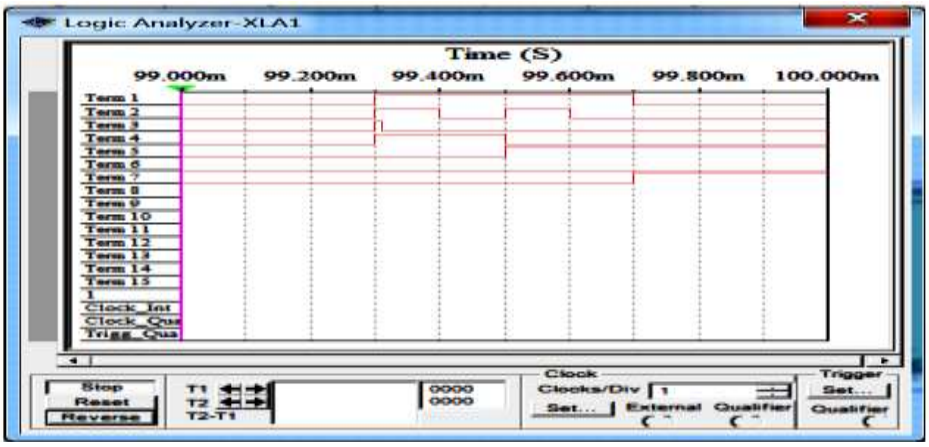


Figure (8): Simulation state diagram of the data receiver unit.

Th

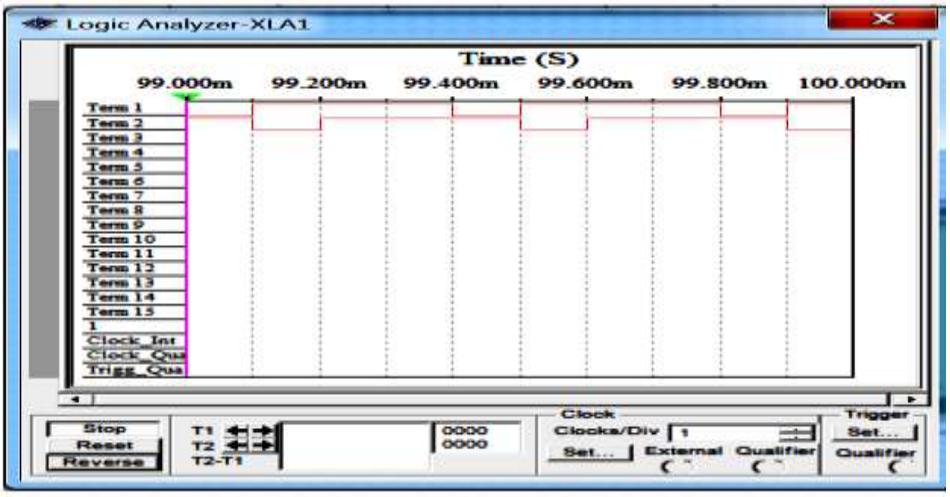


Figure (9): Simulation state diagram of the key transmitter unit.

Term1 represents output pulse of the comparator IC28, which had a duration (30msec), term2 represents output clock of the controlled oscillator IC31, which oscillates for a period of three clock cycles, term3 represents the Reset narrow pulse of the Monostable (IC29 and IC30), which triggered at each positive edge of output pulse of the comparator IC28, term4 and term5 represent Q_A and Q_B output lines of the binary counter IC34, term6 and term7 represent Q_A and Q_B output lines of the Latch IC36, which triggered at each negative edge of output pulse of the comparator IC28. Term8 represents the output pulse of the Monostable IC42, which triggered at each positive edge of output pulse of the comparator IC28, finally term9 represents the state of output signal of the OR gate IC40, which driven to the Buffer driver IC41 to control the Relay switch (1). Whenever the output state of the OR gate is LOW, the Relay switch(1) is activated to ON state, which connects the +5 Volt power supply terminal to the feeding input of the data transmitter unit.

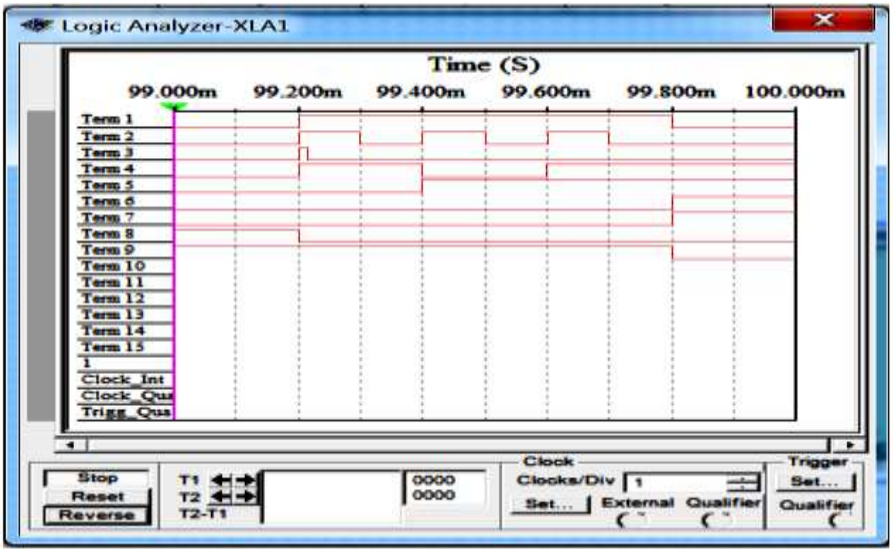


Figure (10): Simulation state diagram of the key receiver unit.

Finally, the proposed system had been implemented on four printed circuit boards as shown in Figure (11), which connected to two Carbon Monoxide gas sensors and FPGA type Xilinx Spartan6 SP 605.

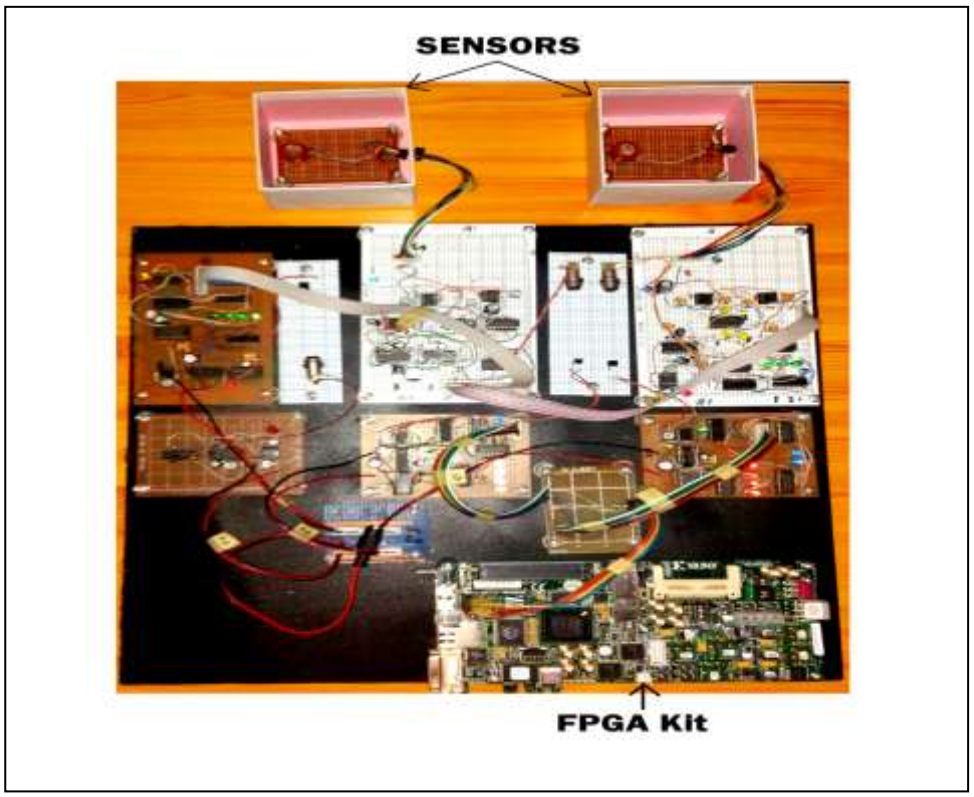


Figure (11): The practical proposed system connected to two sensors an FPGA kit

CONCLUSIONS

The internal resistance of the sensor will be reduced by exposing the sensor to the effecting element, this process leads to increase the output level of the analog-to-logic level line converter, and increase the binary output data of the Latch IC.

The analog signal of the sensor circuit had been converted to three levels: LOW, MEDIUM, and HIGH levels, while output of the pulse period decoder had three binary data, these are: (01), (10), and (11). These levels and binary data can be increased more and more to increase the accuracy of the output results.

TTL logic integrated circuits had been used in the logic circuit of the interface unit, and one can use high speed CMOS integrated circuits to increase the speed of the logic circuits, and decrease the consumed power, which leads to increase the battery life that feeds the sensor unit.

An electromechanical Relay switch had been used for connecting the +5Volt power supply to the feeding input of the data transmitter unit, and one can use a driver transistor instead of this Relay for increasing the switching speed and reducing the board size of the key receiver unit.

REFERENCES

[1]. Geoff V. M., Yen K. T.," Wireless Sensor Networks: Application-Centric Design", Intech,2010.
[2]. Elena G., Lewis G., Michael A., Geoffrey C.," Wireless Sensor Networks",Springer Science+Business Media, Lcc., 2010.
[3]. Pedro M., Thiemo V., Luca M., "Real World Wireless Sensor Networks", Springer-Verlog Berlin Hiedelberg, 2010.
[4]. Suraiya T.," Wireless Sensor Networks", Intech Co., 2011.
[5]. Anathram S., Qing Z., Lang T.," Wireless Sensor Networks", John Wiley&Sons Ltd, 2007.
[6]. Waltenegus D., Christian P., " Fundamentals Of Wireless Sensor Networks: Theory And Practice", John Wiley&Sons Ltd., 2010.
[7]. Mahmood F. M., Duaa S. T.," Hardware Implementation Of Wireless Sensor Network Using Arduino And Zigbee Protocol", Eng.&Tech. Journal, Vol.34, Part(A), No. 5, 2016.
[8]. Hayder A. S., Labeab O. A.," Design And Implementation Of Free Space Simplex Video-Laser Communication System ", Eng.&Tech. Journal, Vol. 27, No. 12, 2009.
[9]. Nihal K., " Electronic Circuit Design", Taylor&Francs Group, 2008.
[10]. Muhammad H. R.," Microelectronic Circuits Analysis And Design" Cengage Learning, Inc., 2011.
[11]. Tony R. K.,"Lessons In Electric Circuits: Volume Iv-Digital", Tony R. Kuphaldt, 2015.
[12]. Anil K. M., " Digital Elecronics", John Wiley&Sons, Ltd., 2007.