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Effects of Enhancement P^+ Layer on IGBT Operation

Abstract- *IGBT (Insulated-gate bipolar transistor), is used widely in high voltage applications, it is very important to realize the doping profile in order to understand the design and the electrical performances of such devices. The performance depends on the layer, doping, and a carrier distribution among each layer. A specific selected layer can be added with precise properties for enhancing the device and increase the low current operate requirement. In this paper, an IGBT device is an enhanced and better performance achieved by the addition of a heavily positive doped intermediate layer. The collector current is decreased from 0.05 mA to 0.03 mA at 600 V. Decreasing the current results in higher efficient device by decreasing the amount of heat produced by the device.*

Keywords- *heavily doped, symmetric blocking, enhancement*

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1. Introduction

The IGBT (Insulated gate bipolar transistor) is representing the true MOS–bipolar integration, in the sense of hybrid combination the physics of the operation structure of the MOSFET and PNP transistor. The MOSFET provides the base current for the transistor, and the transistor modulated the conductivity of the drift of the MOSFET [1]. Pulsed power applications and power electronics requires devices that withstand high current and high voltage. IGBTs have properties that make them eligible to be used in such applications [2]. IGBTs has been used in varying applications depending on the desired usage specifications as well as switching power supplies, power inverters, uninterruptible power supplies, motor drive controlling, and automatic ignition switch circuit [3]. I-V curve is traced in a T-IGBT blocking condition in a presented model. The base of the transistor is used to regulate the ration between the electrons and the holes in the depletion region. The ratio is calculated for each current density level of accurate charge control mode [4].Later, the laser annealing process has been used for producing ultra-low conduction loss in nonpunch-through NPT-IGBT. The annealing process enabled achieving of thin wafer based IGBT [5].The lifetime, failure mechanisms, and pressback of the IGBT is studied and compared. The results of analytical models are used to expect the lifetime of wire bonded IGBTs. The results showed that using press back mechanism prevents the dominant failure mechanism as well as provides better power cycle capability [6]. In this paper, a MOSFET has been designed and simulated. The structure is analyzed and the electrical characteristics are evaluated. An enhancement layer is added to the device, which altered the electronic characteristics of the device leading to better forward bias characteristics and better thermal properties.

2. Theory

The IGBT structure has four alternating semiconductor layers (N–P–N–P) as shown in Figure 1. However, the structure is made by including a deep diffusion and short circuit the base (P+) to the emitter (N+) using emitter electrode. The symmetric blocking refer to as the NPT-IGBT structure because of in the lightly doped of the drift the electric field does not stretch out through the width [7]. The MOSFET is supplied transistor base current, the basic equivalent circuit of IGBT shown in Figure 2, the base of the transistor is lightly-doped with virtual contact. This contact is placed at end of the base near to the collector. The IGBT's current density range has high level injection and low gain condition that competes this transistor [8]. This is the most important of the IGBT equivalent circuit. The transistor terminals are with C', B', and E'. The IGBT collector C is the transistor emitter E'. The channel current I_{CH} flow in the base of the transistor, and threshold voltage V_T

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lower than gate voltage V_G. For the current $I_{C'} = \beta_{pnp} * I_{CH}$, and the relation $\alpha = \beta/(\beta + 1)$[9].

$$I_{C'} = \frac{\alpha_{pnp}}{1-\alpha_{pnp}} I_{CH} \quad (1)$$

$$I_{C'} = I_{C'} + I_{CH} = \frac{\alpha_{pnp}}{1-\alpha_{pnp}} I_{CH} + I_{CH}$$

$$I_{C'} = \frac{1}{1-\alpha_{pnp}} I_{CH} \quad (2)$$

$$I_{Csat} = \frac{1}{1-\alpha_{pnp}} . \frac{k}{2} (V_G - V_T)^2 \quad (3)$$

When κ is the channel conductivity, and α_{pnp} must be adjusted very exactly and not too high [10].

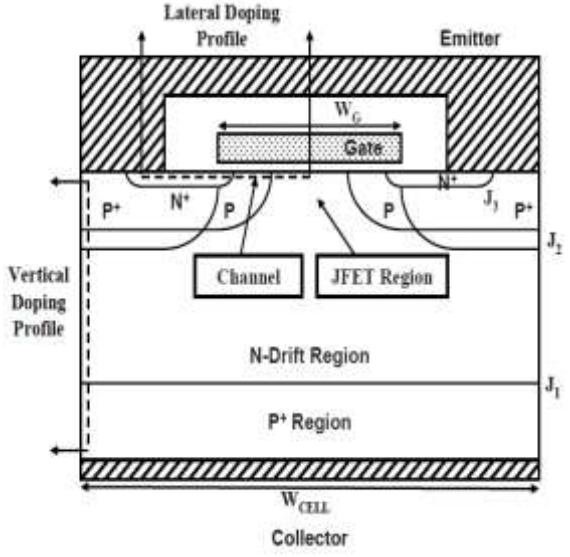

Figure 1: IGBT structure

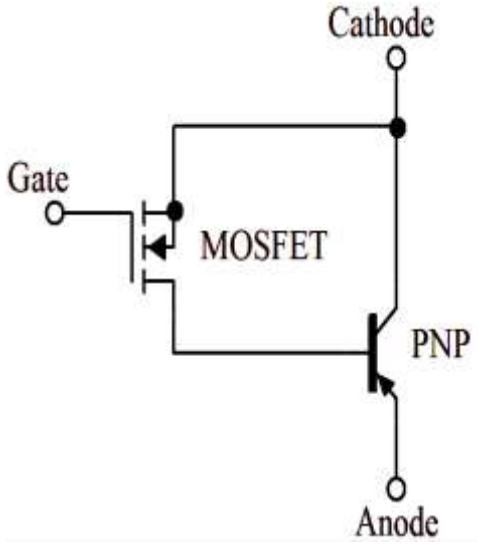

Figure 2: IGBT equivalent circuit

3. Simulation

Two devices were designed and simulated using SILVACO software. The first device shown in Figure 3-a consists of four doped semiconductor layers representing an IGBT device. It consists of an emitter layer, gate metal, and collector metal. The structure of the device starts with a heavily doped (P+) layer attached to the collector with 5 µm thickness. The second layer is 100 µm n-doped layer with 30 µm width. The top of this layer is doped to build p doped layer with 5 µm thickness and heavily doped N+ region forming the emitter and gate. The emitter is fused on N+ and P layer. The proposed design is shown in Figure 3-b. A heavily doped p+ layer is added to enhance the emitter and enhance the performance of the IGBT.

The doping profile of the unenhanced IGBT is shown in Figure 4. The collector is doped with Boron, the emitter Phosphor, and the gate Boron. The thickness of the intermediate Silicon Oxide layer is n-doped with 14.2 $x10^{13}/cm^3$ for providing the required electrons that contribute in the conduction process.

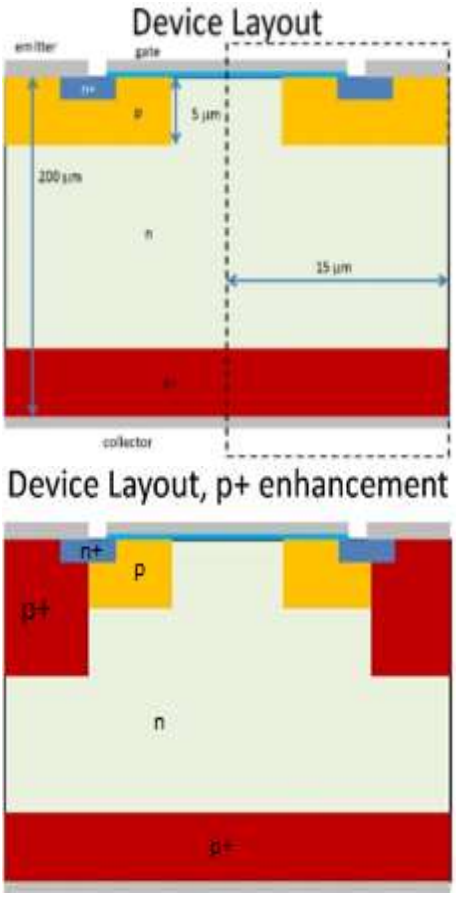

Figure 3: (a) IGBT device before enhancement
(b) Enhancement IGBT

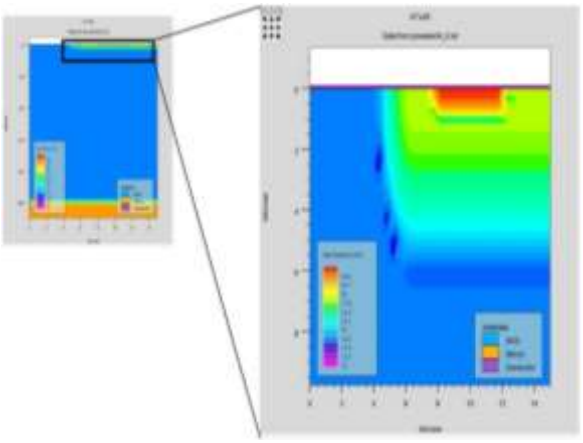

Figure 4: Doping before enhancement

Figure 5 shows the doping profile for the enhanced IGBT. The additional p+ layer can be recognized by the heavily doped p+ profile. The other doping concentrations remain unaltered. Figure 6 illustrates the cross section view of the doping concentration. The unenhanced IGBT starts with $20x10^{13}/cm^3$, and ends with p-doped $19x10^{13}$ $/cm^3$. Figure 7 shows the cross section doping profile of the enhanced IGBT. It can be seen the peak concentration is $1x10^{19}$ $/cm^3$ for the enhanced P+ layer.

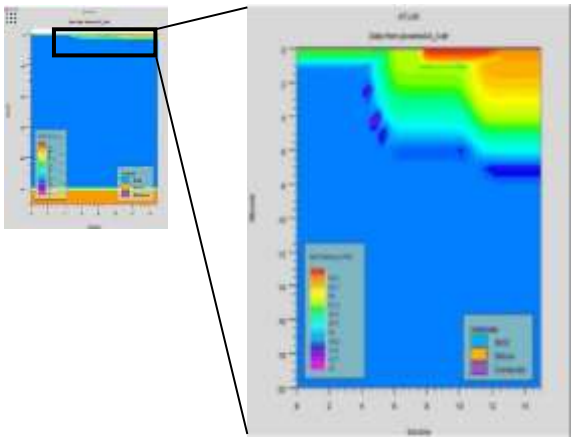

Figure 5: P+ Enhanced device

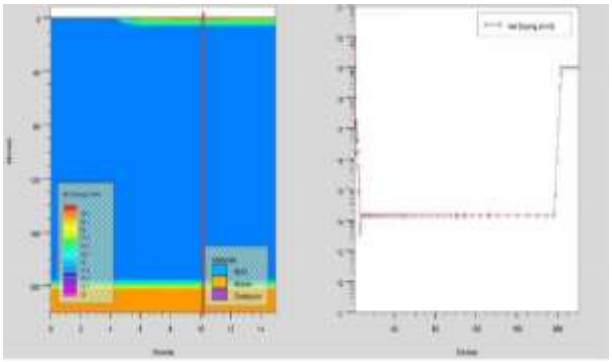

Figure 6-a: Vertical doping concentration before enhancement

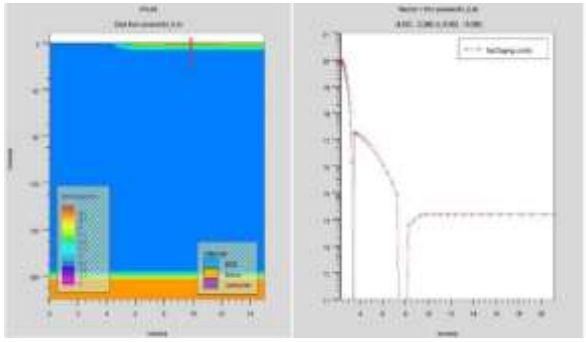

Figure 6-b: zoom of Figure 6-a

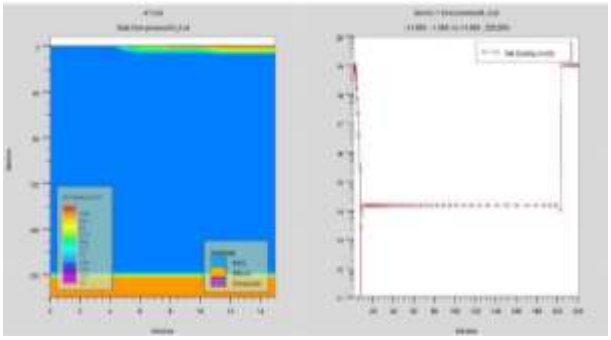

Figure 7-a: vertical doping profile after enhancement

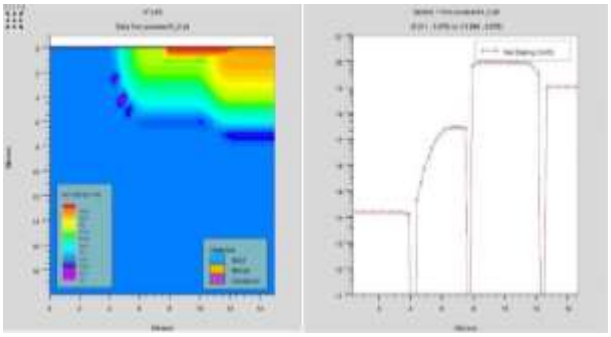

Figure 7-b: zoom of Figure 7-a

4. Results

The designed device is simulated for obtaining forward bias I-V curve. Different gate voltage is applied and the collector voltage is calculated. Figure 8 illustrates the I-V curve for the proposed IGBT device without the enhancement layer. The gate voltage is increased from 5 - 10.5 volt with the collector voltage is varied from 0 - 1000 volt and the collector current is measured. Figure 9 presents the I-V curve for the enhanced IGBT device. The device simulated using the same gate trigger voltages as previous device. However, the enhanced device requires less current to sustain in ON state. This gives the enhanced IGBT extra electrical and physical properties and makes it suitable for extremely high voltage applications. Figure 10 shows the difference between the I-V curves of the two devices when the gate voltage is 10.5 volt.

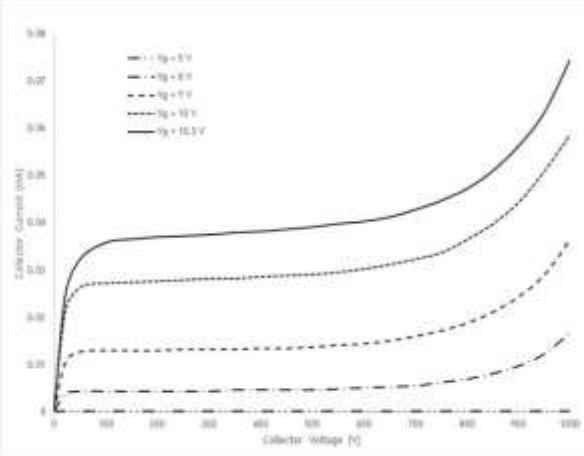

Figure 8: Forward bias before enhancement

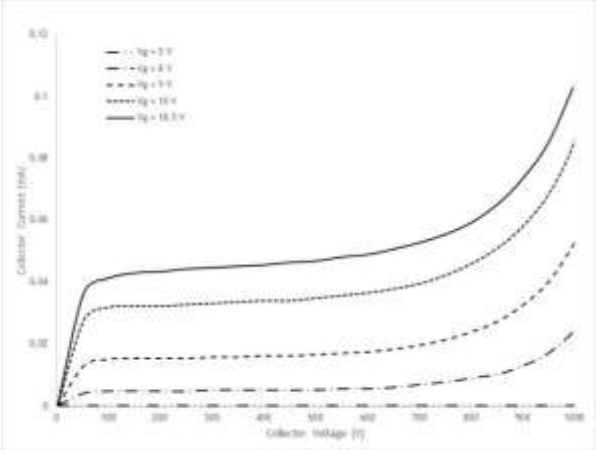

Figure 9: V-I characteristic after P+ enhancement

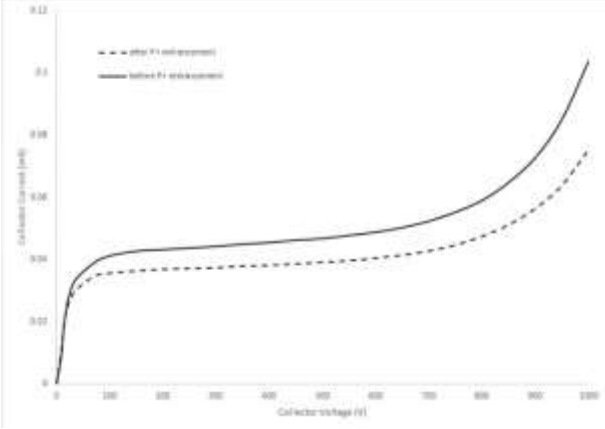

Figure 10: P+ effect on the V-I curve

5. Conclusion

In this paper, two IGBT devices are designed and simulated successfully. The first device is simulated without adding enhancement layer. The second device is studied by adding an enhanced heavily doped P^+ layer. The I-V curves of both devices are compared. The results showed that enhancement layer provides an additional channel for carrier. Thus, decreasing the current that passes through the device when the gate voltage is applied. The collector current is decreased from 0.05mA to 0.03 mA at 600 V. Decreasing the current results in higher efficient device by decreasing the amount of heat produced by the device. Moreover, the device drains less current at the same gate voltage that decreases the required power to operate the device. The proposed IGBT is more suitable for high power heat effective devices. This high power IGBT device is suitable for usage in high power pulsed power supplies such as high powered laser power supply.

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