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Design A Combinational Circuit Consists of 10 Logic Gates Using Quartos

Taha Rashid[1,2], Muhammad Naziiruddin bin Hamzah[2], Mohammed RASHEED[3, 4*], Ahmed Shawki Jaber[5], Mohammed Abdelhadi Sarhan[6], Mustafa Nuhad Al-Darraji[7], Tarek Saidani[8], Ahmed Rashid[1]

[1]College of Arts, Al-Iraqia University, Baghdad, Iraq
[2]Computer and Microelectronic Systems, Faculty of Engineering, Universiti Teknologi Malaysia (UTM), Skudai 81310, Johor Bahru, Malaysia
[3]Applied Sciences Department, University of Technology, Baghdad, Iraq
[4]MOLTECH Anjou, Universite d'Angers/UMR CNRS 6200, 2, Bd Lavoisier, 49045 Angers, France
[5]Mathematics Science Department, College of Science, Mustansiriyah University, Baghdad, Iraq
[6]Mathematics Science Department, College of Science, Mustansiriyah University, Baghdad, Iraq
[7]Department of Biology, College of Science, University Of Al-Anbar, Anbar, Iraq
[8]Department of Physics, Akli Mohaned Oulhadj University of Bouira, Bouira, 10000, Algeria

*Corresponding Author: Mohammed RASHEED

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ABSTRACT: Fault models are designed to forecast the expected behaviors (reaction) from the IC when faults are present, and this is what allows automated test pattern generation (ATPG) software to generate the test patterns. In order to identify these faults at every node in the circuit, the ATPG tool first consults the fault models to establish the patterns that will be necessary for doing so. In this article, ten logic gates are developed using the Quartos program to test for faults in a circuit, and the output waveform was simulated to determine the outcomes of the fault-free output using a variety of test patterns. This fault-free output is compared to the output when a fault injection occurs. It may then be determined if the various test patterns can be utilized to discover the fault in the simulation. The findings demonstrated that the fault can be discovered flawlessly.

Keywords: Combinational logic circuits, fault free circuit, faulty circuit, logic gates, boolean expression, truth table

1. INTRODUCTION

Combinational Logic Circuits are a special kind of non-memory digital logic circuits in which the output at any one time is determined only by the combination of the inputs [1]. In contrast to Sequential Logic Circuits, whose results rely on both the current inputs and the state of the circuit's previous results [2], providing them with Memory. At any one moment, In a combinational logic circuit, the outputs are exclusively determined by the logical function of the current input state [3], logic "0" or logic "1". Consequently, Due to the absence of feedback in combinational logic circuits, the outputs are instantly affected by any changes made to the input signals [4]. The result of a Combinational Logic Circuit is therefore always the product of its inputs. Consequently, In contrast to sequential circuits, combinational circuits can't store any information. Since combinational logic circuits lack memory, timing, and feedback loops by design, the final output will change if the state of any of its inputs transitions from 0 to 1 or 1 to 0. As shown in Figure 1.

*Corresponding author: rasheed.mohammed40@yahoo.com

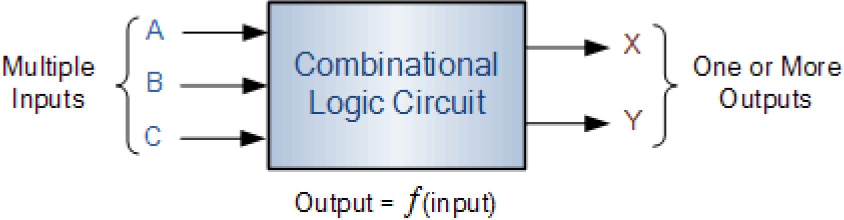

FIGURE 1. - Combinational logic circuit

NAND, NOR, and NOT gates are the building blocks of combinational logic circuits, which are then "combined" or joined to produce more sophisticated switching circuits [5]. They are the backbone of every combinational logic circuit. A decoder is a combinational circuit because it takes in binary information and outputs a series of lines, each of which represents that code in decimal form. [6]. NAND and NOR gates are referred to as "universal gates" because they may be used to form any combinational circuit, from the simplest to the most complicated [7]. There are typically three ways that the purpose of a combinational logic circuit is stated [8-20]:

A- Boolean Algebra: This algebraic statement illustrates how the logic circuit produces a logic "1" in response to True or False input variables.

B- Truth Table: An explanation of how a logic gate works may be found in its "truth table", which provides a compact rundown of all the possible "true" states the gate will produce in response to any given set of input variables.

C- Logic Diagram: This is a graphical representation of a logic circuit, showing the connections and cabling between the many logic gates, each of which is represented by its own visual symbol.

The representations of these three logic circuits are presented in Figure 2.

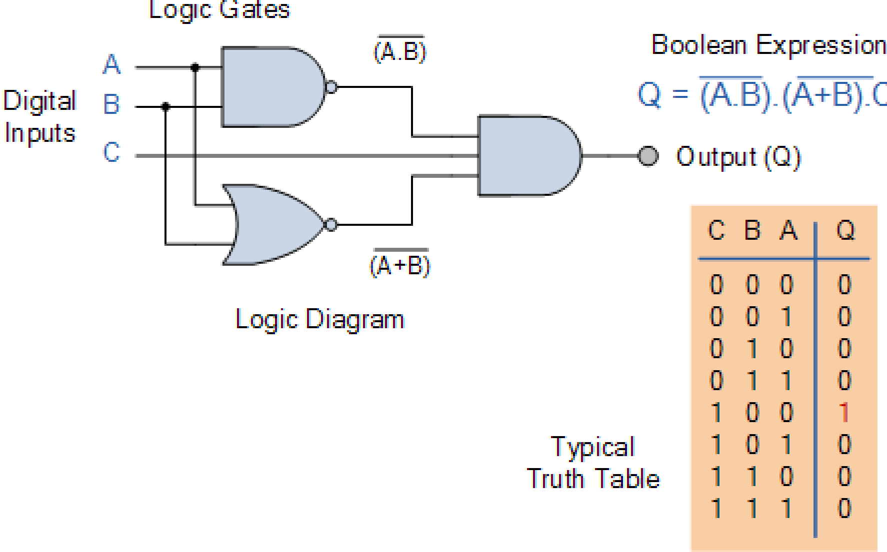

FIGURE 2. - The function of a combinational logic circuit

Because they are built from discrete logic gates, combinational logic circuits are sometimes known as "decision making circuits." Combinational logic is the use of several logic gates to perform a logical function on multiple input signals and produce a single output signal. Standard combinational circuits are made up of numerous logic gates to accomplish a single task, such as multiplexers, de-multiplexers, encoders, decoders, full and half adders, etc. In this paper, 10 logic gates are connected to form a combinational circuit and tested with a different test patterns and the resulting waveforms are compared.

2. METHOD

The Automatic Test Pattern Generation (ATPG) procedure consists of locating a collection of test patterns to be applied to the inputs of the tested circuit in order to discover potentially all faults (under a given fault model). In the Electronics industry, errors in products are defined in a variety of ways, which may lead to misunderstanding over the words defect, error, and fault. Faults are faults in electronic systems that may lead to breakdowns. A fault is a very minor imperfection, such as a frozen memory bit, a stuck-at fault, an uninitialized software variable, an alpha particle collision, or cosmic ray ionization. Error may be seen as the next level of a fault that may result in unanticipated system

behavior. System mistakes might include the erroneous value of a state variable, the entry into an endless loop, or the incorrect outcome of a computation. In general, an error is the corruption of data from its right value to another one. Failure may be seen as the next degree of error, which may result in a system component not functioning as planned.

In this paper, 10 logic gates are designed as shown in Figure 3. The output waveform as shown in Figure 4 was simulated to see the results of the fault free output with various test pattern. This fault free output will be use to compare with the output when an injection of fault happens. By doing this, it can be seen whether the different test patterns can be used to detect the fault or not for the simulation.

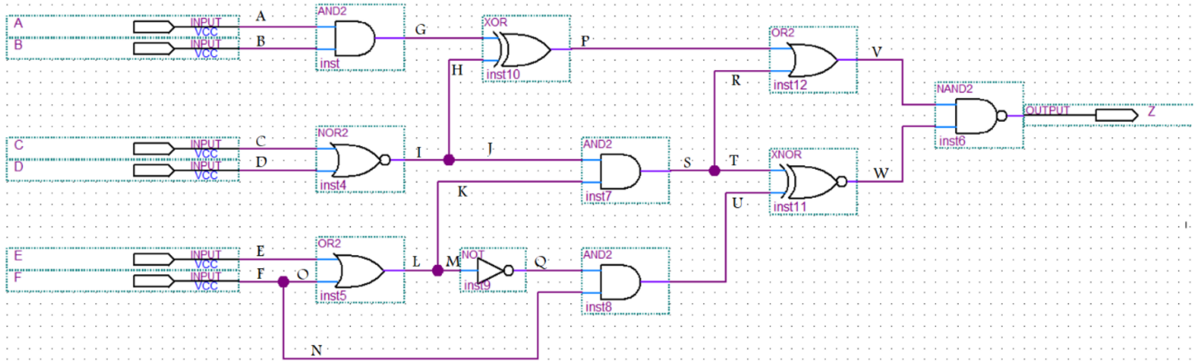

FIGURE 3. - Combinational Circuit Design for Fault Free

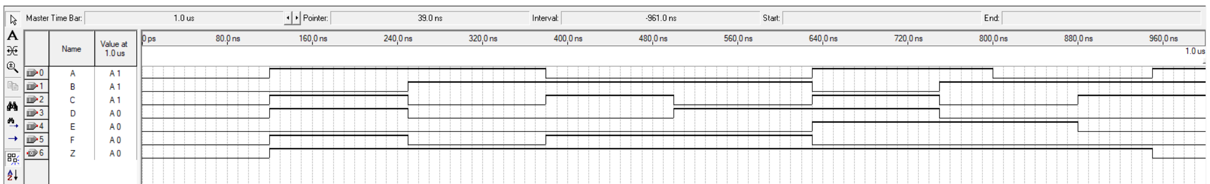

FIGURE 4. - Input and Output Waveform for Fault Free Circuit

3. RESULT AND DISCUSSION

3.1 Combinational Logic Circuit for fault P Stuck at 1

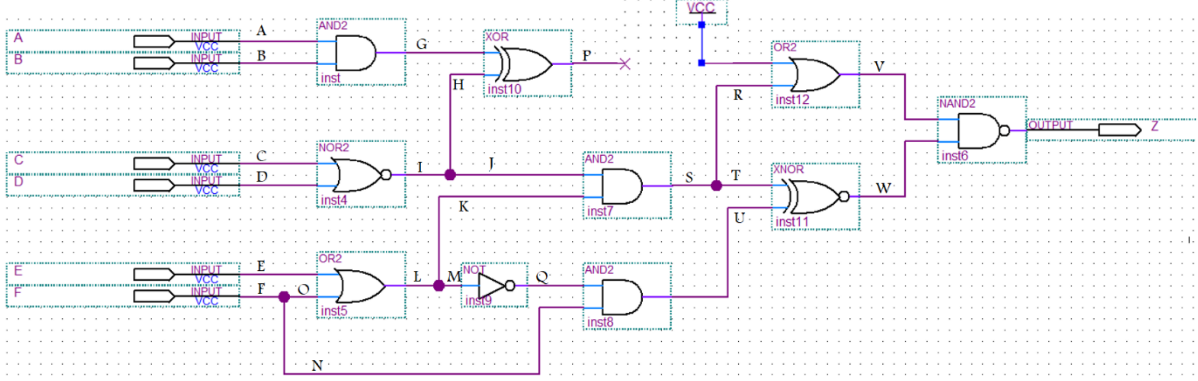

FIGURE 5. - Combinational Circuit Design for P Stuck at 1

Output Waveform P Stuck at 1

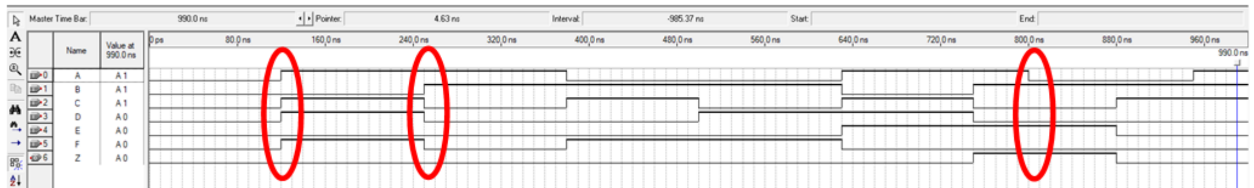

FIGURE 6. - Input and Output Waveform for P Stuck at 1

The circuit was tested with P stuck at 1. This is done by putting a VCC for the input of P to simulate an input high which is stuck at 1 for the P. For example, when the test pattern is set 101101 the output Z will be 0 for P stuck at 1. While for the fault free circuit when the same test pattern 101101 is set the output will be 1 thus the fault can be detected. A second test pattern was use to see the consistency of the simulation. A test pattern 110000 was use and then we get the output of for P stuck at 0. For the fault free circuit when the test pattern 110000 we get the output z is 1 thus the fault can be detected. One of the test patterns where the fault cannot be detected is when the test pattern is set to 010010 because both the output for fault free and P stuck at 1 circuit, we get the value 1 thus the fault cannot be detected since their outputs give different value than the fault free output.

3.2 Combinational Logic Circuit for fault J Stuck at 0

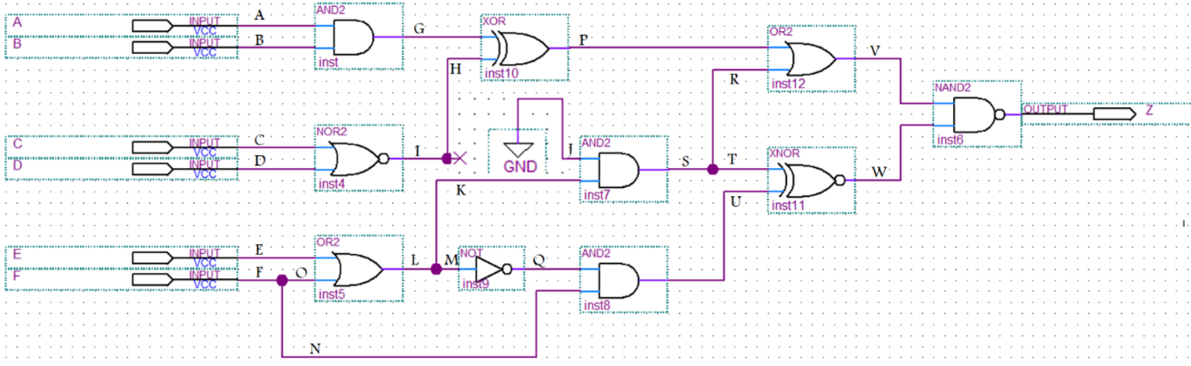

FIGURE 7. - Combinational Circuit Design for J Stuck at 0

Output Waveform J Stuck At 0

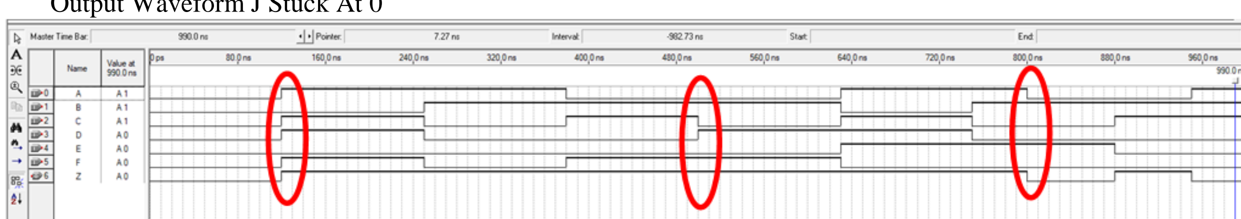

FIGURE 8. - Input and Output Waveform for J Stuck at 0

The circuit was tested with J stuck at 0. This is done by putting a GND for the input of J to simulate an input low which is stuck at 0 for the J. For example, when the test pattern is set 101101 the output will be 1 for J stuck at 0. While the for the fault free circuit when the same test pattern 101101 is set the output is also 1 thus the fault cannot be detected. Another test pattern was use to verify the simulation. A test pattern 010010 was use and then we get the output of 0 for J stuck at 0. For the fault free circuit when the test pattern 010010 we get the output z is 1 thus the fault can be detected. Lastly another test pattern was use which is 010101 and we get the output 1, for fault free circuit we use the same test pattern and we get the output of 1 thus the fault cannot be detected since their outputs give different value than the fault free output.

3.3 Combinational Logic Circuit for fault W Stuck at 1

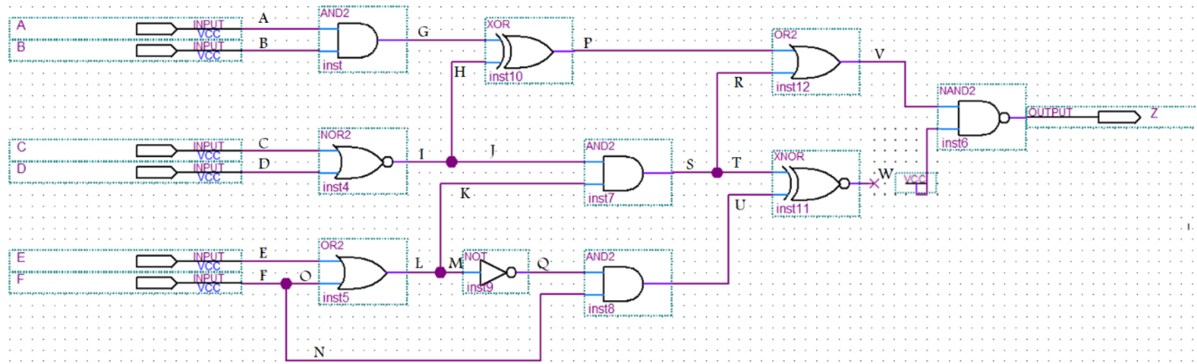

FIGURE 9. - Combinational Circuit Design for W Stuck at 1

Output Waveform W Stuck At 1

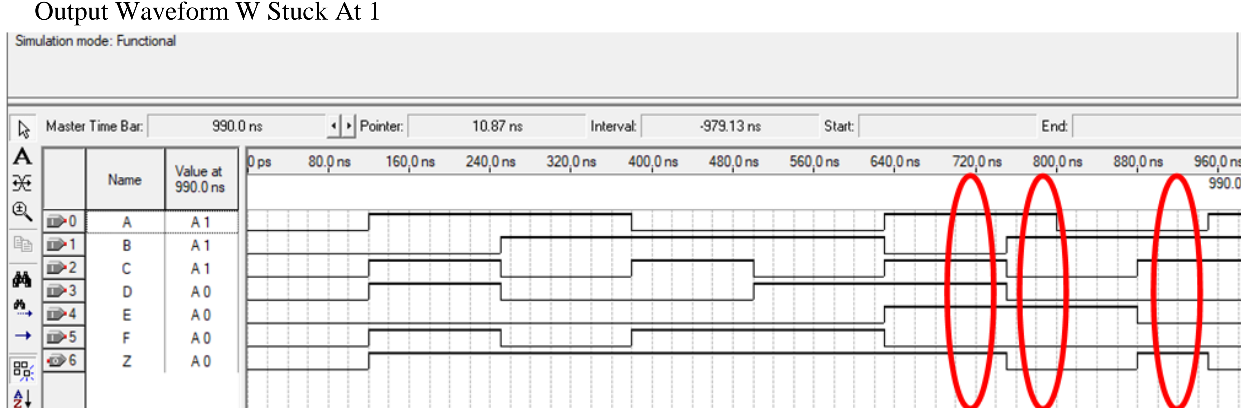

FIGURE 10. - Input and Output Waveform for W Stuck at 1

As we can see from the waveform, by having one of the inputs to the W stuck at fault (SA1), this fault can be detected by using many test patterns. For example, when we apply input test pattern (ABCDEF) = (110010) the output of the faulty free circuit (Z) should be equal to 1, while we are getting 0. which means this fault have been already detected by using that test pattern. Similarly with test patterns (ABCDEF) = (010010). However, when we apply test pattern (ABCDEF) = (111000), the fault will not be detected since the value of the output (Z) are the same for both faulty free and faulty circuit which is 0.

3.4 Combinational Logic Circuit for fault G Stuck at 0

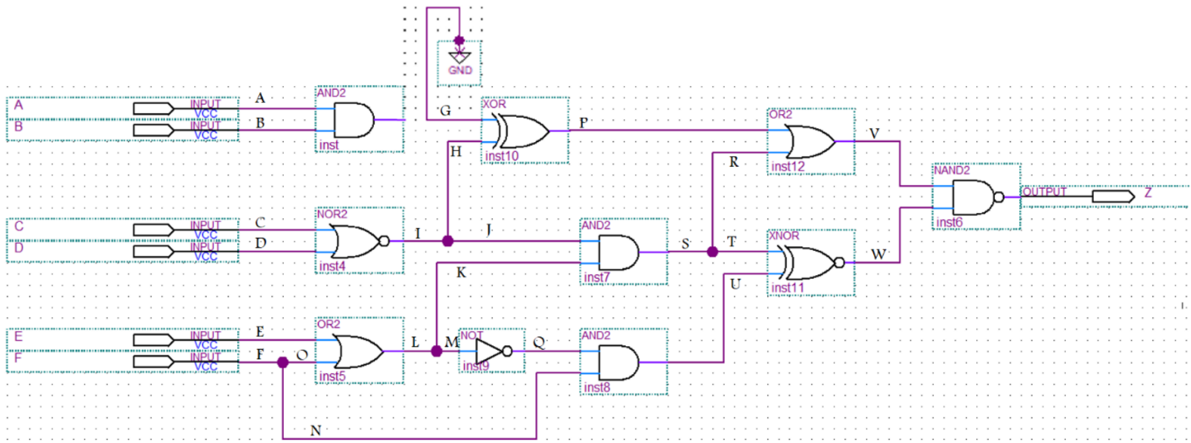

FIGURE 11. - Combinational Circuit Design for G Stuck at 0

Output Waveform G Stuck At 0

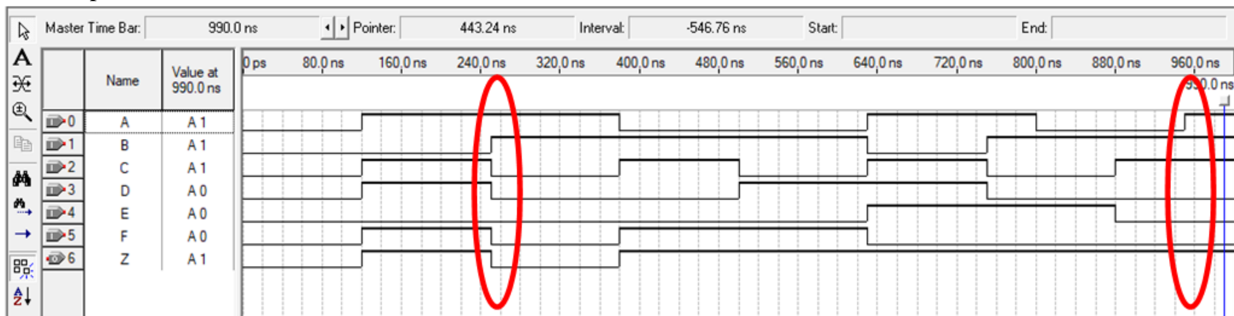

FIGURE 12. - Input and Output Waveform for G Stuck at 0

In this case, we are having G stuck at 0. This fault can be detected by using test pattern (ABCDEF) = (110000). By comparing the fault free circuit waveform with the faulty circuit waveform, we can see that the output (Z) should be = 1, while we are getting (Z) = 0 in the waveform of faulty circuit. In addition, when the test pattern was (ABCDEF) = (111000), Z=0 for faulty free circuit, but we got Z=1 for faulty circuit. Therefore, this fault can be detected using test patterns (ABCDEF) = {110000, 111000}.

3.5 Combinational Logic Circuit for fault N Stuck at 0

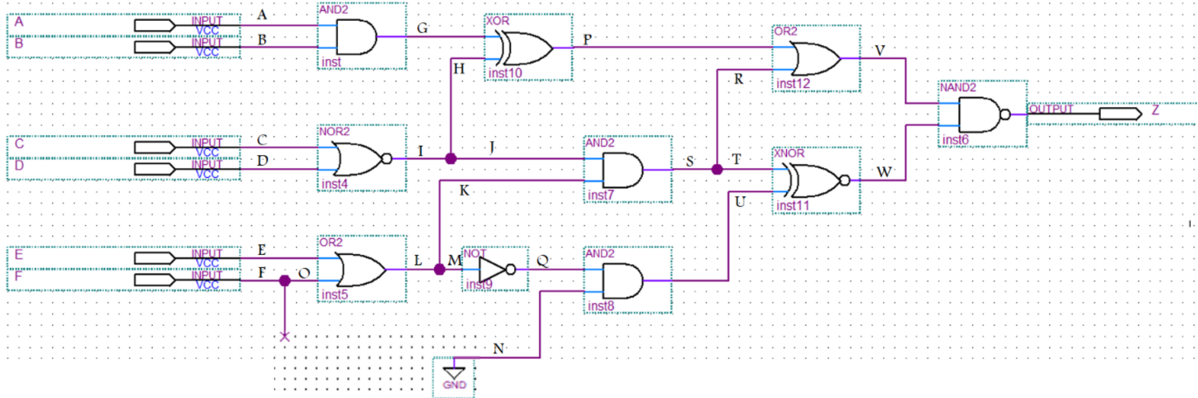

FIGURE 13. - Combinational Circuit Design for N Stuck at 0

Output Waveform N Stuck at 0

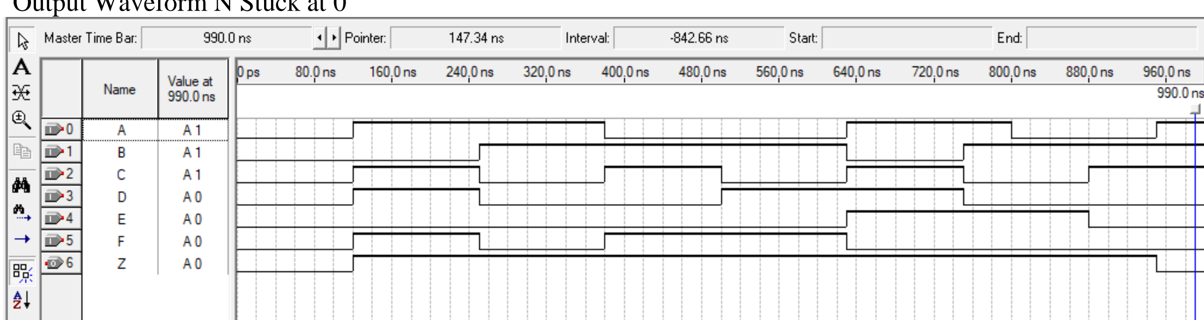

FIGURE 14. - Input and Output Waveform for N Stuck at 0

Here we are injecting a fault which is N stuck at 0. After generating the waveform and by comparing the faulty free circuit with the faulty circuit waveforms, we can notice that this fault cannot be detected by our selected test pattern, since the values of the output (Z) are all identical for all input patterns.

Table 1. - Full test pattern used to detect the fault

Test Pattern	J Stuck at 0	P Stuck at 1	W Stuck at 1	G Stuck at 1	N Stuck at 1	Fault Free
101101	1	0	1	1	1	1
110000	1	0	1	0	1	1
011001	1	0	1	1	1	1
010101	1	0	1	1	1	1
101110	1	0	1	1	1	1
110010	1	1	0	1	1	1
010010	0	1	0	1	1	1
011000	1	0	1	1	1	1

Lastly the full test patterns were compiled into a table so the results can be observed more clearly which test pattern can be used to detect the stuck at faults.

4. CONCLUSION

Combinational Logic Circuits are comprised of inputs, two or more fundamental logic gates, and outputs. The logic gates are combined so that the output state is totally determined by the input states. The functioning of combinational logic circuits is immediate, since they have no memory, time, or feedback loops. An operation assigned logically by a Boolean expression or truth table is carried out by a combinational logic circuit. To allow automated test pattern generation (ATPG) software to generate test patterns, fault models predicting the anticipated behavior

(response) of the IC when flaws are present must be developed. The ATPG tool then utilizes the fault models to establish the patterns necessary to identify these faults at all locations of the circuit. In this paper, 10 logic gates are designed using Quartos software to test the fault in the circuit and the output waveform was simulated to see the results of the fault-free output with various test patterns. This fault-free output will be used to compare with the output when an injection of fault happens. By doing this, it can be seen whether the different test patterns can be used to detect the fault or not for the simulation. The results showed that the fault can be detected perfectly.

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CONFLICTS OF INTEREST

The authors declare no conflict of interest

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