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An NMOS transistor-based high-gain operational amplifier designed in 0.25-micron CMOS technology

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ABSTRACT: This project describes in detail the process of designing and simulating CMOS Technology is used in a one-stage folded cascode operational amplifier (SFCOA) with the self-biasing scheme for the NMOS a stage of differential input is discussed. The design of the required circuits is done using the LTspice simulator. We will see that the simulation result approximately matches with the desired and theoretically calculated performance values. We are changing width values to bring all the transistors of the circuit in saturation, then; two stage of (FCOA) technique with Miller compensation technique for the NMOS input have been employed. The operational amplifiers circuit is designed with 0.25 µm CMOS Technology using LTspice software. The applicable technique, which includes all of the design equations, has been fully stated in order to implement the circuit design for a particular specification. The parameter of Phase Margin (PM) and DC Gain are presented and discussed. Finally, a designed circuit based on NMOS input provide a 96 DC Gain has been performed.

Keywords: CMOS Technology 0.25 µm; Two stage; NMOS; DC Gain; Phase Margin; High swing cascode current mirror biasing circuit; NMOS; Saturation; High open loop DC gain

1. INTRODUCTION

CMOS (Complementary Metal Oxide Semiconductor) technology is always getting smaller so that digital systems can be made that use less power, move faster, cost less, and have more parts. Due to how quickly digital CMOS technology is changing, single-chip solutions are becoming a good choice for systems that are getting more complicated [1-5]. In the last 30 years, the world has seen a rapid growth and change in integrated circuit (IC) technologies. This is because signal processing systems are getting more and more complicated [6-11]. These ICs are used in many different fields, such as communications, medical imaging, speech processing, instrumentation, sonar,

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radar, satellite communication, … etc. Operational amplifiers (Op-amps) are a key part of many analog and mixed-signal circuit design systems [12-17]. Op-amps usually come in a few different topologies, such as the telescopic op-amp, the folded cascode op-amp, and the two stage op-amp [18-22].

This project; a two stage NMOS differential folded cascode op-amps circuit has been designed. The desired circuit is designed and simulated using LTspice software.

2. METHOD

2.1. APPLIED METHODOLOGY AND SPECIFICATIONS

A- In milestone1, a (SFCOA) using 0.25µm CMOS technology with a self-biasing scheme for the NMOS differential input stage is designed using the LTspice simulator. Design is supposed to follow the given specifications:

i) Power dissipation ≤ 2.5 mW
ii) Open loop DC voltage gain, |Av0| ≥ 500
iii) Overdrive voltage, |VOD| = 0.3 V for all transistors excluding the input pair
iv) Gate length, L = 2 µm for all transistors as shown in Figure 1.

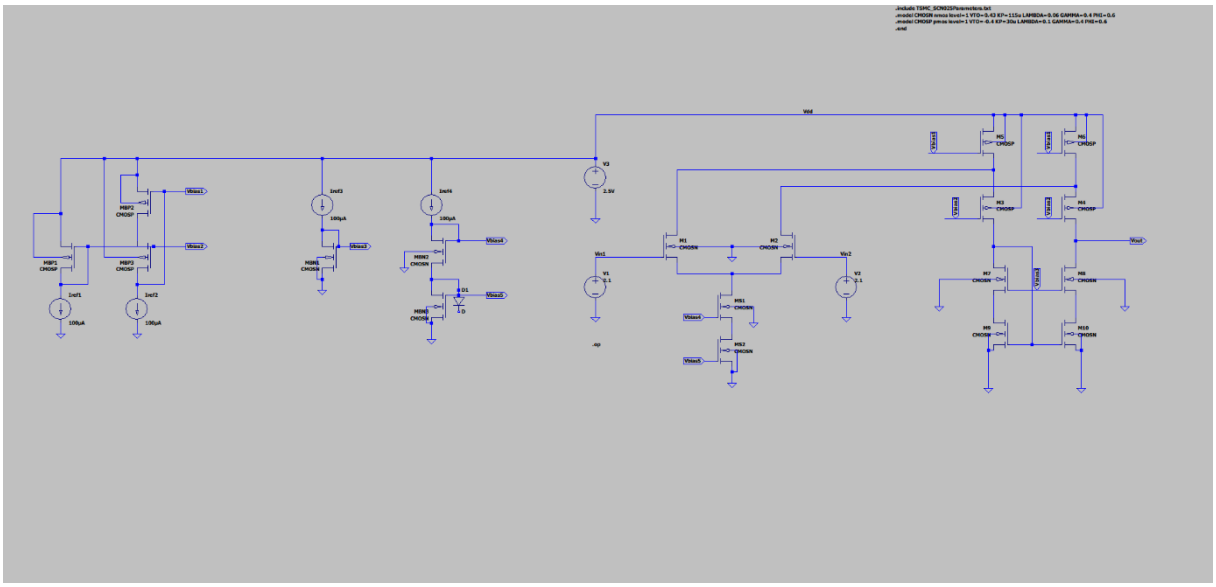

FIGURE 1. - Design of the required circuit using LTspice.

Procedures (milestone1)

Following procedures are being implemented to design the required above circuit: [23-28]

1. Initially, naming of the different transistors of the main circuit and the self-biasing circuit is done with the given format. Then, as mentioned, the tail current is replaced with the help of a cascode current source. And all the bias voltages of the circuit are implemented with the help of high-swing cascode current mirror. The different values considered here for the given above specifications are mentioned in the Table 1:

Table 1. - Specification parameters of the circuit

Parameter	Value
$\|I_{SS}\|$	100 µA
$\|I_{D5}\|$	100 µA
$\|I_{D6}\|$	100 µA
$\|V_{OD1}\|$, $\|V_{OD2}\|$	0.66V
$V_{ICM(min)}<ICMR<V_{ICM(max)}$	2.04<2.1<2.51
$V_{O(max)}<V_O<V_{O(max)}$	0.6 V to 1.9 V

2. After this, the ICMR i.e, Input Common-Mode Range is obtained using the dc analysis of the above circuit by which the transfer curve plot is obtained. This plot shows the range of V_{in} where the circuit performs correctly and also the maximum output voltage is obtained. A proper value of V_{in} (2.1 V) is chosen as common mode for the proper dc

operation of the circuit and for this particular value of V_{in}, operating point analysis (.op) is run to get the different nodal voltages and currents of the circuit. From these values, we are ensuring that all the transistors are in saturation. Or if they are not in saturation, widths of these transistors are changed accordingly to make them saturated (see Table 2) [29-35].

Table 2. – The parameter's values of the circuit.

	M_1, M_2 (V)	M_3, M_4 (V)	M_5, M_6 (V)	M_7, M_8 (V)	M_9, M_{10} (V)
V_{dsat} (VOD)	0.8	0.3	0.3	0.3	0.3
V_{ds}	1.33	1.467	0.305	0.415	0.313
Saturated?	Yes	Yes	Yes	Yes	Yes

B- In milestone 2, the project's main goal is to design a one-stage folded op amp with self-biasing scheme to the following specifications:

- Power dissipation ≤ 4 mW
- Open loop DC voltage gain, |Av0| ≥ 80 dB
- Phase margin, PM at least 45°
- Zero, |z| at least 10 GB

The op-amp that was made is mostly made up of two parts. The first part is the differential input, and the second is the high-swing cascode current mirror biasing circuit.

Procedures (milestone2): Circuit diagram and its simulation results

A theoretical study was made before the structural design with the objective of determining the dimensions of each transistor that constitute the operational amplifier to meet the required requirements [36-46].

3. RESULTS AND DISCUSSION

3.1 OBSERVATIONS (milestone 1)

In the above results of operating point analysis, different nodal voltages and currents through the transistors can be observed and can be used to bring all the transistors in the saturation region. One can see that the values obtained are approximately similar to the values obtained using hand calculations for the given specifications. To make all the MOSFETs to be in saturation, the width of MBP1 has been changed to 28 µm from 37.037 µm (as per calculations) and the width of MBN1 has been changed to 7 µm from 9.662 µm (as per calculations) as shown in Figure 2.

3.2 TRANSFER CURVE PLOT

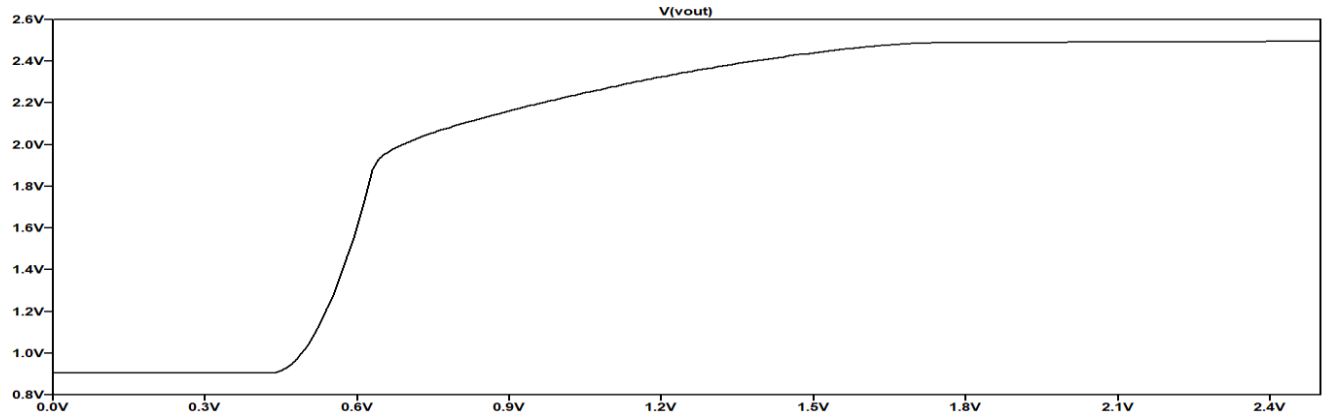

FIGURE 3. – Transfer curve plot.

From the above figure, the range of V_{in} (ICMR) is obtained using the DC analysis of the above circuit.

3.3 TRANSIENT PLOTS

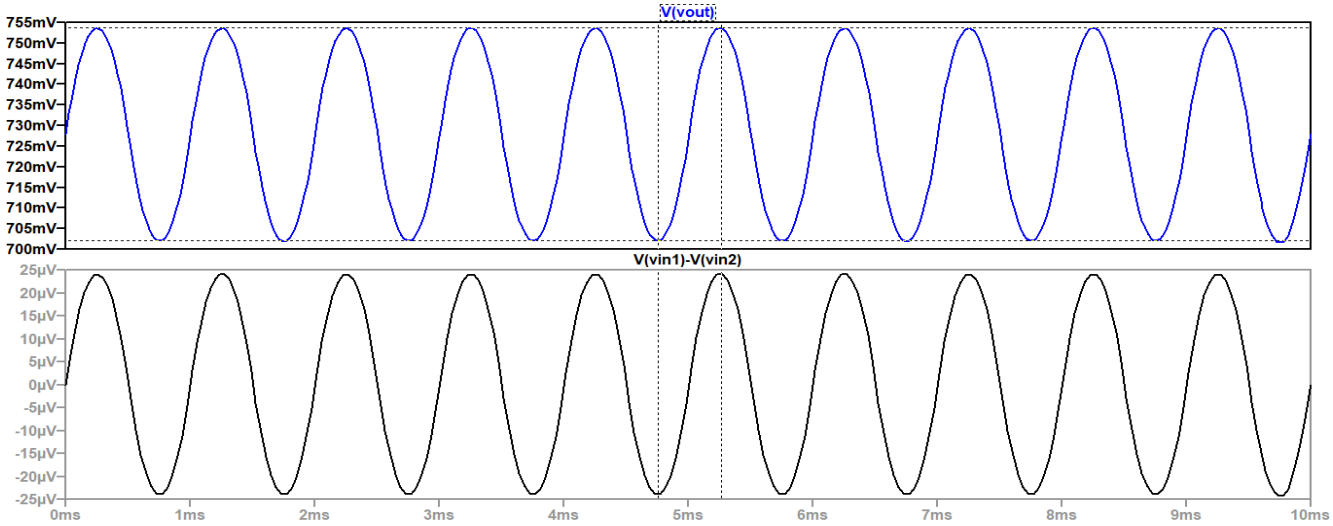

FIGURE 4. – Transfer plot.

From the above plot, the gain of the circuit is obtained and it can be seen that it is nearly what has been desired in the milestone. Voltages of the differential input and single ended output are shown in different plot panes. V_o(pp) obtained is 105.63 mV for the given sine signal mentioned above.

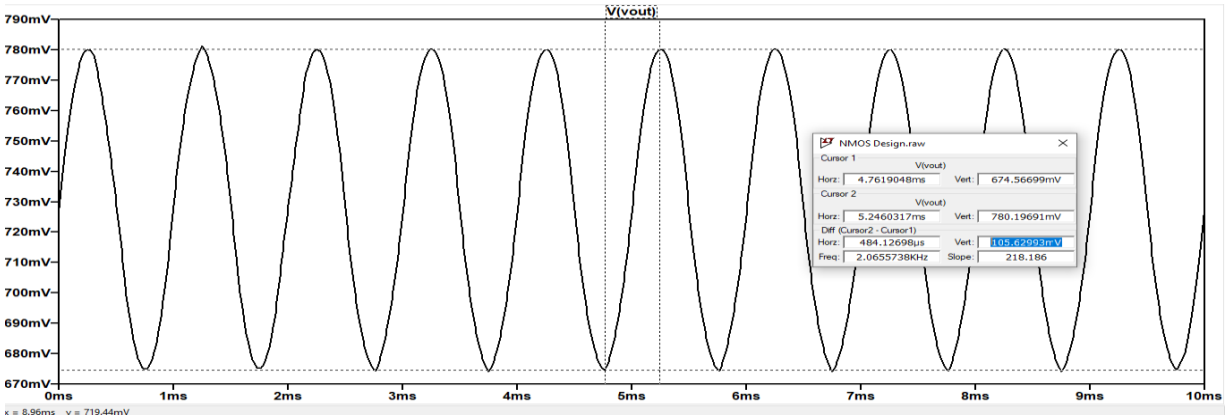

FIGURE 5. – Transfer plot.

3.4 TRANSFER FUNCTION OUTPUT

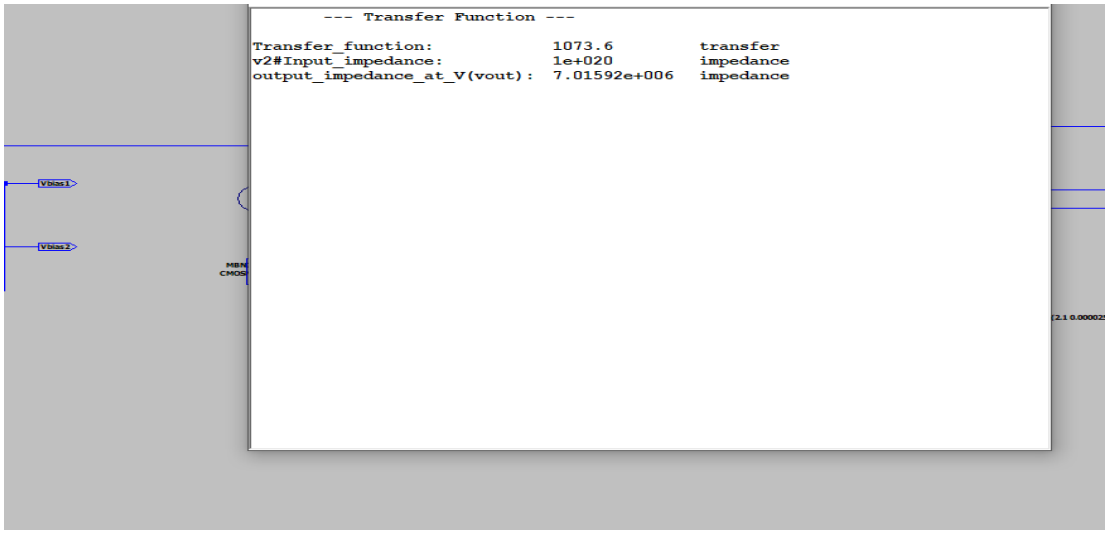

FIGURE 6. – Transfer function.

Transfer function analysis has been done to verify the gain obtained in the transient plot. It can be observed that the gains obtained in both the methods are matching with each other.

3.5 THEORITICAL CALCULATONS OF (milestone 2)

This section shows you how to design a basic miller-compensated two-stage CMOS op amp. It also gives you the basic equations for op amps. Basic op amp equations: The MOSFET, strong inversion, square law equations are listed below [47-55].

The first stage

In saturation regime, drain current depends on (W / L). The power dissipation of the designed circuit is:

$$Pdiss = (Vdd - Vss)\ (Iss + Id5 + Id6) \quad (1)$$

Where Iss= 10 µA = 2 Id1=2 Id2

$Id5 = Id6 = 67.5\ uA$ = (2.5) ($10e^{-6}$ + 2×67.5e^{-6}) = 0.3 mW < 4 mW

The Gain Equation of the circuit is:

$$Gain = gm1 * R0 = gm1\ ([gm3.rds3\ (rds1 \backslash\backslash rds5)] \backslash\backslash [gm7.rds7.rds9]) \quad (2)$$

Gain=7.2 × (3×1(1.5\\1.2)) \\ (2.4×1×1.5)

Gain= 7.2x9.5833

Gain = 69

The output resistance of M1, M3, M5, M7, M9 transistor in the circuit using

$$R0 = 1/\ (lambda.Iss) \quad (3)$$

Where $R0 = [gm3.rds3\ (rds1 \backslash\backslash rds5)] \backslash\backslash [gm7.rds7.rds9]$

R0 = (3×1(1.5\\1.2)) \\ (2.4×1x1.5)

R0 = 9.5833 KΩ

Calculation of saturation Voltage

$$V_{DSAT6} = V_{DSAT4} = \frac{1}{2}(V_{dd} - V_{outmax}) \quad (4)$$

$$V_{DSAT8} = V_{DSAT10} = \frac{1}{2}(V_{outmin} - V_{ss}) \quad (5)$$

Vdsat6 = Vdsat4 = ½ (2.5-0.8) = 0.85 V

Vdsat8 = Vdsat10 = ½ (2) = 1 V

W/L Ration of the Transistor

$$W = \frac{2LI_D}{KV_{OV}{}^2}$$

PMOS transistor

$$W = \frac{2LI_D}{K_P V_{OV}{}^2}$$

NMOS transistor

$$W = \frac{2LI_D}{K_N {V_{OV}}^2}$$

$$W_1 = W_2 = \frac{2(5\mu)(2\mu)}{(115\mu)(0.058)^2} = 51.7\ \mu m$$

$$W_3 = W_4 = \frac{2(5\mu)(2\mu)}{(30\mu)(0.3)^2} = 7.4\ \mu m$$

$$W_5 = W_6 = \frac{2(67.5\mu)(2\mu)}{(30\mu)(0.3)^2} = 100\ \mu m$$

$$W_7 = W_8 = W_9 = W_{10} = \frac{2(5\mu)(2\mu)}{(115\mu)(0.3)^2} = 1.93\ \mu m$$

The second stage

Drain current:

$$I_D = \beta {V_{OV}}^2 = \frac{\mu_{n,p} C_{ox}}{2} * \left(\frac{W}{L}\right) * {V_{OV}}^2$$

$$\beta = \frac{\mu_{n,p} C_{ox}}{2} * \left(\frac{W}{L}\right)$$

Aspect ratio:

$$\frac{W}{L} = \frac{2I_D}{\mu_{n,p} C_{OX} * {V_{OV}}^2}$$

Transconductance:

$$g_m = \sqrt{2 * \mu_{n,p} C_{OX} * \left(\frac{W}{L}\right) * I_D}$$

where VOV = (VGS -V_{tn}) for NMOS and VOV = (VSG - V_{tp}) for PMOS, will be used in the paper as a whole. For a bulk MOSFET to work well at room temperature, VOV values of more than 200 mV are usually needed for strong inversion.

Step 1: The pole P2 should be placed 2.2 times higher than the Gain on the compensation capacitor Cc. The resulting need for the minimum value for Cc is as follows:

$$C_c > \frac{2.2}{10} * C_L$$

$$C_c > \frac{2.2}{10} * 10 * 10^{-12}$$

$$C_c > 2.2 * 10^{-12}$$

$$C_c = 2.3\text{pF}$$

Step 2: The estimation of the bias current is the next step in the design process. The slew rate specification provides us with:

Slew rate:

$$(SR) = \frac{I_{SS}}{C_c} = \frac{I_5}{C_c}$$

where I_{ss} = I5 is the tail current.

$$I_5 = S.R * C_c = 50 * 10^6 * 2.3 * 10^{-12}$$

$$= 115\ \mu A$$

Step 3: Taking into account the GB created by the dominant node, we have:

$$g_{m1} = GB * C_c = 2 * \prod * f * C_c$$

$$= 0.0017 = 1.7\ \text{m}\ \Omega^{-1}$$

$$W_{11} = W_{13} = \frac{Lg_{m1}}{K_N I_5} = 437.05\ \mu m$$

Step 4:

$$W_{12} = \frac{Lg_{m1}}{K_p I_5} = 1675.36\ \mu m$$

Schematic circuit in LTspice (milestone2)

Figure 1 depicts the miller compensated two stage op amp with a reliable biasing circuit. It contains a high-swing cascode current mirror biasing circuit and two stages Op-Amp. The first stage typically consists of a differential amplifier with high gain. The common source amplifier typically satisfies the second stage's requirements and has a moderate gain.

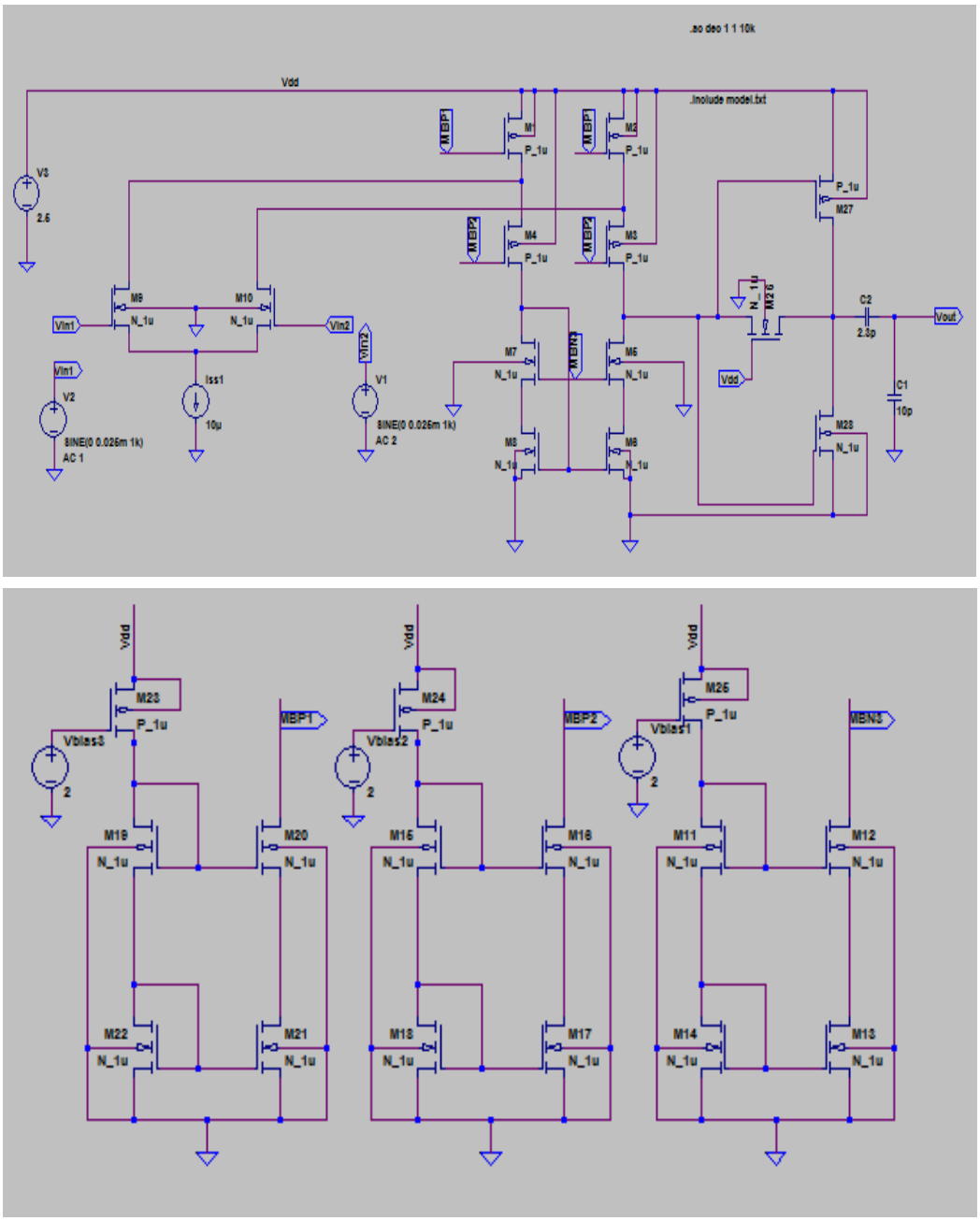

FIGURE 7. - Two-Stage OP-Amp miller compensated.

Table 3. - Electrical characteristics of designed circuit.

Parameter	Value
P_D	10.72
A_{v0}	96 dB
GB	10
PM	1.6°

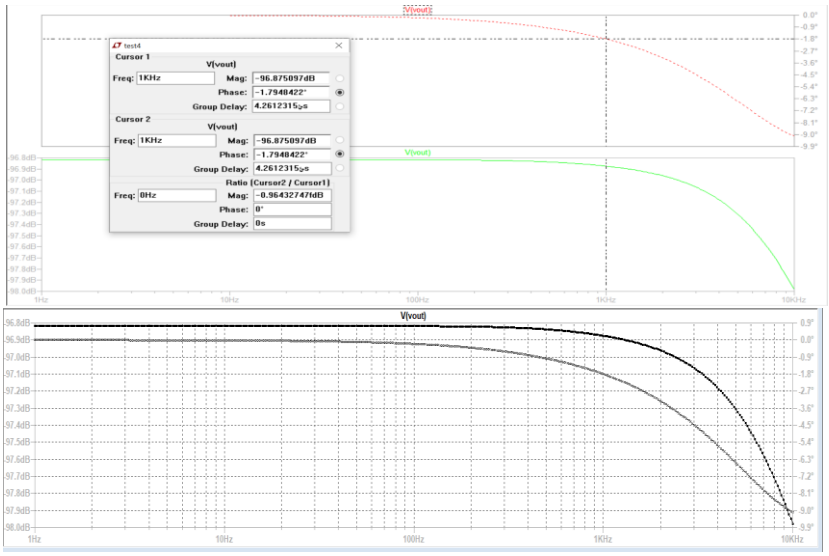

FIGURE 8. - Gain and phase margin results

Simply put, the gain of the amplifier with infinite input resistance is the transconductance of the totally differential folded cascode op-amps. We have designed an op-amp with a gain more than 96 dB and a PM of: It serves as a gauge for the system's stability. The TSMC 0.25 µm Technology is used throughout the simulation and the minimum channel length of the transistors is set to 2 µm. The fully differential folded cascode op-amps were used in the simulation with 2.5 supply voltages at both NMOS input.

Table 4. - Resulted from simulation

Parameter	NMOS input
Gain (dB)	96
Phase Margin (°)	1.8

The fully differential folded cascode op-amp for NMOS input is 96 dB, according to our examination of the table.

4. CONCLUSION

In conclusion, a (one-SFCOP) using 0.25 µm CMOS Technology with the self-biasing scheme for the NMOS differential input stage is designed. The procedures and hand calculations required for different transistors's widths and voltage biases are attached herewith. From the above simulation results, it can be notices that the circuit designed is performing as per desired. The high ICMR and high open-loop DC voltage gain is obtained. The range of Vin (ICMR) is obtained using the DC analysis of the above circuit. Using transient analysis, the gain of the circuit is obtained and it can be seen that it is nearly what has been desired in the milestone. Transfer function analysis verifies the gain obtained in the transient plot. From the netlist of the design, different nodal voltages and currents through the transistors can be observed and have been used to bring all the transistors in the saturation region. It can be seen that the values obtained are approximately similar to the values obtained using hand calculations for the given specifications. As we can see, with thorough design calculations, the design of single ended, two-stage operational amplifiers is described. According to simulation data, the op amp has a unity gain frequency of 1 kHz and an open loop DC gain of 96 dB.

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