Low temperature epitaxial graphene on 3C-SiC surface induced by carbon evaporation

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المستخلص

بواسطة القصف بالكاربون تم تحوير طريقة تحضير الجرافين على سطوح السيلكون كارباید Sic. عملية تبخير الكاربون اثرت على ديناميكية نمو مادة الجرافين على السيلكون كارباید السداسي لقد تم الحصول على الجرافين بواسطة تبخير الكاربون عليه بدرجات حرارة واطئه تصل الى حد 950 درجة مئوية في حالة (0001) Sic . بهذه الطريقة تم الحصول على طبقة احادية من الجرافين والذي تم التأكد عليه بواسطة عدة تقنيات نانوية كحيود الالكترونات منخفضة الطاقة (LEED) والكهروضوية فوق البنفسجية (ARUPS) .

لقد تم الحصول على طبقة الجرافين الصفرية على سطح 3C-Sic وبنفس الطريقة اعلاه وبدرجة حرارة منخفضة ايضآ عند حوالي 1000 درجة مئوية ولقد تم التاكد من ذلك بواسطة مطياف الاشعة البنفسجية الكهروضوئي (XPS) وتقنية (LEED) .بنفس الطريقة يمكن الحصول على مادة الجرافين على سطح ال 3C-Sicبواسطة تبخير الكاربون علية عند درجات حرارة منخفضة.

Abstract

With the carbon bombardment, the procedure of producing graphene on SiC surfaces is modified. The carbon evaporation influences the dynamical growth of graphene on the hexagonal SiC. The epitaxial graphene induced by carbon evaporation is obtained at lower annealing temperatures of about 950 oC in case of SiC(0001). By this method, we were able to construct a monolayer graphene which is confirmed by low energy electron diffraction (LEED) and angle resolved ultraviolet photoelectron spectroscopy (ARUPS). On the 3C-SiC surface, zero-layer graphene is obtained at annealing temperatures of about 1000 oC as this evident by X-ray photoelectron spectroscopy (XPS) and LEED. Similarly, carbon evaporation on the 3C-SiC surface can be applied in order to get graphene at reduced temperatures.

Introduction

Graphene is a flat sheet of carbon atoms tightly bonded into a two-dimensional (2D) honeycomb lattice. Due to its extraordinary properties, especially the high carrier mobility, graphene rapidly becomes a rising star on the horizon of material sciences (1-4). Therefore, in the last few years, geaphene receives a tremendous attention for developing graphene-based electronics. The notion of graphene stands for monolayer graphene, bilayer graphene, and several graphene layers (up to ten layers). More than about ten layers are practically indistinguishable from bulk graphite. In addition to its unconventional electronic structure, graphene represents the building block of fullerenes and carbon nanotubes (CNTs). The micromechanical cleaving technique yields large graphene flakes but it is a very complicated and time consuming process,

as a consequence, the device fabrication is going to be cumbersome. However, for the purpose of graphene-based electronics, the epitaxial growth of graphene by thermal decomposition of SiC surfaces seems to be the most promising method (5-10). Nevertheless, the control of the preparation conditions for large homogenous graphene area is still under investigation. Different kinds of surface analysis techniques have been used in this work such as low energy electron diffraction (LEED), angle resolved ultraviolet photoelectron spectroscopy (ARUPS), atomic force microscopy (AFM), and X-ray photoelectron spectroscopy (XPS). One of the severe issues is the exact determination of the graphene layers on top of the SiC surfaces. It is known that LEED fingerprint is capable to determine the thickness of graphene layers (up to three layers) on hexagonal SiC(0001) which is produced at high annealing temperatures of about 1250 oC (11). Thus, the principle of LEED fingerprint has been adopted in the current work. The LEED fingerprint of monolayer graphene is calibrated via (ARUPS) with He II excitation at 41.8 eV photon energy from laboratory based UV source, accordingly, avoiding the necessity of the synchrotron based angle resolved photoemission spectroscopy (ARPES) measurements. The most important thing to get monolayer graphene is to have zero-layer graphene $(6\sqrt{3}\times6\sqrt{3})R30°$ which is also known as precursor phase. For the surface annealing process in the current work, the electron beam heating method is used. In the present letter, the influence of carbon deposition on 3C-SiC(111) crystal surface was investigated. **Experiment** Hexagonal SiC samples were hydrogen etched to get rid of the polishing-induced damage (12), to chemically passivate the surface [13]. The 3C-SiC(111) surface was cleaned before its introduction into the UHV system. However, this cleaning procedure was applied to all samples no matter to what polytype. The aim is to get rid of the dirt or any tiny particle that might get stuck on the surface of the sample. Cleaning the sample is also recommended before any AFM measurements to avoid deformed micrographs. The tools used for this procedure are Acetone, Methanol, and an ultrasonic bath. AFM images show regular array of atomically flat terraces of about 1 μm width (14). First of all, the sample is mounted to the load-lock chamber (the entrance of our UHV system). Then, it is transferred to the preparation chamber where the annealing and Si-deposition processes are carried out. Usually, the sample is annealed to about 900°C-1000°C for one minute in order to get rid of the contaminants (especially oxidic layers) on the surface of the sample prior to its introduction, see Fig. 1. Thereafter, several essential preparation processes are applied in order to achieve the required reconstruction.

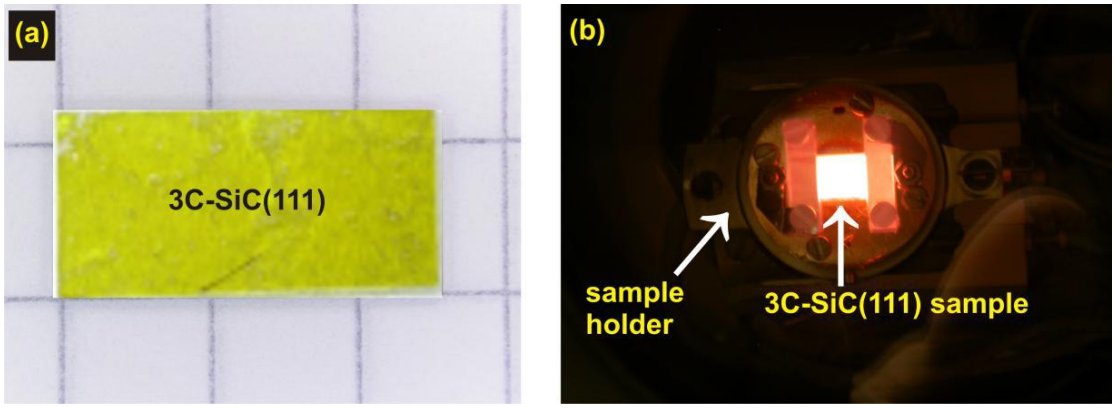


Figure (1): The sample used in the current paper: (a) the 3C-SiC(111) surface prior to its upload into the UHV system, (b) the sample while it is annealed to about 950°C

Once the cleaning process is achieved, the sample was treated by Si deposition (1 ML/min) and annealing (around 800 oC) (15) in order to obtain the starting point for the current procedure, namely, the Si rich (3×3) reconstruction as can be seen in Fig. 2 (b). The reason behind preparing the Si rich (3×3) reconstruction is to start from a periodicity where the carbon has no way to present in order to notice the graphitization process later as indicated by (√3×√3)R30°, and (6√3×6√3)R30° reconstructions, cf. Fig. 2 (c) and (d). Results Starting from the Si rich (3×3) reconstruction, cf. Fig. 2 (b), which is prepared by annealing the 3C-SiC(111) surface under simultaneous Si flux.

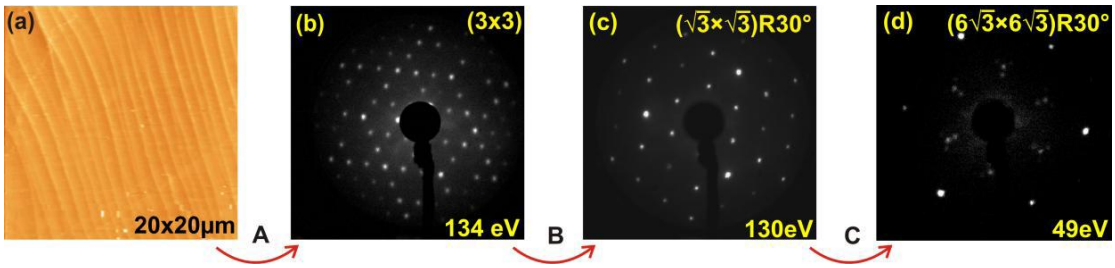
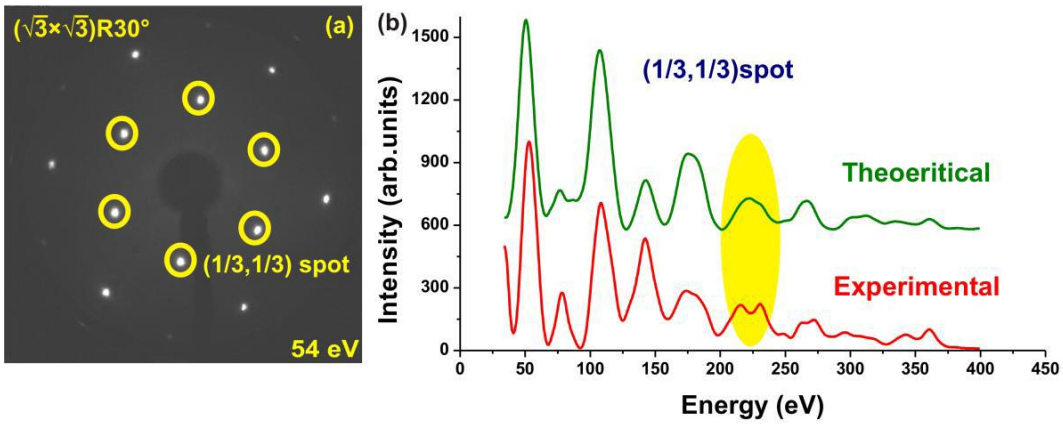


Figure (2): Phase diagram of the 3C-SiC(111) surface: (a) An AFM micrograph shows the morphology of the 3C-SiC(111) surface

LEED images of the (b) (3×3), (c) (√3×√3)R30°, and (d) (6√3×6√3)R30° reconstructions on 3C-SiC(111). Different preparation steps are indicated by the letters associated with arrows. In particular, the (√3×√3)R30° periodicity should be as sharp as possible so that perfect LEED spectra (IV-curves) can be accomplished. The most important is: remaining patches of the (3×3) structure should be gone and (6√3×6√3)R30° spots should not be there yet. A practical fingerprint for a homogeneous surface phase is that the IV-curves should go to zero at their minima. Hereby, this necessarily leads to a good theoretical fitting. It is known that the (1/3,1/3) diffraction order spot is characteristic for the (√3×√3)R30° structure [16]. Therefore, LEED intensity spectrum of this spot is performed. LEED intensity spectra of (1/3,1/3) diffraction order spot for the (√3×√3)R30° structure were measured for different preparation conditions and samples. The LEED spectra in Fig. 3 (b) are

theoretical and experimental (1/3,1/3) diffraction order spot for the (√3×√3)R30° periodicity on 3C-SiC(111) surface by means of annealing only (conventionally). While LEED spectra in Fig. 4 of the same spot diffraction order are both experimental on hexagonal SiC surface. The top spectrum (in black) is conventionally prepared, whereas the bottom one (in red) belongs to the carbon evaporation under low annealing temperatures. Obviously it coincides with the LEED intensity spectrum of the same spot performed from a conventional and carbon assisted (√3×√3) R30° structure, cf. LEED intensity spectra in Fig. 3 and Fig. 4.



Figure(3): LEED spectra measurement of 3C-SiC(111): (a) (√3×√3)R30° reconstruction LEED pattern shows the spot (1/3,1/3) diffraction order which are surrounded by circles. (b) LEED spectra (IV-curves) showing the coincidence of theoretical and experimental LEED spectra

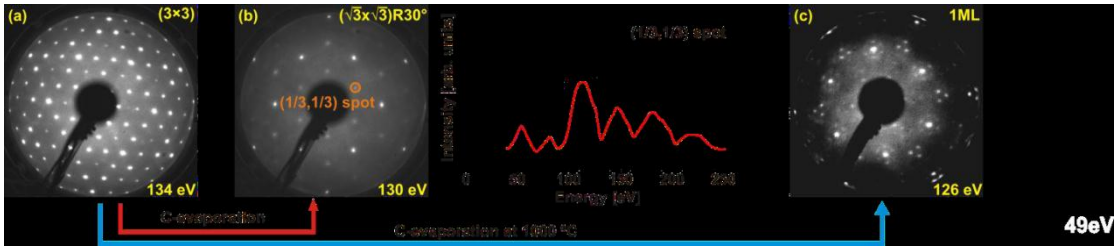


FIG. 4: (a) LEED pattern of the (3×3) phase on SiC(0001), (b) LEED pattern of the carbon source induced (√3×√3)R30° structure together with LEED intensity spectra of its (1/3,1/3) spot (bottom in red) and for comparison the corresponding spectrum for conventional preparation (top in black), and (c) LEED pattern of monolayer graphene grown with assistance of carbon deposition

The (1/3,1/3) diffraction order spot was measured over the complete energy range starting at 35 eV. This spot is illustrated in Fig. 3 (a) while (b) of the same figure showing the LEED spectra. The LEED IV-curves in Fig. 3 (b) demonstrate a full agreement all over the energy scan. At around 225 eV, experimental spectrum has double small peaks while the theoretical one shows a single (envelope) peak, cf. the

yellow shaded area in Fig. 3 (b). However, experimental carbon induced (1/3,1/3) spot spectrum (bottom in red) in Fig.4 has no double peak around 225 eV and hence coincides even with the theoretical spectrum.Slightly higher annealing temperatures result in a carbon richer structure: Further annealing temperatures to about 1000°C for 30 minutes result in the beginning of the (6√3×6√3)R30° reconstruction (zerolayer) as judged by the LEED pattern in Fig. 2 (d). This process is shown by step "C" in Fig. 2. Note that the (6√3×6√3)R30° reconstruction normally starts to develop around 1100°C (16). The beginning formation of this phase is evident by the small shoulder in the XPS carbon peak shown around 285 eV (17) in Fig. 5. In principle, this absolutely indicates the possibility to obtain graphene at a bit higher annealing temperatures on 3C-SiC(111) surface as well (18).

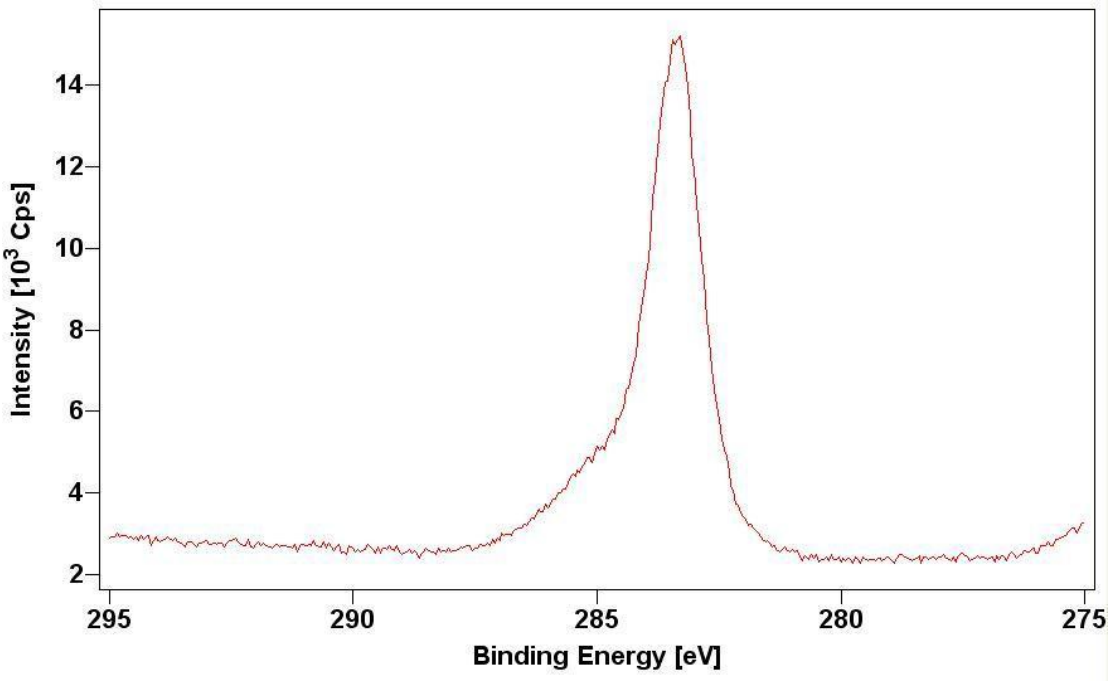


Figure (5): The XPS carbon (C1s) peak shows the beginning formation of the (6√3×6√3)R30° reconstruction

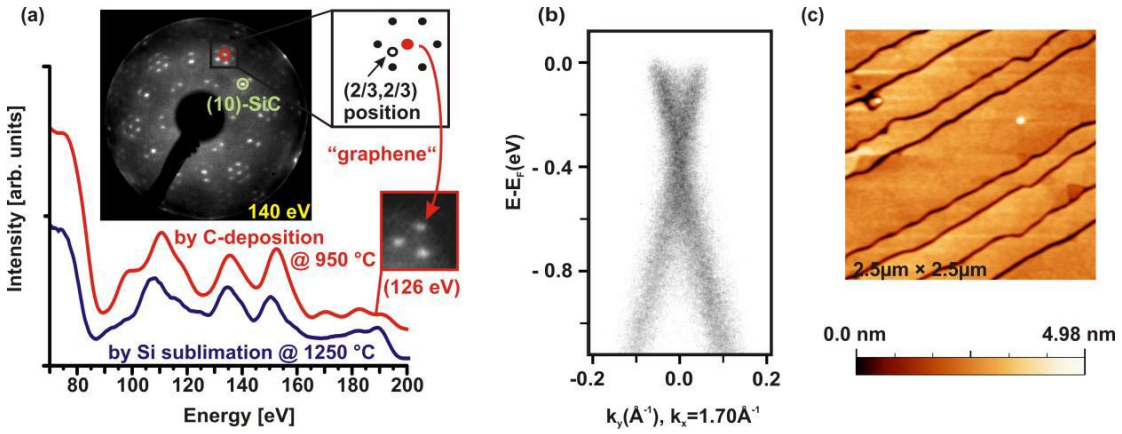


Figure (6): Epitaxial monolayer graphene on SiC grown by carbon deposition and simultaneous annealing to about 950 oC: (a) LEED pattern at 140 eV with the (10) spot of the SiC substrate indicated, and a close-up view at 126 eV for the region around the first order graphene diffraction spot (centre spot in the schematic inset). Below, intensity spectra of the graphene related spot are shown for carbon assisted growth (top) and for conventional growth by annealing in UHV (bottom). (b) π-bands dispersion perpendicular to the - direction as obtained from ARUPS. (c) AFM micrograph showing the morphology of the carbon source induced monolayer graphene sample

Thus, the zerolayer graphene or the $(6\sqrt{3}\times6\sqrt{3})R30°$ reconstruction was obtained as confirmed by two powerful techniques, namely, LEED and XPS. Therefore, the condition to get monolayer graphene is fulfilled. Likewise, monolayer epitaxial graphene can also be obtained when 3C-SiC(111) surface experiences low annealing temperature under simultaneous carbon deposition as this shown above in Fig. 6 (18). Summary In summary, we have shown quite good $(\sqrt{3}\times\sqrt{3})R30°$ periodicity as indicated by sharp LEED crystallography and spectra measurements on 3C-SiC(111) surface qualifies this surface to be promising in the lane of further graphitization. Based on LEED and XPS measurements of the $(6\sqrt{3}\times6\sqrt{3})R30°$ reconstruction, graphene can also be obtained on the 3C-SiC(111) surface. As is mentioned, graphene requires high annealing temperatures about 1250°C. However, these high annealing temperatures would be sufficient to decompose Si from the substrate. Thus, the decomposition of the Si will create a problem. Another problem will be Si segregates to the SiC surface through grain boundaries and hence sufficient carbon rich conditions may not be reached. To overcome this problem, a possible solution would be to apply the idea of obtaining graphene by carbon deposition at reduced temperatures, namely, 950°C (18). What makes it special is that 3C-SiC samples can be obtained on top of a Si substrate. Thus, in principle, graphene can be obtained on a Si substrate too. Therefore, graphene with its extraordinary electronic properties can be produced on top of the cheapest known semiconductors. From the industry

perspective, this is a quite promising path in terms of industrial expenses and hence profitable.

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