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A study of MOSFET Device for the characterization of ID-VG and ID-VD Curves

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ABSTRACT: In this paper, the MOSFET device structure has been simulated using an open-source simulator and the characterization of the ID-VG and ID-VD curves has been studied. The n-channel MOSFET device structure for three distinct generations has been simulated using the provided parameters, getting the corresponding I-V curves and observing their surface charge - V_g properties using the online simulator Nanohub. Based on the reported electrical characteristics, we may deduce that the V_{th} values decrease when the MOSFET device is scaled down. The current Id when V_g is zero is substantially higher in the third generation of the device than in the first and second generations, indicating that there is greater leakage current. Consequently, this is the punch through effect because current flows regardless of the gate voltage (i.e. even gate voltage is zero). Therefore, the device's third generation is poorly developed. In terms of performance, we can infer that the first iteration of the design is superior than the second and third generations. Therefore, substrate doping may be enhanced further for the second and third generation, while oxide thickness can be lowered further for improved performance. As the concentration of doping increases, however, we must additionally consider the influence of ionization .

Keywords: MOSFET device, ID-VG and ID-VD Curves, Vth, Vg, Id.

1. INTRODUCTION

Over the few decades, the microelectronic industry has greatly benefitted from the MOSFET scaling or miniaturization [1]. The shrinking of the MOSFETs allows hundreds of millions of transistors to be placed on a single silicon chip [2]. The miniaturization in MOSFETs, over the years, has enabled higher device density in ICs and has improved the operating frequency and therefore the overall performance of the devices [3].

As Gordon Moore observed, the density of electronic components in a IC doubles every year, this prediction of him has become a target for miniaturization in the semiconductor industry [4]. Later Robert H. Dennard described how transistors could be scaled reliably to smaller dimensions (essence of Moore's Law) [5]. He showed how to reduce the

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transistor's major parameters, including the operating voltage, capacitance, and power, as the transistors become smaller which is shown in Figure 1.

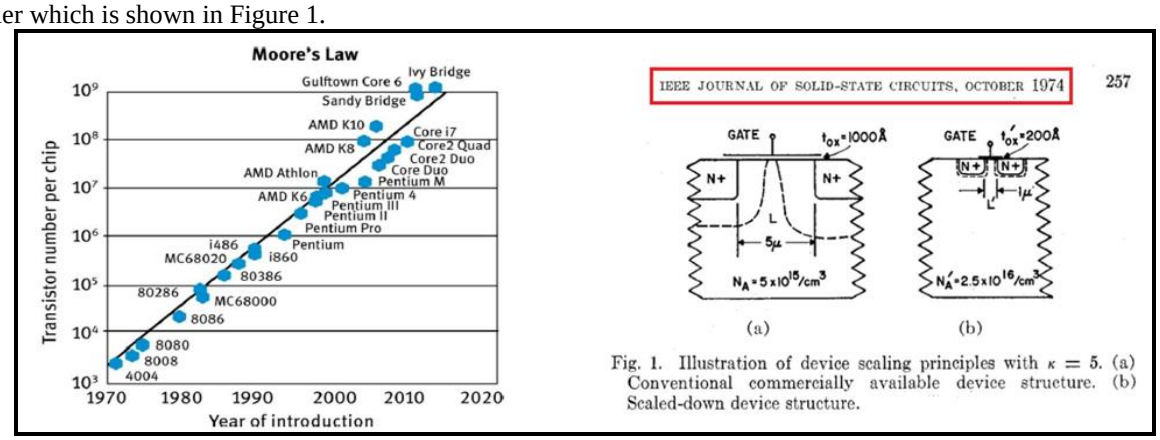

Fig. 1. Illustration of device scaling principles with $\kappa = 5$. (a) Conventional commercially available device structure. (b) Scaled-down device structure.

FIGURE 1. - Device scaling principles with, (a) conventional commercially available device structure. (b) Scaled-down device structure

So, with every technology node, the area of the transistors has been scaled down to half i.e., the gate channel length is made 0.7 times the previous value. The technology node refers to a specific manufacturing process and its design rules. Different nodes often imply different circuit generations and architectures [6]. Moore's Law as shown in Figure 2.

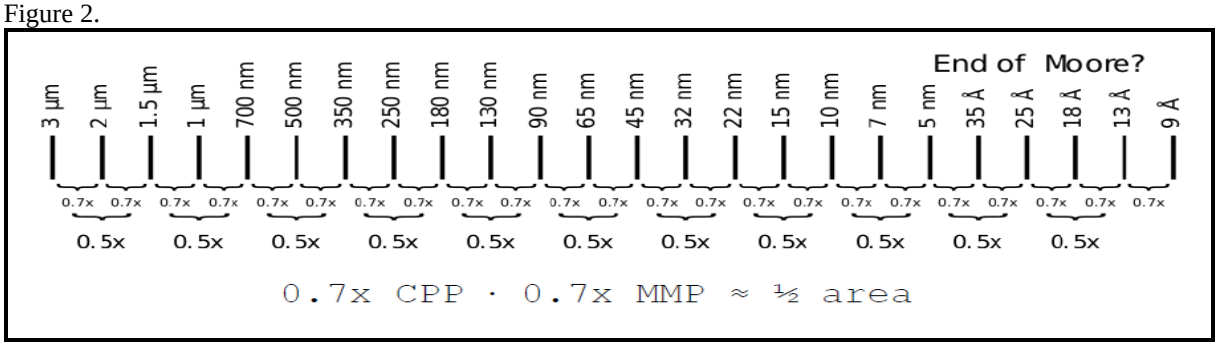

FIGURE 2. - Moore's Law

However, apart from these advantages of MOSFET scaling, there are certain limitations also [7]. Because of this, maintaining good performance over the years has become very difficult. The major issues of MOSFET device scaling have been described in sections 2 and 3.

1. SHORT CHANNEL EFFECTS OF MOSFET

This phenomenon happens when the gate channel length becomes comparable to the sums of the depletion region's length of source and drain side. Therefore, if channel doping is very low, which is needed to have the required threshold voltage, the punch-through effect can occur [8].

2. PUNCH-THROUGH EFFECT

This happens when the depletion regions around the drain and the source of the MOSFET contact each other and form a single depletion region. Thus, current flow increases very rapidly and is not controlled by the gate voltage. The amount of punch-through current is dependent largely on the applied drain voltage and on the source or drain junction depths [9]. Because of this effect, the sub threshold leakage current increases that result in the increment of power dissipation as shown in Figure 3.

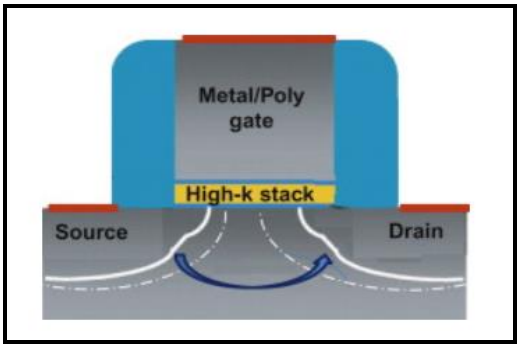

FIGURE 3. - Schematic view of a MOSFET, Large drain bias can result in "punch-through".

Punch-through effect can be reduced by increasing the channel doping and decreasing the oxide thickness. In this case, the drain and source depletion regions will be reduced and no parasitic current path is formed.

However, other short channel effects also appear when the channel length is reduced and channel doping is increased. One of the major effects is the Impact Ionization process [10-22].

3. IMPACT IONIZATION

Because of the reduced channel length, as the channel doping increases, the critical electrical field in the channel, due to reversed-biased drain-channel junction, increases rapidly. Thus, free carriers are accelerated under a high electric field to gain sufficient kinetic energy, allowing them to promote an electron from the valence band to the conduction band and therefore resulting in the creation of an extra electron-hole pair, the holes get swept towards the negatively charged substrate causing generation of substrate current, also known as avalanche breakdown [23-30], impact ionization as shown in Figure 4**.**

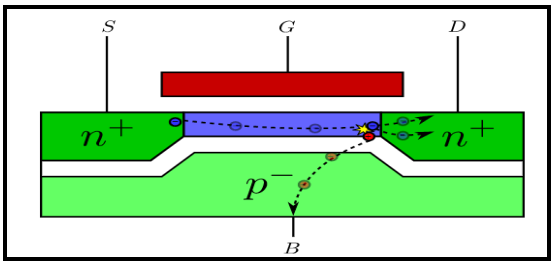

FIGURE 4. - Impact Ionization.

2. RESULTS AND DISCUSSION

In this project assignment, we will simulate following three generations of devices with the given parameters and without impact ionization included in the model

a) **First Device:** Channel length - 100 nm; Substrate Doping - $1 \times e^{17}\, cm^{-3}$; Oxide thickness - 3 nm; **First device** as shown in Figure 5.

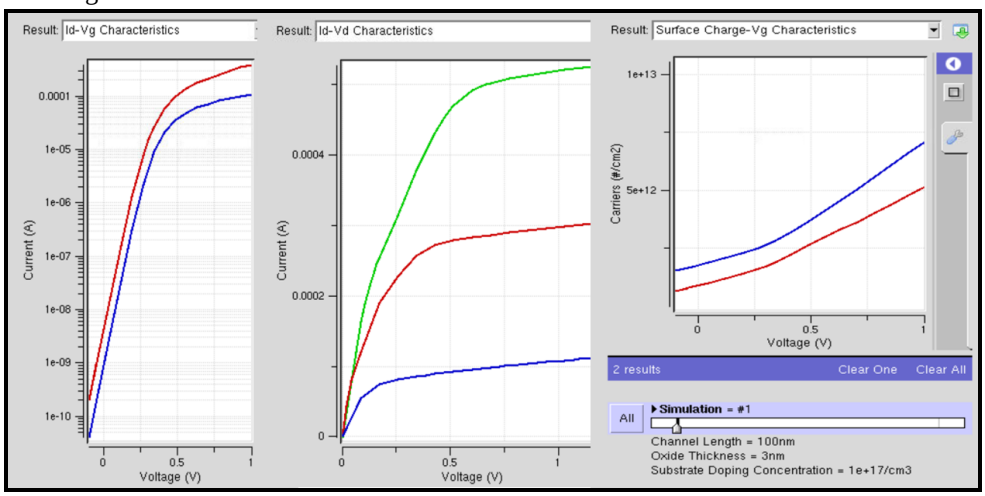

FIGURE 5. - First device.

- From the plot of I_d-V_g Characteristics, we can see that we are simulating the device for both maximum (V_d = 1 V) and minimum (V_d = 0.05 V) voltage biasing. We can see that the performance of the device is better and more accurate when it is biased at maximum voltage biasing i.e., 1 V.
- In the next part of the above plot, it can be noticed that the current ID is plotted against the VDS for three particular values of VGS. It can also be noticed that the current gap between different plots varies quadratically with the respective VGS differences. Thus, the device is in saturation.
- In the final part of the above plot, it is showing Surface Charge - V_g Characteristics for both maximum and minimum voltage biasing. The surface charge density for the minimum voltage scaling is more than that for maximum scaling for the same value of V_g.

b) Second Device: Channel length - 60 nm; Substrate Doping - $6 \times e^{17}\, cm^{-3}$; Oxide thickness - 2 nm;

Here, as the channel length is decreased (scaled), so to eliminate the punch through effect, the substrate doping is increased and oxide thickness is reduced. Thus, the drain and source depletion regions will be reduced and no parasitic current path is formed and punch through effect is avoided. **Second device** as shown in **Figure 6**.

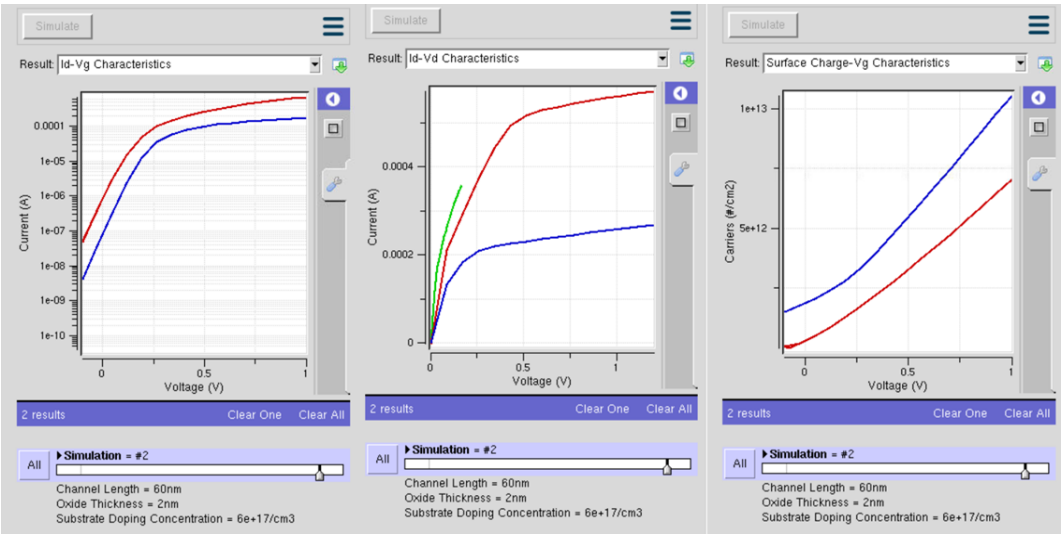

FIGURE 6. - Second device.

- From the plot of I_d-V_g Characteristics, it can be seen that we are simulating the device for both maximum (V_d = 1 V) and minimum (V_d = 0.05 V) voltage biasing. It can also be observed that the current I_d when V_g is zero is significantly more than the first device i.e. leakage current has increased.
- In the next part of the above plot, it can be noticed that the current ID is plotted against the VDS for three particular values of VGS. It can also be noticed that the current gap between different plots varies quadratically with the respective VGS differences. Thus, the device is in saturation. In addition, the drain current is more than the first device for similar values of V_d and V_g.
- In the final part of the above plot, it is showing Surface Charge - V_g Characteristics for both maximum and minimum voltage biasing. The surface charge density for the minimum voltage scaling is more than that for maximum scaling for the same value of -V_g. It can be noticed that the surface current is increasing with the voltage scaling.

c) Third Device: Channel length - 45 nm; Substrate Doping - $6 \times e^{17}\, cm^{-3}$; Oxide thickness - 2 nm;

Here, channel length is further decreased i.e. scaled. As shown in Figure 7.

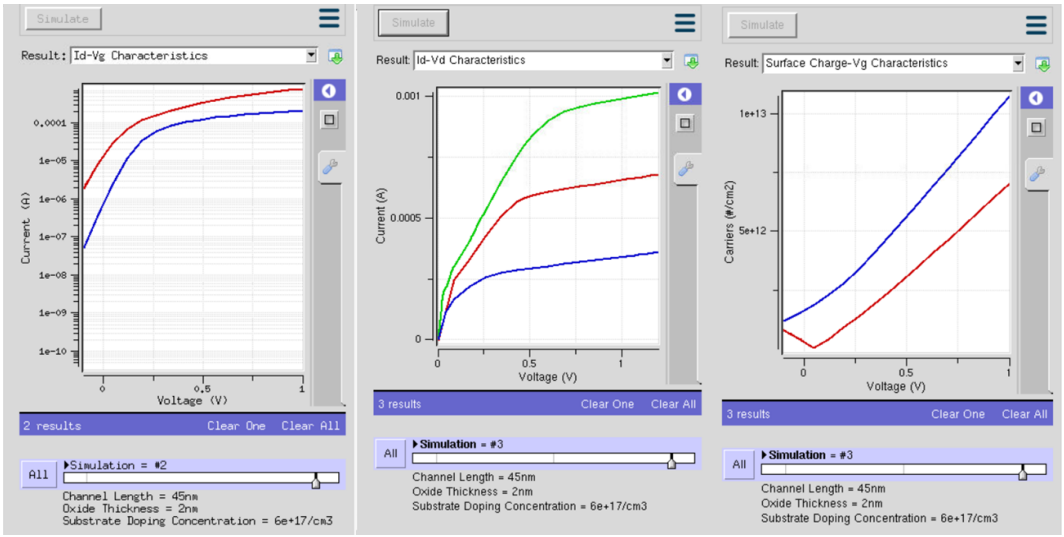

FIGURE 7. - Third device.

- From the plot of I_d-V_g Characteristics, it can be seen that we are simulating the device for both maximum (V_d = 1 V) and minimum (V_d = 0.05 V) voltage biasing. It can also be observed that the current Id when V_g is zero is significantly more than the first and second device and hence there is more leakage current. Hence, this is the sign of punch through effect as current is flowing irrespective of the gate voltage (i.e., even gate voltage is zero).
- In the next part of the above plot, it can be noticed that the current ID is plotted against the VDS for three particular values of VGS. As the gap remains same for the drain current for the similar V_g gap, thus, it denotes that it is a short channel effect and the device is saturated for very less value of V_d compared to first and second device. In addition, the drain current is more than the first and second device for similar values of V_d and V_g.
- In the final part of the above plot, it is showing Surface Charge - V_g Characteristics for both maximum and minimum voltage biasing. The surface charge density for the minimum voltage scaling is more than that for maximum scaling for the same value of V_g.

3. MANUAL CALCULATION OF THE ELECTRICAL PROPERTIES (V_{th}, I_{on} AND I_{off})

a) **First Device:** For maximum scaling i.e. V_d = 1 V as shown in Figure 8.

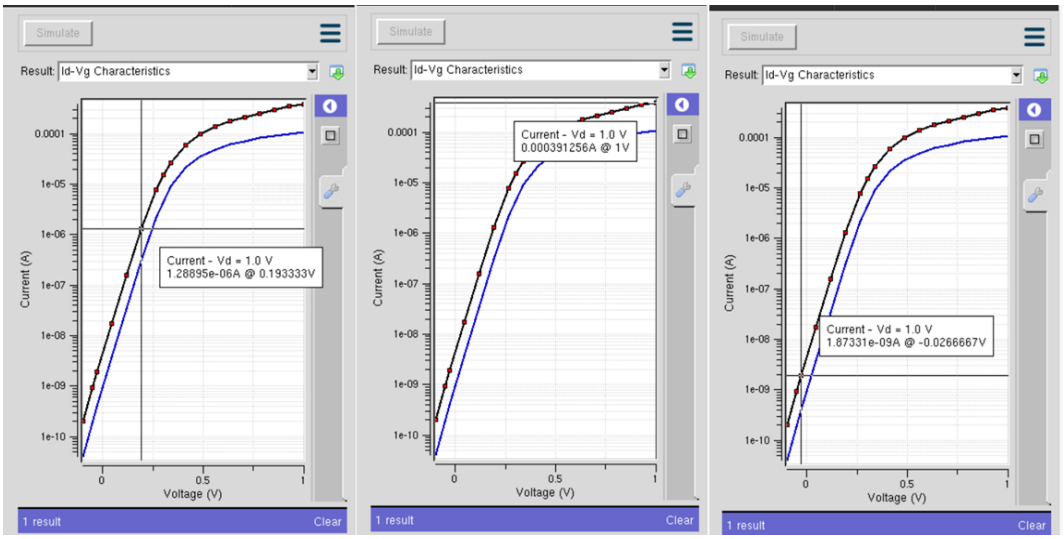

FIGURE 8. - V_{th} **= 0.193** V; I_{off} **= 1.87** $e^{-9}A$; I_{on} **= 0.39** mA.

In Figure 9, the minimum scaling i.e. $V_d = 0.05\ V$

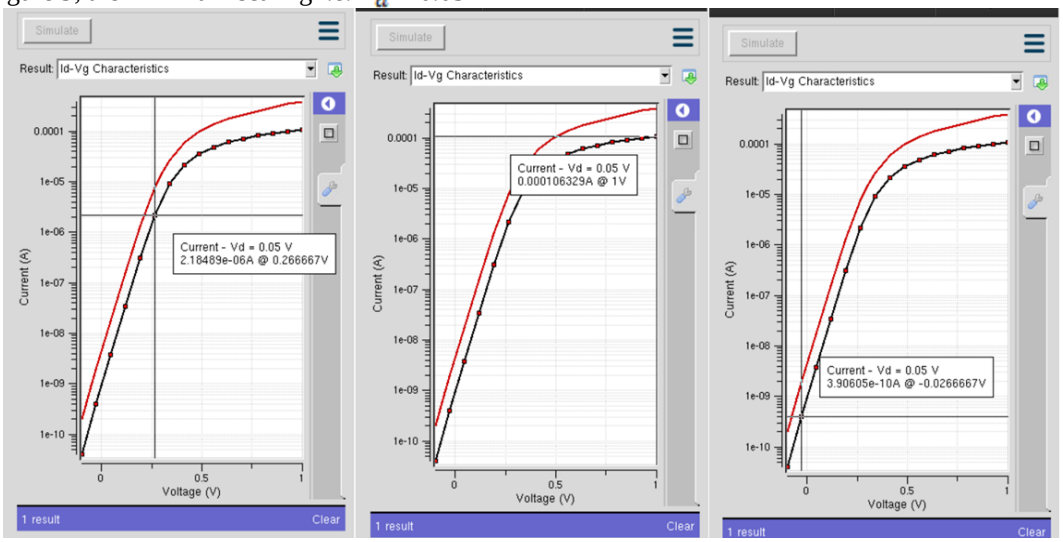

FIGURE 9. - $V_{th} = 0.266\ V$; $I_{off} = 3.9e^{-10}\ A$; $I_{on} = 0.106\ mA$.

b) **Second Device:** For maximum scaling i.e. $V_d = 1\ V$ as shown in Figure 10.

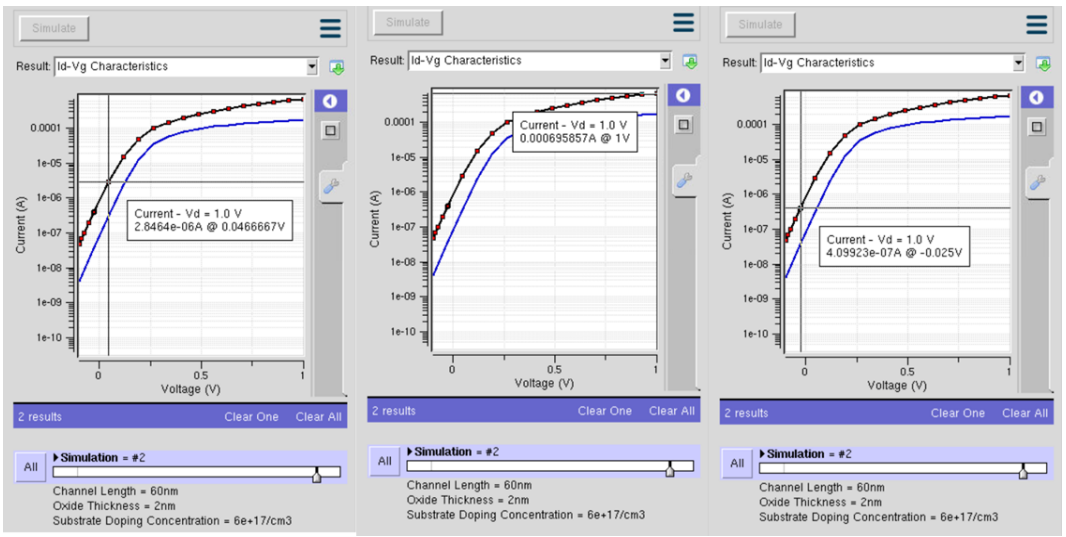

FIGURE 10. - $V_{th} = 0.046\ V$; $I_{off} = 4.09e^{-10}\ A$; $I_{on} = 0.695\ mA$.

Figure 11 shows the minimum scaling i.e. $V_d = 0.05\ V$.

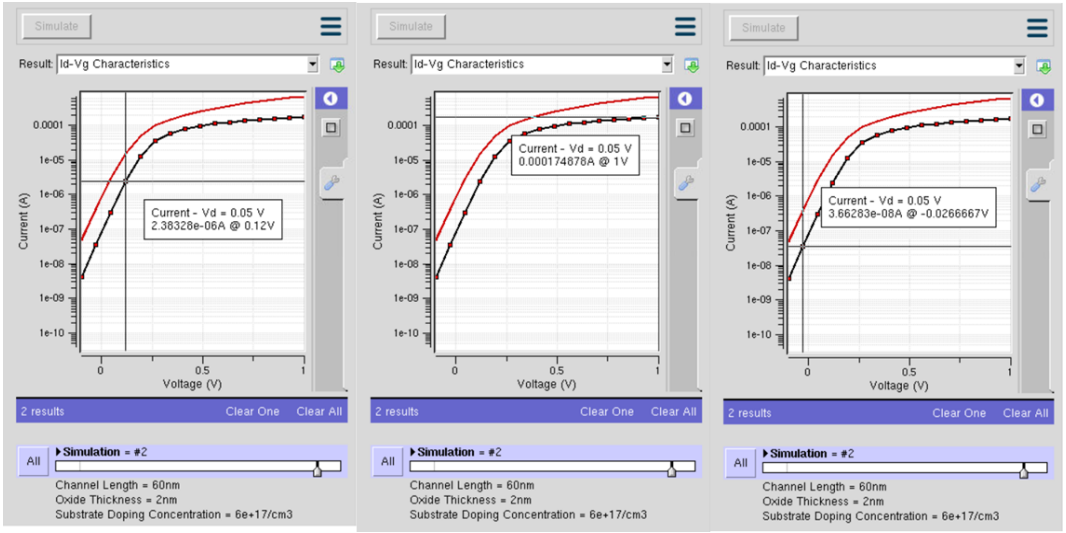

FIGURE 11. - V_{th} = 0.12 V; I_{off} = 3.66e^{-8} A; I_{on} = 0.175 mA.

c) **Third Device:** For maximum scaling i.e. V_d = 1 V as shown in Figure 12.

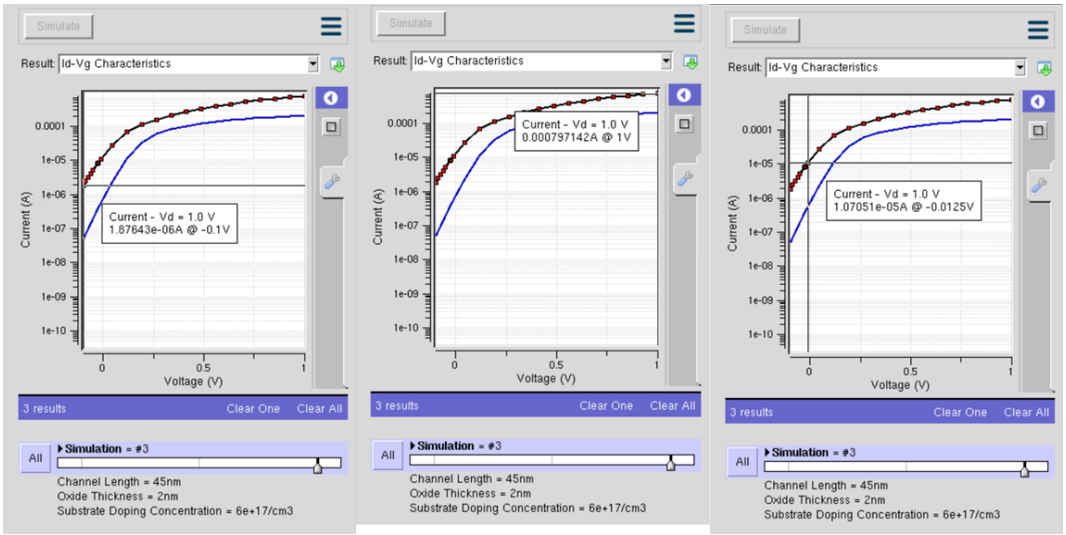

FIGURE 12. - V_{th} =-0.1 V; I_{off} = 1.07e^{-5} A; I_{on} = 0.797 mA.

Figure 13 shows the minimum scaling i.e. V_d = 0.05 V.

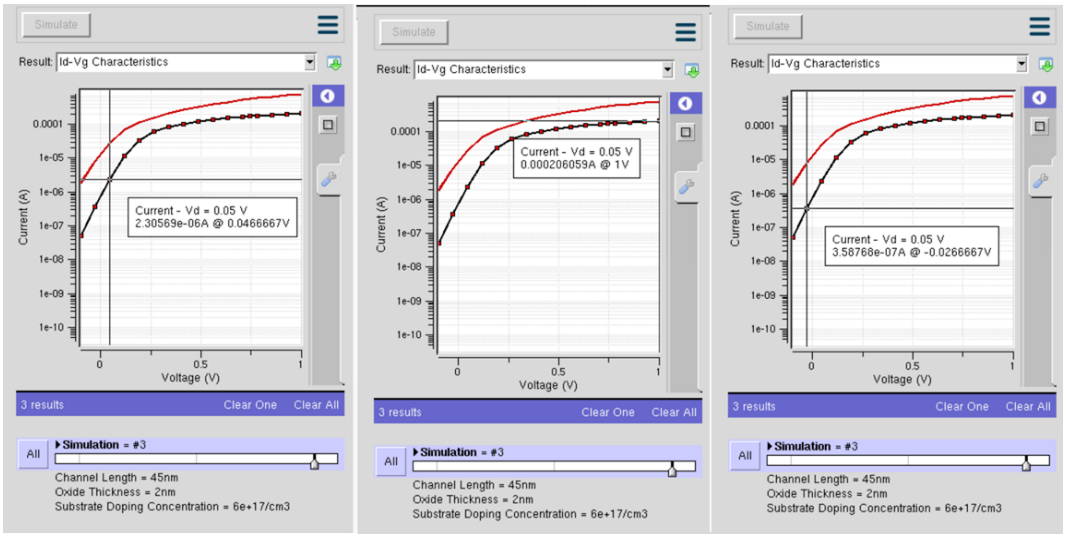

FIGURE 13. - V_{th} =0.046 V; I_{off} = 3.58$e^{-7}A$; I_{on} = 0.206 mA.

- In this paper, we are simulating the MOSFET device structure using an open-source simulator and doing the characterization of the ID-VG and ID-VD curves.
- We have seen that with the advancement of technologies over generations, devices have been scaled down, particularly termed as MOSFET scaling or miniaturization. But apart from the advantages of MOSFET scaling, there are certain limitations also.
- We have learned about some short channel effects like punch through effect and impact ionization.
- In this assignment, we are simulating the n-channel MOSFET device structure for three different generations with the given parameters and obtaining the respective $I-V$ curves and observing their surface charge - V_g characteristics using an online simulator Nanohub.
- From the plot of I_d-V_g Characteristics of the three generations of devices, we can observe that we are simulating the device for both maximum (V_d= 1 V) and minimum (V_d = 0.05 V) voltage biasing. We can see that the performance of the device is better and more accurate when it is biased at maximum voltage biasing i.e., 1 V.
- It can also be noticed in the I_d-V_d characteristics that the current I_D is plotted against the VDS for three particular values of VGS. For saturated device, from the plots, it can be clearly seen that the I_d gap for two consecutive values of V_g is square proportional to the V_g change.
- We are also plotting Surface Charge - V_g Characteristics for both maximum and minimum voltage biasing. The surface charge density for the minimum voltage scaling is more than that for maximum scaling for the same value of V_g.
- From the I_d-V_g characteristics plots of different devices, we are obtaining their electrical properties like V_{th}, I_{on} and I_{off}. The values are not exact as mentioned in the manual, but are nearby values obtained from the plots.

4. CONCLUSION

From the electrical properties obtained, we can conclude that the V_{th} values are decreasing as we are scaling down the MOSFET device more and more. In the third generation of the device, we can notice that the current I_d when V_g is zero is significantly more than the first and second device and hence there is more leakage current. Hence, this is the punch through effect as current is flowing irrespective of the gate voltage (i.e. even gate voltage is zero).

Hence, the third generation of the device is not well designed. By comparing, we can conclude that the first generation of the design is better than the other two generations in terms of performance. Therefore, for the second and third generation, substrate doping can further be increased and oxide thickness further decreased to have better results. However, we also have to take care of the impact of ionization as doping concentration is increasing.

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