The Implementation of an Efficient FPGA-based Digital Controller for Solar Panels

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Abstract

This paper proposes an FPGA-based implementation of a maximum power point tracking (*MPPT*) Controller for solar panels. The proposed architecture is implemented using Field Programmable Gate Array (*FPGA*) technique, with observance of feature desired as flexibility, and speed without performance loss. The design have been written in *VHSIC* Hardware Description Language (*VHDL*) language, that can be used to accelerate the implementation.

FPGA architecture of MPPT is implemented to overcome the large processing time to obtain maximum power for any environmental condition, during moment to moment variations of light level, shading, temperature, and Photovoltaic(Solar) cell array characteristics.

The implementation of the design is achieved using Xilinx Virtex-II platform as a suitable selected programmable device. The development of the system software for this work has been done using Active *HDL 3.5*, and *ISE Navigator 6.3 i* programs. Simulation results demonstrating the validity of the proposed algorithm are also reported.

الخلاصة

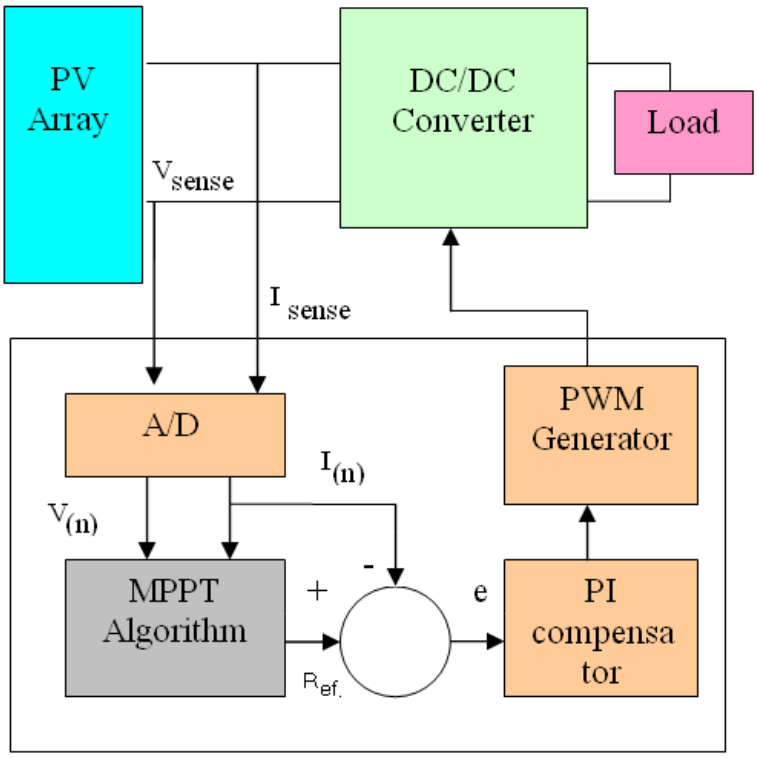
يقترحُ هذه البحث تطبيّقَ معماريه نظام سيطرة لتتبع نقطة القدرة ألقصوى(*MPPT*) مستخدم في الألواح الشمسية. هذه الهندسة المعمارية المقترحة مُطَبَّقة باستعمال تقنية مصفوفة البوابات المبرمجة (*FPGA*)، مَع مراعاة الميزّات المطلوبة كالمرونة، والسرعة بدون خسارةِ في الأداءِ. هذا التَصميم مكتوبِ بلغة (*VHDL*) والتي استعملت لتَعجيل التطبيقَ.

تم تنفيذ الطريقة المقترحة في ظروف بيئية مختلفة شملت الاختلاف في مستوى الضوء من لحظه الى لحظه، الظل ، درجات حرارة مختلفة وكذلك خصائص مختلفة لمصفوفة الخلية الشمسية وقد أثبتت الطريقة اختزلها لوقت المعالجة اللازم للحصول على الطاقة القصوى .

تم تنفيذ التصميم بأستخدام رقاقة المصفوفة البرمجية نوع (*Virtex* II) التي تنتجها شركة (*Xilinx*) كاداة للكيان المادي .في عملية التصميم أستخدامنا برنامج (*Active-HDL* 3.5) في حين تمت عملية محاكاة التنفيذ بأستخدام برنامج *ISE Navigator 6.3i* . وقد أثبتت نتائج المحاكاة صلاحية الطريقة المقترحة.

Introduction

In a Photovoltaic(PV) panels, Maximum Power Point Tracking (MPPT)is the automatic adjustment of electrical load to achieve the greatest possible power harvest. Solar cells have a complex relationship between solar irradiation, temperature and total resistance that produces a non-linear output efficiency known as the "I-V curve"[1]; the purpose of the MPPT system is to sample the output of the cells and apply a load to obtain maximum power for any given environmental conditions.



Figure(1): Equivalent circuit for MPPT

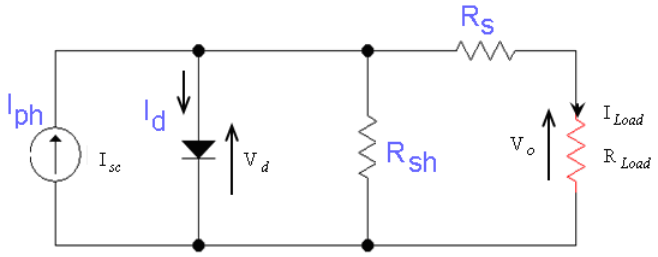
The Power Point Tracker is a high frequency DC to DC converter. They take the DC input from the solar panels, change it to high frequency AC, and convert it back down to a different DC voltage and current to exactly match the panels to the batteries as shown in figure (1).[2]

A solar cell is a non-linear power source and its output power depends on the terminal operating voltage. The Maximum Power Point Tracker (MPPT) tracks the output voltage and current from the solar cell and determines the operating point that will deliver the most power. The proposed MPPT must be able to accurately track the constantly-varying operating point where the maximum power is delivered in order to increase the efficiency of the solar cell.[3]

The control algorithm for extracting maximum power from the cell is proposed by means of the VHDL code and implemented using Xilinx ISE Navigator FPGA Board. FPGA is a programmable logic device considered as an efficient hardware for rapid prototyping.

At the core of this system, the Perturb-and-Observe (P&O) algorithm is used to track the maximum power point. The paper continues as follows: Section I discuses the mathematical model of PV. Section II shows the standard P&O algorithm. In Section III, the implementation and the experimental results are described. In section IV, the discussion is described Finally, conclusions are presented in section V.

Principle Analyzing And Modeling of PV



Figure(2): Equivalent circuit of practical photovoltaic cell

The literature [4-6] proposed various modeling of PV. The output current I and output voltage of PV is given by (1) and (2) using the symbols in Figure(2)[4].

$$I = I_{ph} - I_d - V_d / R_{sh} \quad \text{---------} \quad (1)$$

$$V = V_d - R_s I \quad \text{----------} \quad (2)$$

$$I_d = I_o \left[exp\left(\frac{qV_d}{nkT} \right) - 1 \right] \quad \text{----------} \quad (3)$$

Where I_{ph} is the photocurrent (in amperes), I_o is the reverse saturation current (in amperes), I_d is the average current through diode (in amperes), n is the diode factor, q is the electron charge (in coulombs), $q = 1.6 \times 10^{-19} C$, k is Boltzmann's constant (in joules per Kelvin), $k = 1.38 \times 10^{-23} J/K$, and T is the PV panel temperature (in Kelvin). R_s stands for the intrinsic series resistance of the PV, which is ideally zero. R_{sh} denotes the equivalent shunt resistance of the solar array, which is ideally infinity. In general, the output current of PV is expressed by

$$I = I_{ph} - I_o\left[exp\left\{\frac{q}{nkT}\left(V + R_s I\right)\right\} - 1\right] - \frac{V + R_s I}{R_{sh}} \quad \text{-------- (4)}$$

Where the resistances and Rsh can generally be neglected, and therefore, last term in (4) is generally dropped.

$$I = I_{ph} - I_o\left[exp\left\{\frac{q}{nkT}\left(V + R_s I\right)\right\} - 1\right] \quad \text{------- (5)}$$

When the circuit is opened, the output current $I = 0$,and the open-circuit voltage V_{oc} is expressed by

$$V_{oc} = V_{max} = \frac{nkT}{q} ln\left(\frac{I_{ph}}{I_o} + 1\right) \approx \frac{nkT}{q} ln\left(\frac{I_{ph}}{I_o}\right) \quad \text{--------- (6)}$$

If the circuit is shorted, the output voltage $V = 0$, the average current through diode I_d is generally be neglected, and the short-circuit current $I_{sc} = 1$ is expressed by using (7). The relationship exists between short-circuit current and photocurrent by using (8).

$$I = I_{ph} - \frac{R_s I}{R_{sh}} \quad \text{------- (7)}$$

$$I = I_{sc} = I_{ph} / \left(1 + \frac{R_s}{R_{sh}}\right) \approx I_{ph} \quad \text{------- (8)}$$

Finally , the output power P is expressed by (9)

$$P = IV = \left(I_{ph} - I_d - V_d / R_{sh}\right)V = \left(I_{ph} - I_d\right)V$$

$$= \left(I_{ph} - I_o\left\{exp\left[\frac{q}{nkT}\left(V\right)\right] - 1\right\}\right)V \quad \text{------- (9)}$$

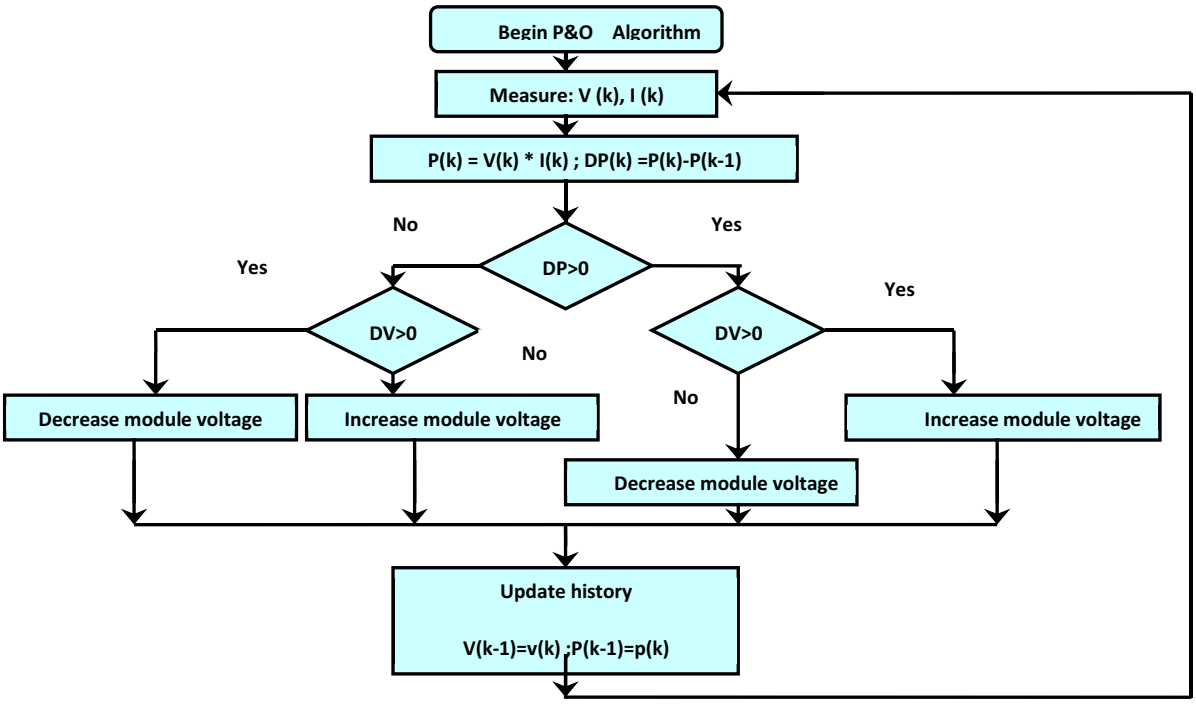
$$P_{max} = I_{ph}\left\{V_{oc} - \frac{nkT}{q} ln\left(1 + \frac{qV_{mppt}}{nkT}\right) - \frac{V_{oc}}{qV_{mppt}\left(nkT\right)} + \left(\frac{nkT}{q}\right)^2 \frac{1}{V_{mppt}} ln\left(1 + \frac{qV_{mppt}}{nkT}\right)\right\} \text{--------(10)}$$

Where : P_{max} and V_{mppt} the maximum output power and optimal output voltage

Here P and are V the instantaneous output power and output voltage of PV, respectively. The steady-state of the Maximum Power Point (MPP) contains $\partial P / \partial V = 0$. The maximum power is expressed by (10).

The Perturb and Observe Algorithm

The classic P&O algorithm is pretty simple [6]. Figure(3) depicts a flow chart explaining it. It operates by perturbing the PV array voltage (i.e. incrementing or decreasing) and comparing the PV output power with that of the previous perturbation cycle. If the perturbation leads to an increase/decrease in array power, the subsequent perturbation is made in the same/opposite direction. In this manner, the peak power is tracked continuously.



Figure(3): Perturb-and-observe algorithm

The operating voltage is perturbed with every MPPT cycle. As soon as the MPP is reached, V will oscillate around the ideal operating voltage V_{mpp}. Figure(1 and 4) and Table(1) summarized the control action of the P&O method. The value of the reference voltage,V_{ref}, will be changed according to the current operating point. For example, when the controller senses that the power from solar array increases $(\partial P \rangle 0)$and voltage decreases $(\partial V \langle 0)$, it will decrease (-) V_{ref} by a step size ***C***, so V_{ref} is closer to the MPP. The MPP represents the point where V_{ref} and scaled down V_{sense} become equal.

Table (1) : perturb & observe control action

Case	∂P	(∂V or ∂I)	Control action
1	<0	<0	Increase (V or I)
2	<0	>0	Decrease(V or I)
3	>0	<0	Decrease (V or I)
4	>0	>0	Increase (V or I)

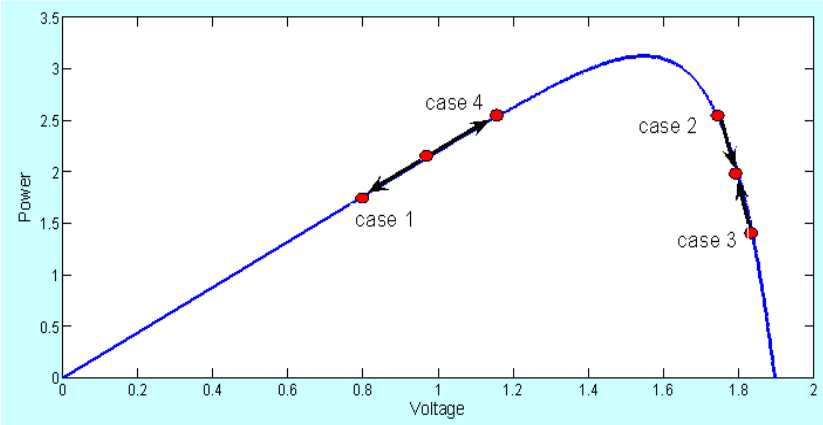


Figure (4): Plot of power versus voltage for the simulated PV.

MPPT Hardware Implementation

The P&O algorithm resides on the MPPT controller[7]. This controller receives values for voltage and current, calculates all the necessary differentials and performs updates to V_{ref} after the necessary error checking has been performed. Also, it stores the power, voltage, and current values from the previous iteration. In addition, the MPPT algorithm also detects whether the system is operating in Output Voltage Regulation or MPPT. In case, the present output voltage of the array will exceed V_{ref} by a pre-determined threshold C_{OVR}. When this condition, called Output Voltage Regulation (V_{OVR}). OVR detection is enabled when the difference between the system voltage and V_{ref} exceeds a certain threshold.

Figure (5) It has input ports named $i_{\_sence}$ and $v_{\_sence}$, which receive data from PV array to the MPPT chip, Some signal in MPPT block are used as control signal which are clk(clock), $V_{\_out}$, and one output port V_{avr} named The MPPT controller block are implemented using VHDL code in a structural form. The structural codes of the block MPPT is shown in Figure (6) .

Figure ((5) a , b) illustrates hierarchy block diagram of MPPT controller.

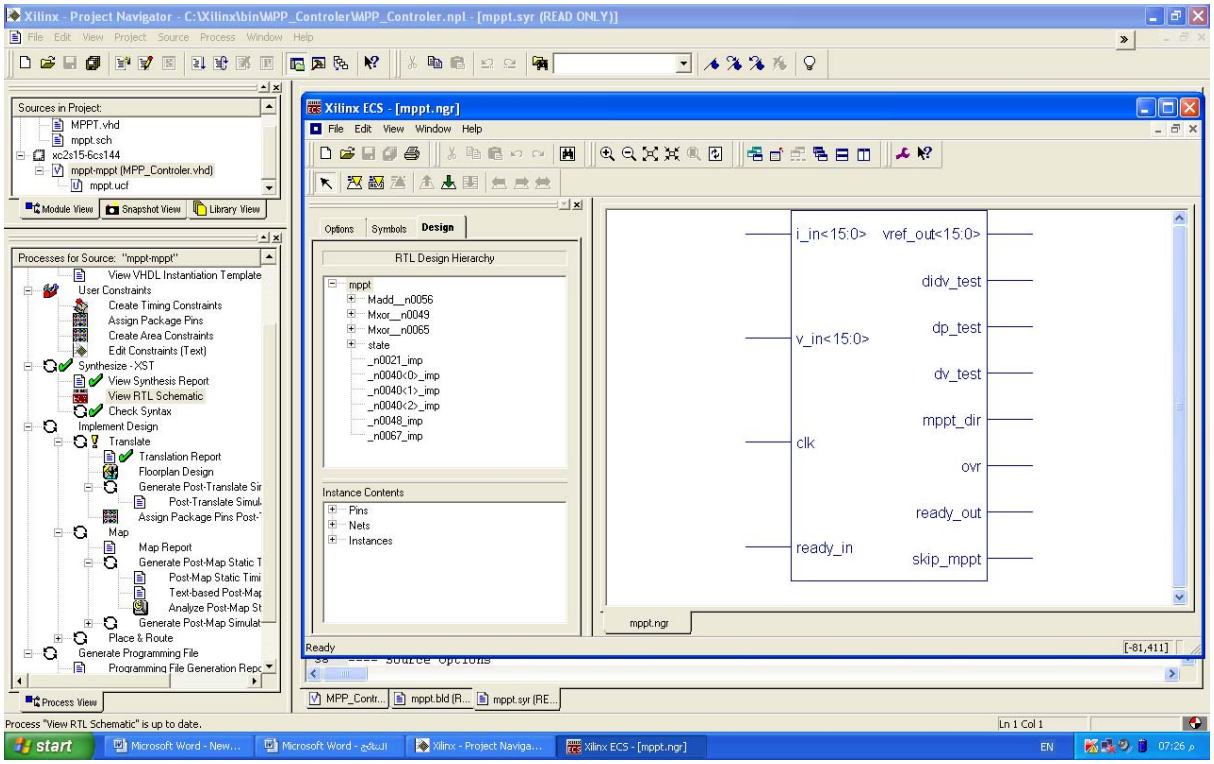


Figure (5-a): The MPPT controller block.

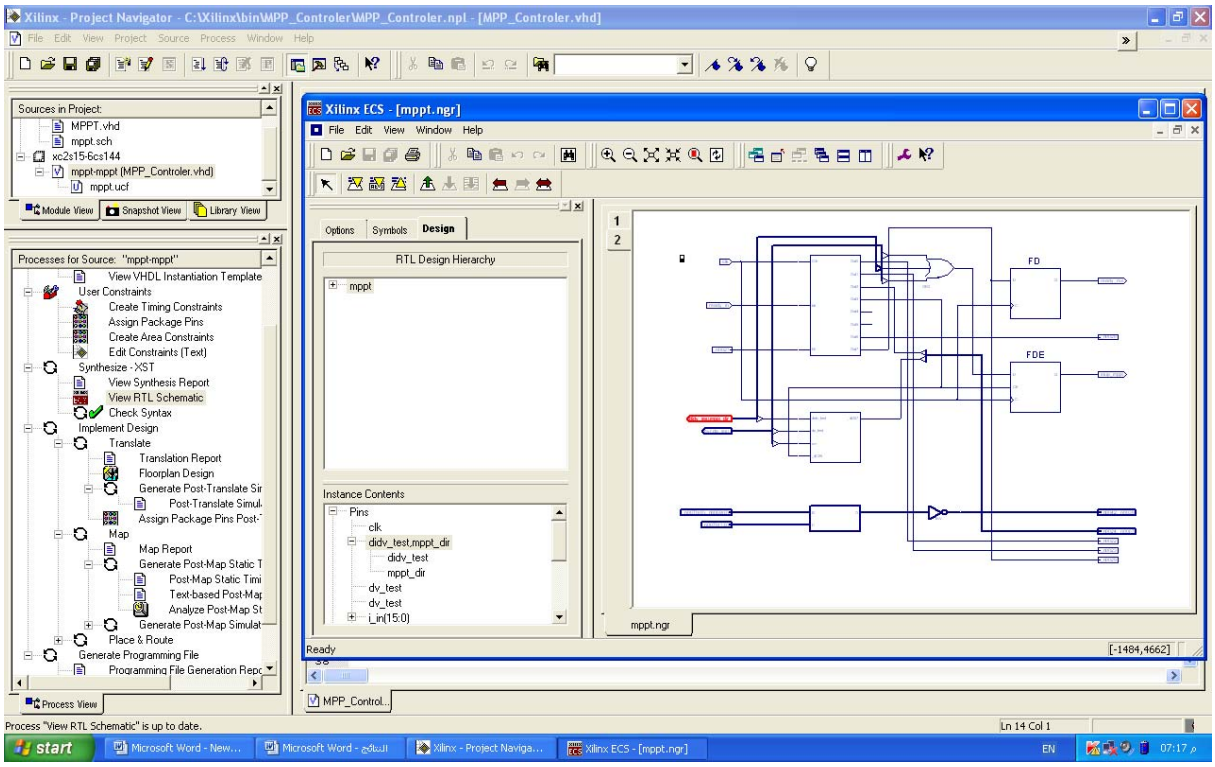


Figure (5-b): The MPPT controller block.

Figure ((6) a , b) illustrates structural codes of MPPT controller.

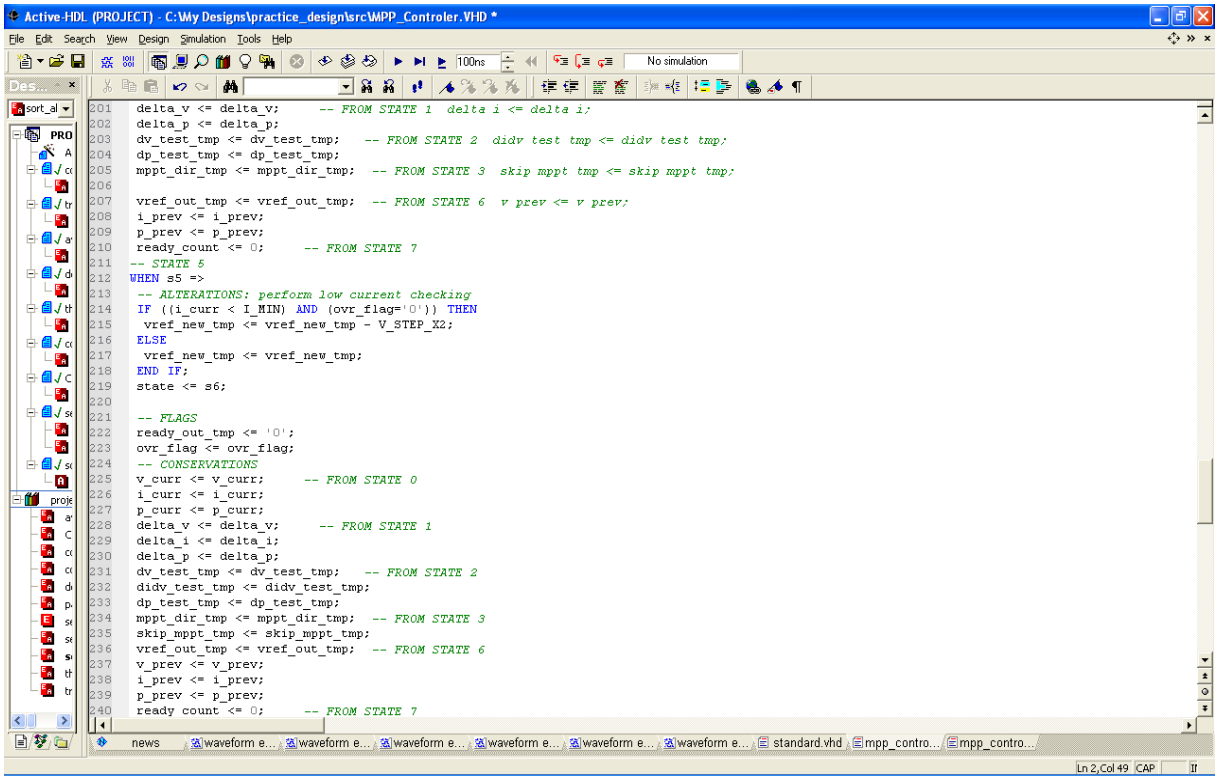


Figure (6-a) :The MPPT controller block.

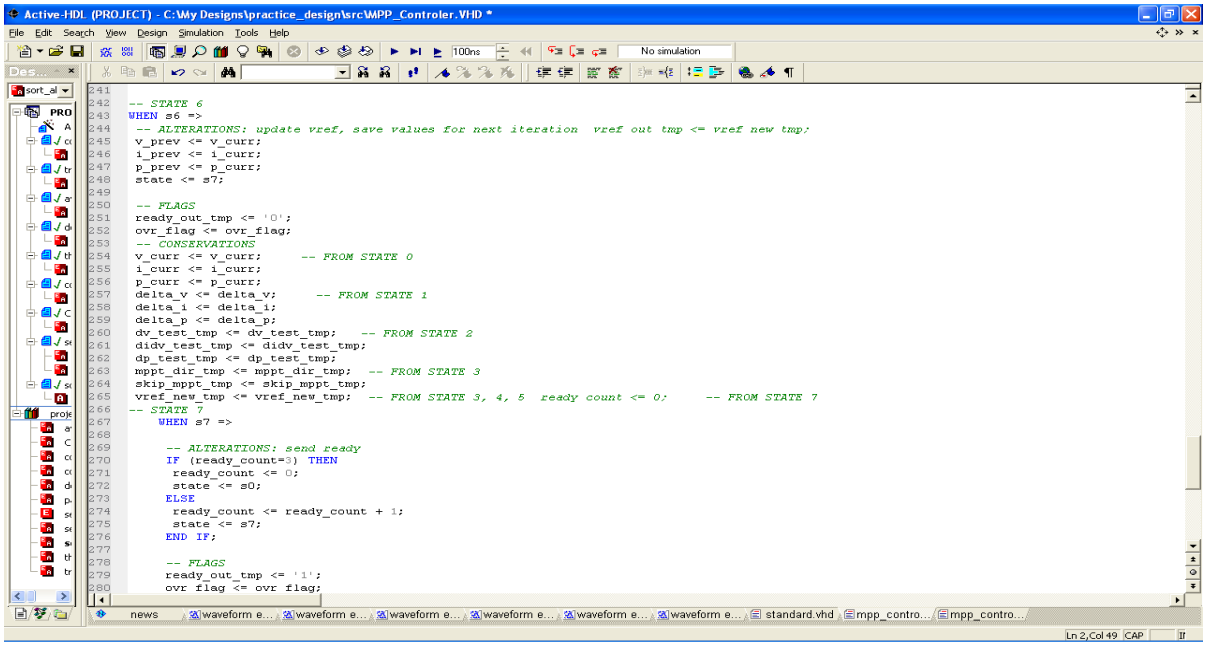


Figure (6-b): The MPPT controller block.

Simulation Results

Figure (7) illustrates the simulation Results of the MPPT controller, the functional simulation of the proposed design is done through using Active-HDL software tool, After running the simulator, it gives the waveform results. The unit responsible for making the decisions regarding tracking. For each clock cycle that is high, the voltage and current are read, and the differentials are processed in order to make decisions about whether or not to track, and in what direction. The signals V_{OVR} are internal flags based upon each calculation and provide information about the decisions made by the algorithm. The modified V_{ref} is sent out on V_{avr}.

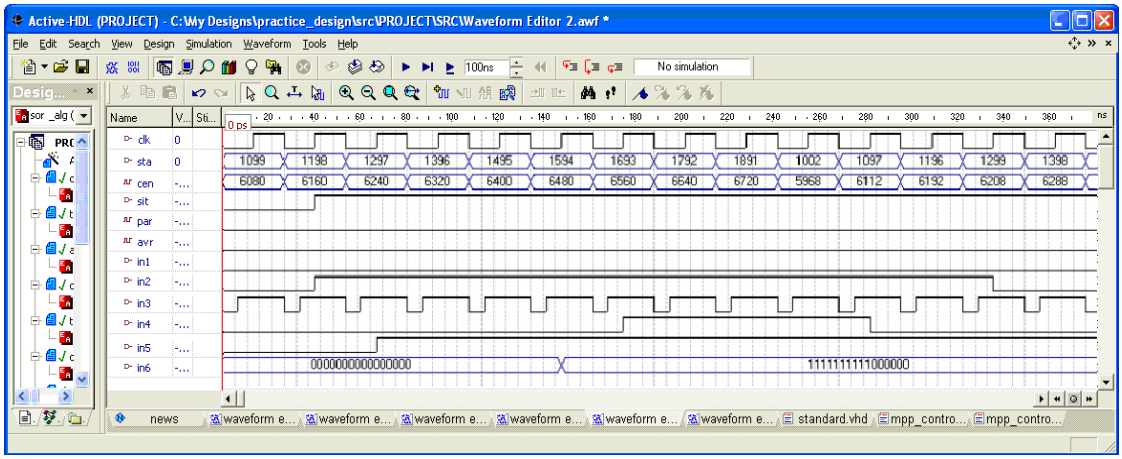


Figure (7): Simulation results of MPPT controller.

Discussion

To increase the output efficiency of a photovoltaic (PV) generation system it is important to have an efficient maximum power point tracking (MPPT) technique.the proposed approach can effectively improve the tracking speed and accuracy simultaneously.

Designing the MPPT controller in this way is guided by the idea of getting the best speed/cost ratio that results from using the piplining approach. This is to ensure that all stages work synchronously, and that these stages give their intended results on the next clock.

The proposed hardware architecture provides a high throughput for digital signal processing(DSP) with low hardware resource utilization. The processing time obtained for the DSP implementation was about 420 milliseconds. The reported execution time was obtained considering data is already available in the input memory. The architecture performance is over 20 times faster than the required rotation rate[8].

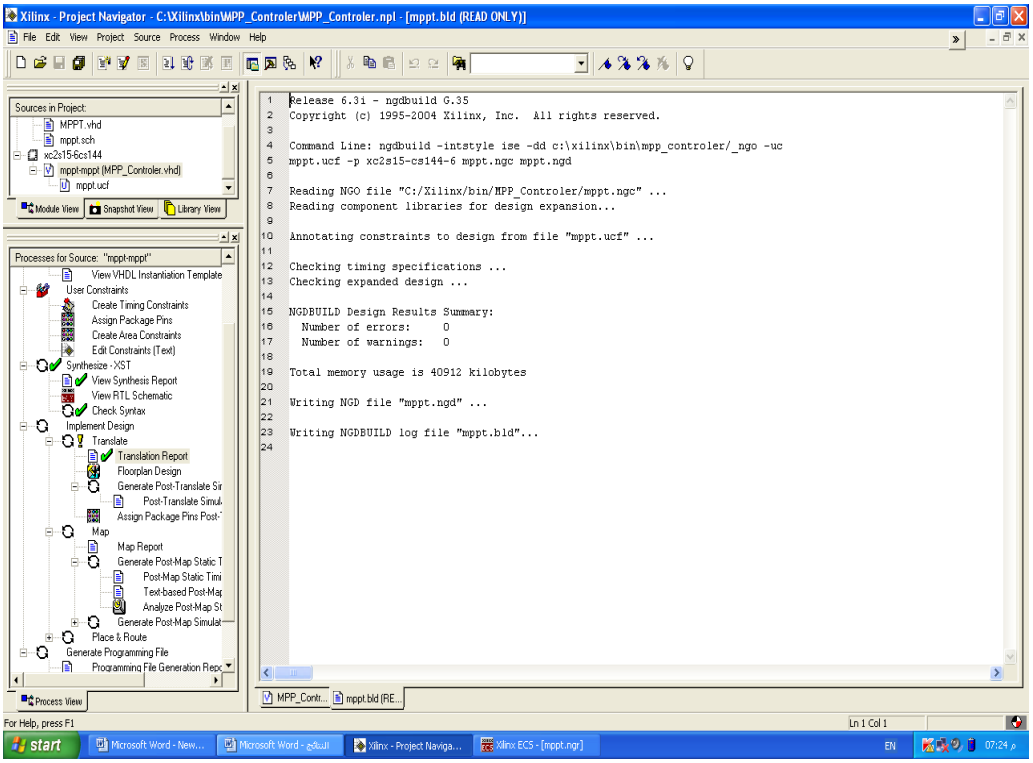


Figure (6):Translation Report of the Proposed Design

The proposed architecture was modeled using the VHDL Hardware Description Language and synthesized with Xilinx ISE Navigator 6.3i targeted for a Xc2s15-6-cs144-6 Virtex-II device.

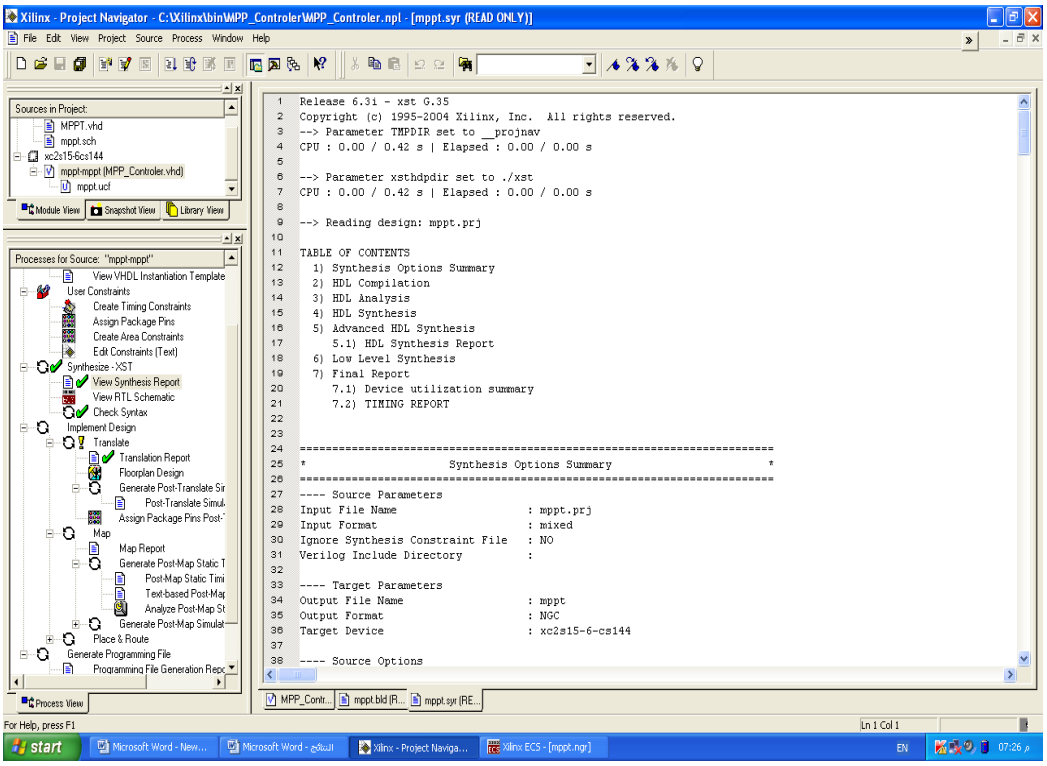


Figure (7): Place and Route Report of the Proposed Design

This FPGA chip is chosen According to its architecture, which is optimal for high density and high performance logic design. According to the repots obtained from the implementation process, the Number of Slices is 260 ;the number of 4-input LUTs is 355; the number of Flip Flops is 182; FPGA Occupation percentage 56%.The maximum operating frequency is 151.172 MHz .

Device Utilization Summary:

Selected Device : 2s15cs144-6

Number of Slices:	260	out of	192	135% (*)
Number of Slice Flip Flops:	182	out of	384	47%
Number of 4 input LUTs:	355	out of	384	92%
Number of bonded IOBs:	56	out of	90	62%
Number of GCLKs:	1	out of	4	25%

Timing Summary:

Speed Grade: -6

Minimum period: 6.615ns (Maximum Frequency: 151.172MHz)

Minimum input arrival time before clock: 15.482ns

Maximum output required time after clock: 7.085ns

Conclusions

In this work an efficient hardware implementation of a (MPPT) was presented. The high performance of the proposed architecture was feasible since the employment of a parallel processing model provided by FPGAs. The use of this technology is suitable because it offers high flexibility in modifying and even developing the required design with a reduction in the required number of hardware and cost.

In addition to the main features of the processing chain architectures such as degree of parallelism, small size, accuracy and high computational speed, there is a requirement for generality and adaptively i.e. the ability to handle many different models of operation in different environments. Integrating FPGA in an MPPT control system provides numerous advantages. To meet performance requirements, FPGAs are desirable since their performance can easily surpass the performance of microcontrollers and DSPs. because their high logic capacity, FPGAs can be adapted to control MPPT by employment of a parallel processing model. In addition, given their reprogrammability, FPGAs can be used to conduct in-circuit experimentation, testing and optimization of various parameters that affect the performance of the MPPT control system.

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