Low Complexity Spectrum Sensing System for GFDM Cognitive Radio Signals

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ABSTRACT:

Cognitive radio is a promising technology that aims to use the transmission spectrum efficiently. Each cognitive transmission process consists typically of two phases. During the first phase, which is called sensing phase, cognitive system attempts to detect an available spectrum hole. While in the second phase, data transmission phase, the secondary user data is transmitted to the destination via detected hole. The throughput of the cognitive radio system is mainly depending on the ratio of the transmission time to the sensing time. To reduce the sensing time, this paper suggests a design of simple spectrum sensing system capable for detecting Generalized Frequency Division Multiplexing (GFDM) signals. The reduction in sensing time is based on using XilinixVirtix-6 Field Programmable Gate Array (FPGA) as a target device for implementation the proposed design, which operates at 600 MHz clock frequency. This work includes a discussion of more than one approach to reduce the arithmetic operations needed to implement a sensing system with 250 subcarriers. The simulation results show that the power consumption represents the main challenge of such implementation.

Keywords: Cognitive Radio, OFDM, FPGA, GFDM, Spectrum Sensing.

منظومة تحسس النطاق الاقل تعقيدا لـ GFDM لادراك الاشارة الراديوية

الخلاصة

تقنية (CR)هي تقنية واعدة تهدف إلى استخدام النطاق الترددي بكفاءة. تتكون أية عملية إرسال قياسيا من طورين: خلال الطور الأول - والذي يطلق عليه طور التحسس – تحاول المنظومة كشف أية فجوة ممكنة في النطاق الترددي, بينما في الطور الثاني (طور إرسال البيانات) ترسل البيانات إلى الوصول عبر تلك الفجوة. تعتمد كفاءة المنظومة أساسا على نسبة زمن الإرسال إلى زمن التحسس. و لأجل تقليل زمن التحسس, يقترح هذا البحث تصميم بسيط لمنظومة تحسس للنطاق الترددي لها القابلية على كشف إشارات (GFDM). إن تقليل زمن التحسس تم بناءا على استخدام تقنية (Xilinix Virtix-6 FPGA) لتنفيذ التصميم المقترح, والتي تعمل بتردد ساعة يصل إلى (600 MHz). تضمن العمل مناقشة لأكثر من مقاربة لتقليل العمليات الحسابية المطلوبة لبناء منظومة تحسس (250) حامل ثانوي. أثبتت نتائج المحاكاة أن الطاقة المصروفة تمثل التحدي الأكبر لبناء المنظومة.

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INTRODUCTION

A highly flexible OFDM system is considered for the cognitive radio baseband system where individual carriers can be switched off for frequencies which are occupied by a licensed user. Inverse Fast Fourier Transform (IFFT) is used to generate OFDM symbols to preserve orthogonality between the subcarriers. However, phase errors caused by residual carrier frequency offset and non-ideal sampling frequency represent the main challenges of making OFDM as a strong candidate for cognitive radio implementations [1,2]. Alternatively, multi-band generalized frequency division multiplexing (GFDM) is relatively new idea for designing a multicarrier physical layer. GFDM is well suited for cognitive radio as the choice of the pulse shaping filters makes the out-band leakage extremely small as compared to the OFDM [3]. To protect opportunistic users, GFDM signals need to be sensed reliably, so that any other secondary signal is not transmitted in the occupied band. Much research has focused on spectrum sensing systems. A summary of spectrum sensing algorithms were introduced in [4]. Hwang et al. [5] reported on sensing OFDM signals based on the energy detector. They showed that such type needs high signal to noise ratio to sense the spectrum properly. Work in [6] introduced a proposed technique to reduce the hardware complexity of the cyclostationary spectrum sensing system to nearly 30% of the traditional type. Panaitopol et al. [7] also presented cyclostationary detector for cognitive radio using GFDM modulation.

In general, GFDM systems have been a relatively difficult functions to implement in hardware. This leads many designers to use digital signal processors for such purpose. However, the nature of parallel architecture of multicarrier systems requires multiple digital signal processors. This is costly as well as power intensive [8]. With the rapid development of microelectronic technology, recent types of FPGA offer lower power, better reliability and built in digital signal processors [9]. In this paper, GFDM spectrum sensing system is designed for FPGA implementation. The challenges of power consumption, hardware complexity and parallel processing reliability are included in this work. The paper is organized as follows. In section II, GFDM system model is presented. A design of the GFDM spectrum sensing system is proposed in section III. Section IV evaluates the design complexity, solutions of fitting problems and the effect of frequency on the whole design. The last section concludes the work.

Generalized Frequency Division Multiplexing

In OFDM, each subcarrier is shaped with a rectangular pulse. Therefore, the side lobes of the corresponding frequency domain ($\frac{\sin(x)}{x}$) decay slowly and it is necessary to introduce additional filters to improve the spectral properties. This filtering can cause additional intersymbol interference which degrades the performance. While GFDM with root raised cosine (RRC) transmits a shaped pulse causes lesser interference to the adjacent pulse in the frequency band. Figure.1 shows the block diagram of the GFDM transmitter [3,10].

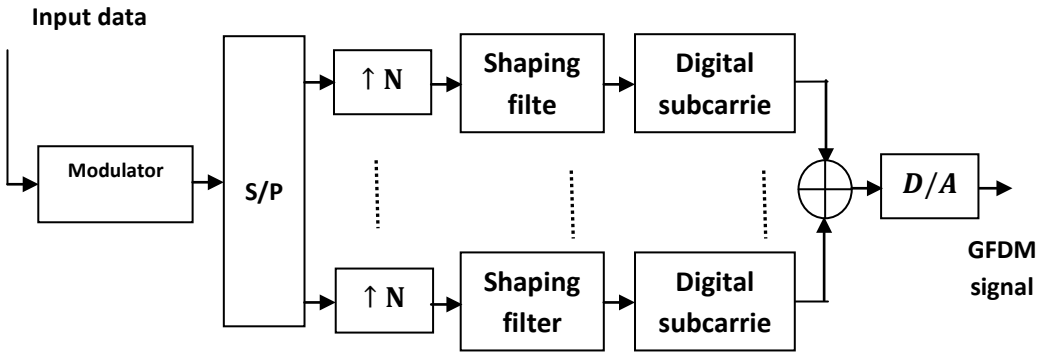


Figure (1) GFDM transmitter model.

The binary input data is firstly modulated and then arranged in two-dimensional form called block structure (**D**). This form consists of M subcarriers and K time slots and may be defined as [3];

$$\boldsymbol{D} = \begin{bmatrix} \boldsymbol{d_0(0)} & \cdots & \boldsymbol{d_0(K-1)} \\ \vdots & \ddots & \vdots \\ \boldsymbol{d_{M-1}(0)} & \cdots & \boldsymbol{d_{M-1}(K-1)} \end{bmatrix} \quad \ldots (\mathbf{1})$$

where the complex data $d_m(k)$ is the data symbol transmitted on the m^{th}subcarrier and in the k^{th} time slot. For each subcarrier branch, the complex data symbols are up sampled by a factor N, which is normally grater than the number of subcarriers, resulting in;

$$d_m^N(n) = \sum_{k=0}^{K-1} d_m(k)\,\delta(n-kN), \qquad n = 0,1,\ldots\ldots,NK-1 \qquad \ldots \quad (2)$$

where δ(.) is the dirac delta function. After that, this sequence is passed through a pulse shaping filter $h[n]$ followed by digital subcarrier $e^{j\frac{2\pi}{N}mn}$. The resulting subcarrier signal can be expressed as;

$$s_m[n] = (d_m^N[n] \ * \ h[n])\, e^{j\frac{2\pi}{N}mn} \qquad \ldots (3)$$

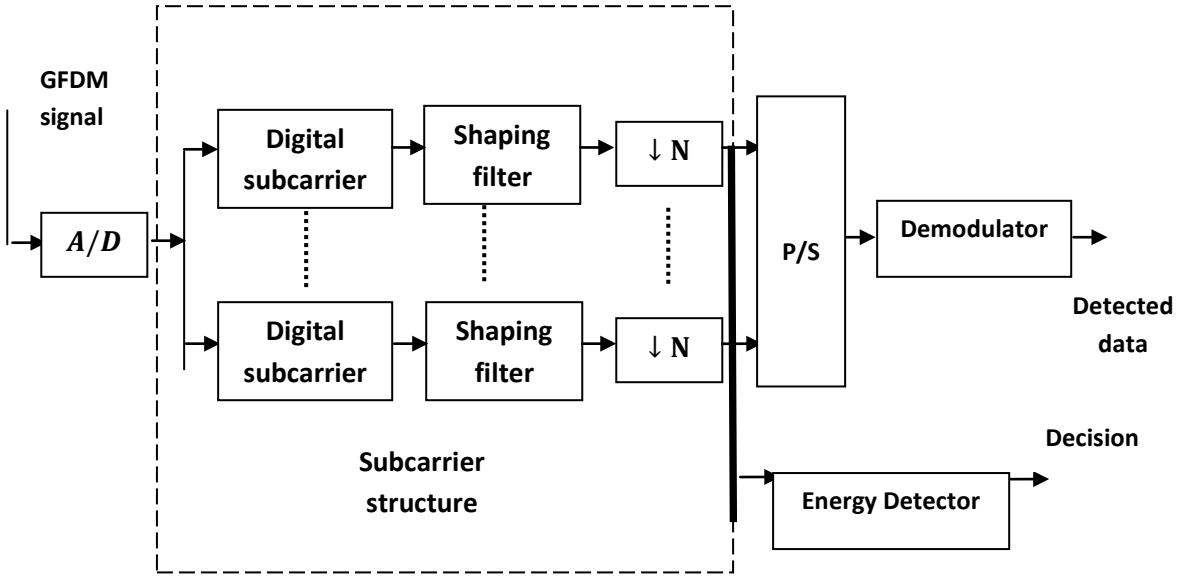
where * denotes circular convolution.

This leads to a total of (NK) samples per subcarrier, which may be expressed in block structure as;

$$\boldsymbol{S} = \begin{bmatrix} \boldsymbol{s_0(0)} & \cdots & \boldsymbol{s_0(NK-1)} \\ \vdots & \ddots & \vdots \\ \boldsymbol{s_{M-1}(0)} & \cdots & \boldsymbol{s_{M-1}(NK-1)} \end{bmatrix} \quad \ldots (\mathbf{4})$$

The sum of all subcarrier branches is then passed through a suitable digital to analogue convertor and then sent over the channel.

Figure(2) shows the block diagram of GFDM receiver [3]. The main parts of such receiver are analogue to digital convertor, subcarrier structure, energy detector, parallel to serial data convertor and demodulator. In this work, it is necessary to concentrate the analysis toward the spectrum sensing system, which consists of two parts; the subcarrier structure and the energy detector.



Figure(2) GFDM receiver model.

a. Subcarrier structure

After the Analogue to digital convertor, the received data vectors are down-converted by multiplying it with ($e^{j\frac{-2\pi}{N}mn}$) to form a subcarrier received vector [3];

$$r_m[n] = y[n] \cdot e^{\frac{-j2\pi mn}{N}} \quad \dots (5)$$

This vector is then passed through a receiver matched filter $g[n]$. The resulting vector may be denoted by $\bar{d}_k^N[n]$ and described as;

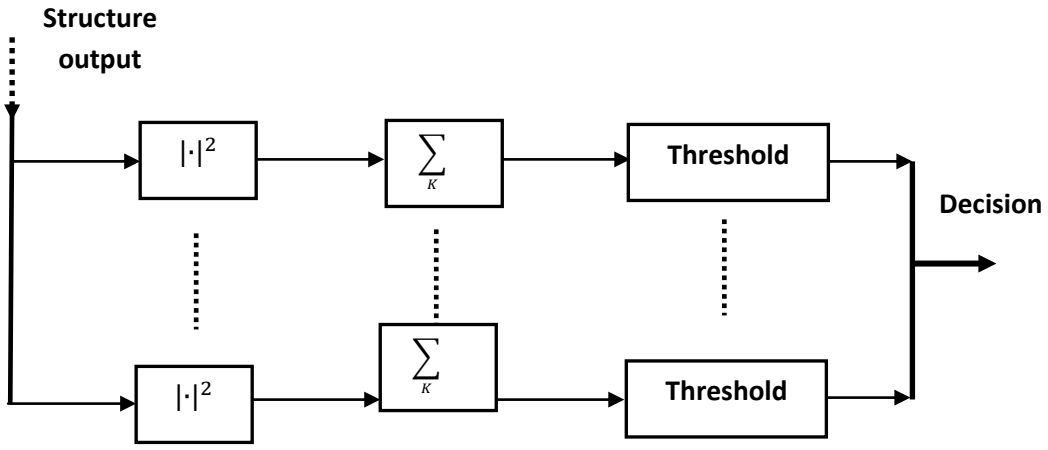
$$\bar{d}_k^N[n] = r_m[n] * g[n] \quad \dots(6)$$

Finally, the required data vector is obtained by down sampling the vector described in (eq.6) above by a factor of N;

$$\tilde{d}_k^N[m] = \bar{d}_k^N[n = mN] \quad \dots (7)$$

b. Energy detector

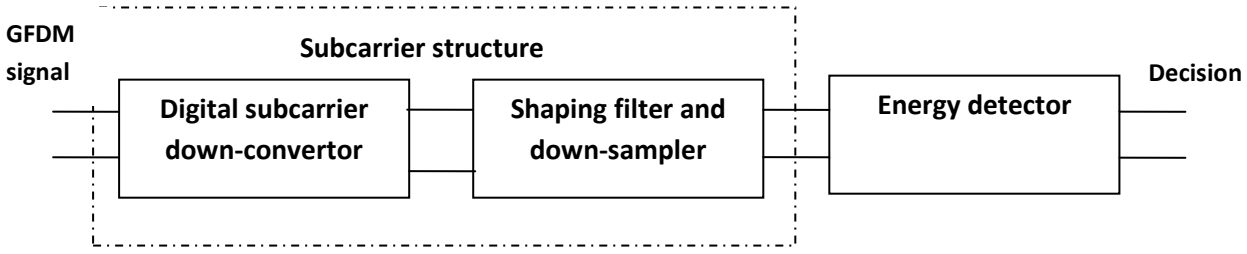
Fig.3 shows the block diagram of simple energy detector [3,10]. The received vector $\tilde{d}_k^N[n]$ (eq.7) is firstly passed through a square law device and then a summer adds up the energy value of the subcarrier samples. The resulted value is compared with a threshold to decide whether the subcarrier band is occupied or empty.



Figure(3) Block diagram of energy detector.

I. Design of the spectrum sensing system

In this section, a design of spectrum sensing system is proposed. The suggested structure consists of three stages as shown in fig.4 below;

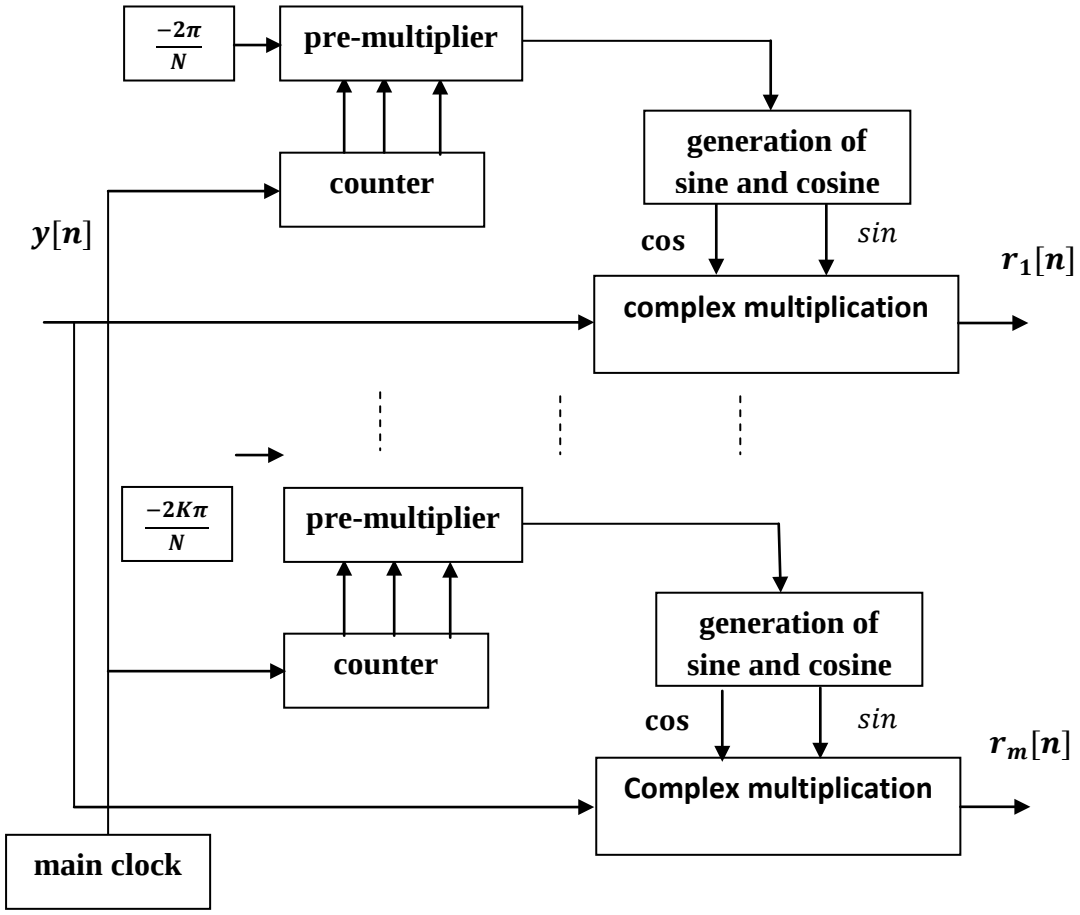


Figure(4) Design stages of the proposed spectrum sensing system.

The first stage is merely a digital subcarrier down-convertor. The main core of this part is the complex multiplication of the received vector ($y[n]$ in eq.5) with ($e^{\frac{-j2\pi mn}{N}}$). There are two approaches to perform the complex multiplication. According to the first approach, the real and imaginary parts of ($e^{\frac{-j2\pi mn}{N}}$) are precalculated and stored in a certain memory for each value of n and . These values are then loaded and multiplied with the real and imaginary parts of the vector $y[n]$.

However, in this paper and due to parallel processing requirement of the subcarrier structure, an approach shown in Fig.5 is considered. In this approach and for each subcarrier m, a constant value of ($\frac{-2\pi m}{N}$) is pre-multiplied by the output of ($log_2 N -$ counter). At each instant, the counter output is equal to the value of n. The result of pre-multiplier generates the real and imaginary values of ($e^{\frac{-j2\pi nm}{N}}$) using cosine and sine series respectively. These two values are then multiplied with the real and imaginary parts of the vector $y[n]$. According to this approach, the number of

arithmetic operations and logic elements needed to implement one subcarrier of this stage are calculated as in Table.1.

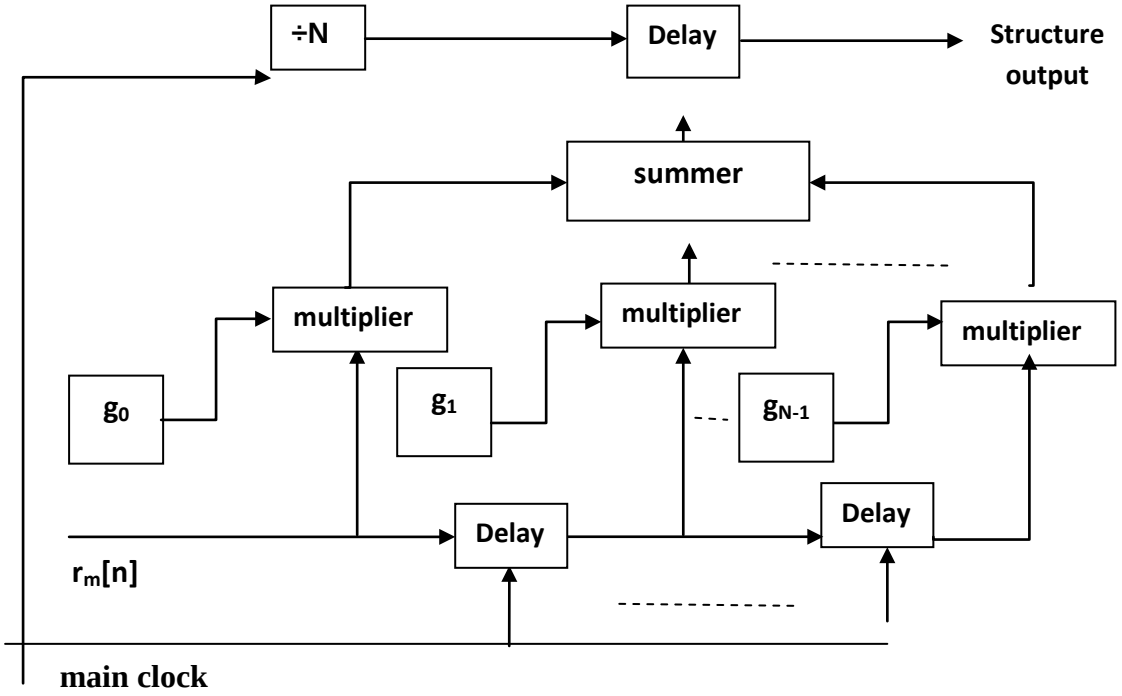


Figure(5) Design of digital subcarrier down convertor (first stage).

Table(1) number of arithmetic operations and logic elements required for first stage.

operation	Description	Total
Multiplication	(4) for complex multiplication, (12) for sine and cosine series generation and (1) pre-multiplier	17
Addition	(2) for complex multiplication and (6) for sine and cosine generation	8
Logic elements	(log_2N − counter)	1

The second stage includes two operations. The first is a convolution of the output of digital down-convertor with N-coefficient shaping filter. While the second one is the down sapling operation. The symbol $(\div N)$ is merely $(log_2 N)$- bit counter. When the output bits of this counter are all 1's, the last delay block is clocked to form the stage output. Fig.6 shows such design and Table.2 includes the number of arithmetic operations and logic elements per subcarrier needed to implement this stage.



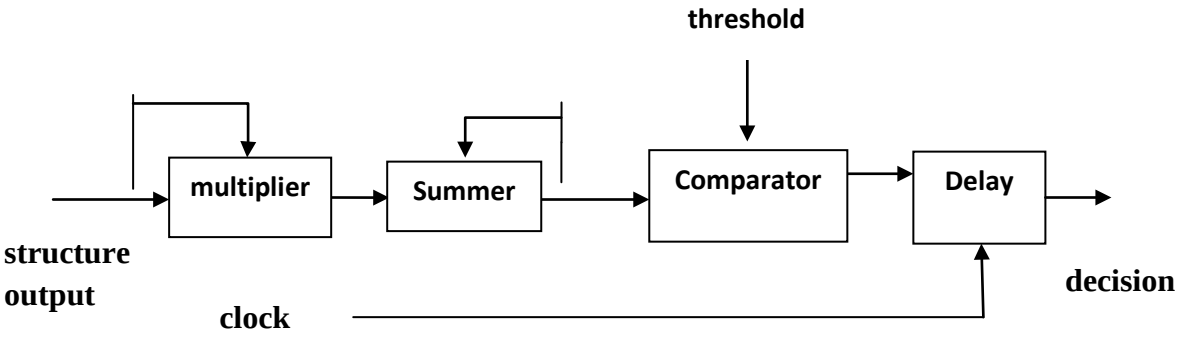
Figure(6) Design of second stage of spectrum sensing system.

Table(2) number of arithmetic operations per subcarrier needed to implement the second stage.

operation	Description	Total
Multiplication	**(4) complex multiplication for each coefficient**	**4N**
Addition	**(2) for complex multiplication with each coefficient and (N-1) for real and imaginary summer**	**4N-2**
Logic elements	**$(log_2 N -$ counter)**	**1**
	(N) D/FF for convolution and (1) for final delay	**N+1**

The final stage in the design of spectrum sensing system is the energy detector. For each subcarrier, the total energy of the shaping filter output is compared with a certain threshold to make right decision if there is a primary signal in the licensed

spectrum or not. Fig.7 shows the design of the detector and Table.3 includes the required number of arithmetic operations and logic elements to perform this stage.



Figure(7) Design of the third stage of spectrum sensing system.

Table(3) number of arithmetic operation and logic elements needed for the third stage.

Operation	Description	Total
Multiplication	(4) complex multiplication	4
Addition	(2+2K) the first two for complex multiplication	2K+2
Logic elements	Comparator	1
	(1) delay	1

In this paper, the design specifications (clock frequency, number of subcarriers, number of samples and number of time slots) are assumed to have values as in Table.4.

Table(4) Design specifications.

Clock frequency	Number of subcarriers M	Number of samples N	Number of time slots K
600 MHz	250	512	15

According to the number of operations and logic elements required for each stage and the value of (N) in Table.4, the total number of arithmetic operations and logic elements needed to implement the three stages of the sensing system are shown in Table(5).

Table (5) Total number of arithmetic operations and logic elements needed for the spectrum sensing system.

Stage	Multiplications	Additions	Logic elements
First	17	8	9 bit counter
Second	2048	1022	513 D/FF and 9 bit counter
Third	4	32	Comparator and D/FF
Total	2069	1062	2 counters, 514 D/FF and comparator

Implementation of the designed system

To implement the design described in the previous section, Xilinix Virtex-6 FPGA is suggested as a target device. The Virtex-6 family provides the most advanced features in the FPGA market. One of these features is the existence of embedded Digital Signal Processing blocks (DSP48E1). Each DSP slice contains a 25×18 bits multiplier, an adder and accumulator. In addition to that, each Configurable Logic Block (CLB) contains four LUTs and eight flip-flops. Block RAMs are also included in the device. A feature summery of four different types of is family is included in Table.6 [12].

Table(6) Feature summery of the four target devices.

Device	CLB Slices	DSP48E1 Slices	Block RAMs	Max. User I/O pins
XC6VLX75T	11640	288	5616	360
XC6VLX365T	56880	576	14976	720
XC6VSX475T	74400	2016	38304	840
XC6VLX760	118560	864	25920	1200

AVHDL code was written to describe the proposed spectrum sensing system as a design entry and then a software called ModelSim is used to estimate the power consumption for the design. For implementation to be possible, the following restrictions must be taken in our consideration:-

a. The total number of multiplication operations needed to implement the system is 2069 operations (Table.5), while the maximum number of DSP48E1 multipliers is in device XC6VSX475T (Table.6) is 2016. That means no ability to implement the proposed system in order to sense one subcarrier using this family.
b. Table.6 shows that the maximum user number of I/O bits for the same device in (point a) is 840. On the other hand the number of bits required to implement 250 subcarrier with 8-bit input and 1-bit output complex data is $(250 \times (8_{bits/input} + 1_{bits/output}) \times 2_{real+imag} = 4500)$ bits, which means a real problem to be solved.
c. It is necessary to choose a device which requires minimum value of power. In this paper, two approaches are suggested to solve the problem in point a:-

Approach 1: Due to the large number of CLB slices and Block RAMs included in the target device (Table.6), one can implement the required number of multipliers using either the conventional method (shift and add operations) or a multiplexer is used to perform the equivalent operation without actual multiplication. In the multiplexer method, all the expected results of multiplication are saved in LUTs, and then the input samples and the coefficients are used to address the required result. However, it is expected that these two methods intensive power. Fig.8 shows the estimate of the required power for these two methods with different values of samples N.

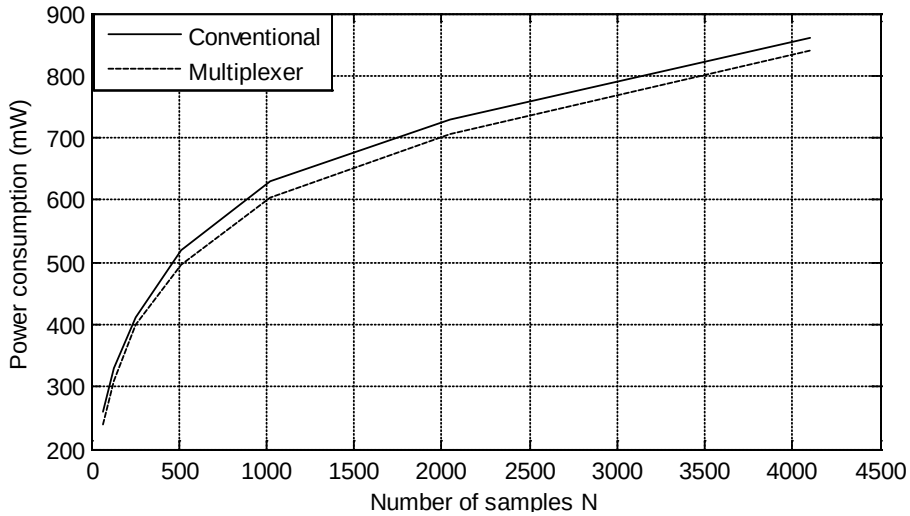
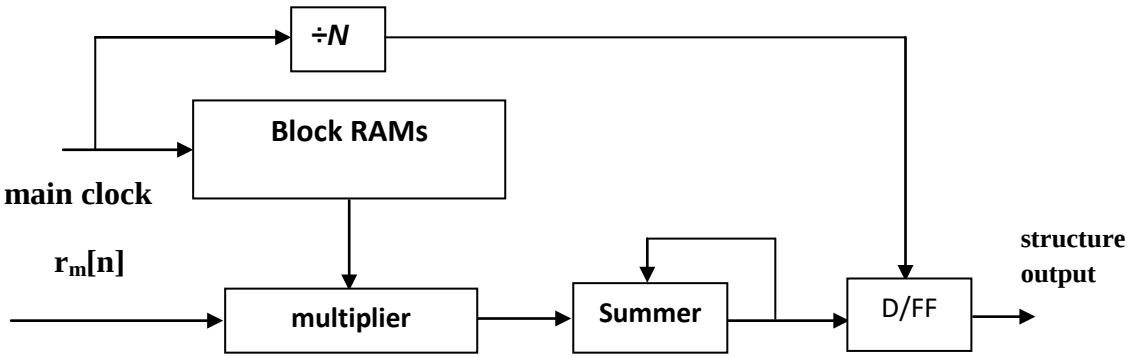


Figure (8) Power consumption for the conventional and multiplexer methods of approach (1).

One can conclude that the two methods of this approach are not suitable for implementation as a result of large values of power consumption.

Approach 2: From Table.5, it is clearly appeared that the number of arithmetic operation of the second stage represents nearly 97% of the total operations needed to implement the whole system. Therefore, it is necessary to redesign this stage in order to fit the required design in the target device. The idea behind this approach is to save the coefficients of the receiver shaping filter in the Block RAMs of the target device and with the raising edge of the main clock, these coefficients are loaded for multiplication with the complex input data. The result of complex multiplication is then summed with former value and so on until the end of N^{th}multiplication of the filter. The number of arithmetic operations per subcarrier needed within this approach reduces to four multiplications and three additions. Such approach may be called serial approach. Figure(9) shows the design for serial approach.



Figure(9) The design of second stage (serial approach).

As a result, the total number of arithmetic operations needed for the whole design is much less than the number of DSP multipliers included in any of the target devices in Table.5. The simulation results show another advantage of this approach, the power consumption is much less than that of the two methods of Approach 1. This is due to the small number of internal logic transition of Approach 2. Fig.10 shows the power consumption of this approach as compared with the multiplexer method of approach 1.

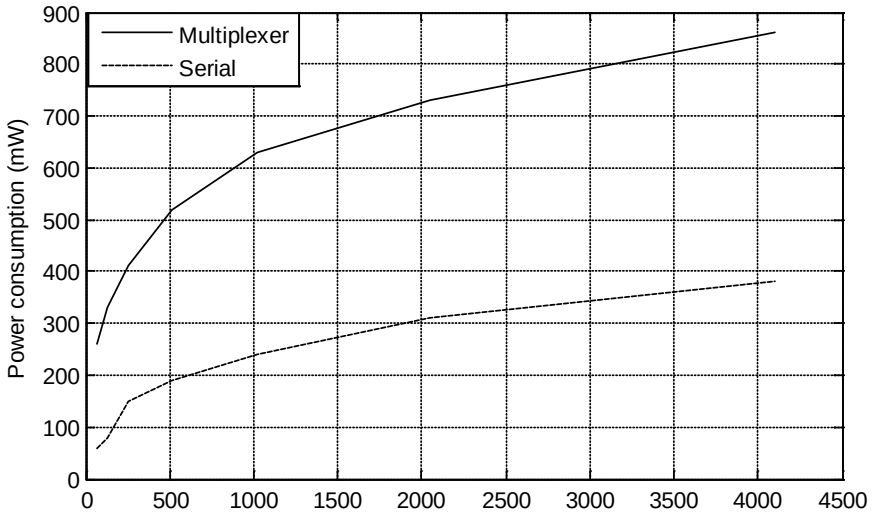


Figure (10) Power consumption for the multiplexer and serial methods.

To reduce the effect of the restrictions in points (b and c) and for any parallel processing system (such as the subcarrier structure of the spectrum sensing system), it is difficult to implement the system in single chip. That is due to restricted number of input/ output pins (bits) of the FPGA device. However, there is no connection between slices used to implement these subcarriers and so it is possible to use more than one device to perform the parallel system. From Table.6 and for 4500 pins (point b), the required number of devices is calculated by dividing the total number of the

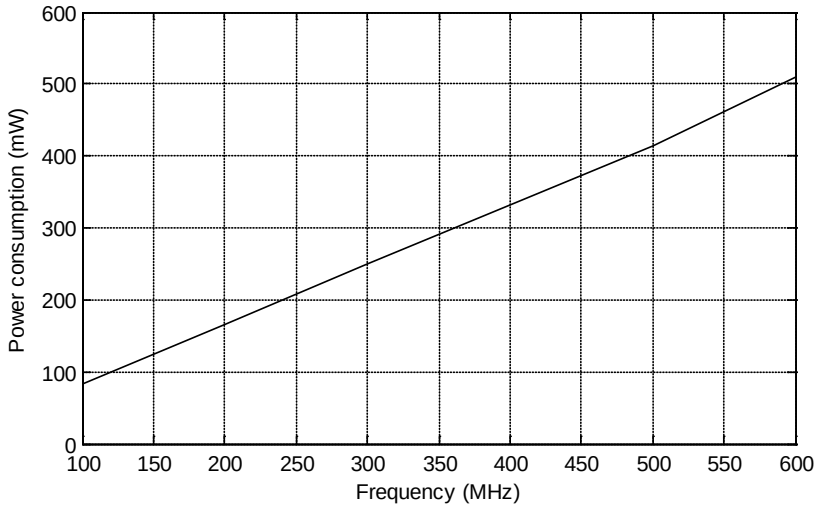
required pins by the number of bits available in any target device. Table.7 shows the number of devices needed for such purpose.

Table(7) Number of devices required to implement the spectrum sensing system.

Device	Number I/O pins	Number of devices
XC6VLX75T	**360**	**13**
XC6VLX365T	**720**	**7**
XC6VSX475T	**840**	**6**
XC6VLX760	**1200**	**4**

However, there is a tradeoff between a choice of a device intensive power and an additional power consumption resulted from the implementation fitted in more than one device. This paper suggests the type XC6VLX760 as a target device to implement the spectrum sensing system with specifications in Table.4 due to acceptable value of power consumption and number of devices required.

Finally, the variation of the power consumption of the system fitted in the device above with different values of clock frequency is plotted in Fig.11. Such plot shows a linear proportionality of the power consumption with the clock frequency.



Figure(11) The variation of the system power consumption with frequency.

CONCLUSION

This paper presents a design of low complexity spectrum sensing system. The simulator used to test the design shows that four devices of (XC6VLX760) Xilinix Vertix-6 FPGA family are enough to implement a system with a structure consists of 250 subcarriers. The results also show that the power consumed in these devices is highly dependent on the number of internal logic transitions and operating clock frequency.

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