Design and Implementation of Convolutional Encoder and Viterbi Decoder Using FPGA.

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Abstract

Keeping the fineness of data is the most significant thing in communication.There are many factors that affect the accuracy of the data when it is transmitted over the communication channel such as noise etc. to overcome these effects are encoding channels encryption.In this paper is used for one type of channel coding is convolutional codes. Convolution encoding is a Forward Error Correction (FEC) method used in incessant one-way and real time communication links .It can offer a great development in the error bit rates so that small, low energy, and devices cheap transmission when used in applications such as satellites. In this paper highlight the design, simulation and implementation of convolution encoder and Viterbi decoder by using MATLAB- program (2011). SIMULINK HDL coder is used to convert MATLAB-SIMULINK models to VHDL using plates Altera Cyclone II code DE2-70. Simulation and evaluation of the implementation of the results coincided with the results of the design show the coinciding with the designed results.
Keywords:- Convolutional encoder, Viterbi decoder, MATLAB-Program,FPGA.

الخلاصة

الحفاظ على دقة البيانات هو الشيء الأكثر أهمية في مجال الاتصالات. هناك العديد من العوامل التي تؤثر على دقة البيانات عندما يتم نقلها عبر قناة الاتصال مثل الضوضاء الخلل تغلب على هذه الاثار يتم تشفير قنوات الترميز. في هذه الورقة يتم استخدام نوع واحد من قناة الترميز هي رموز التلافيف على وجه التحديد. ترميز الالتواء هو أسلوب خطأ إلى الأمام تصحيح (FEC) المستخدمة في وصلات الاتصالات في الوقت الحقيقي المتواصلة في اتجاه واحد التي يمكن أن تقدم تطورا كبيرا في معدلات الخطأ بت وهكذا تكون صغيرة ومنخفضة الطاقة وأجهزة الإرسال الرخيصة عند استخدامها في تطبيقات مثل الأقمار الصناعية. في هذه الورقة تسليط الضوء على تصميم ومحاكاة وتنفيذ التشفير التلافيف وفك فيتربي باستخدام MATLAB– برنامج (٢٠١١). يستخدمSIMULINK HDLالمبرمج لتحويل نماذج MATLAB– SIMULINK إلى رمز VHDL باستخدام لوحات ألتيرا إعصار الثاني70–DE2. تظهر المحاكاة وتقييم تنفيذ نتائج تزامن مع نتائج تصميم.
الكلمات المفتاحية: – التشفير التلافيف، فك تشفير فيتربي، MATLAB برنامج، FPGA.

1. Introduction

In telecommunication and information theory, channel codinghas been used to improve the quality of data transmission. To improve the performance of communication system, there are various numbers of techniques channel coding deals with. Channel coding increases the data transmission rate at a fixed error rate or error rate can be reduced with a fixed data transmission rate in digital communication systems. The maximum performance of data transmission is restricted by Shannon limit [Sh,1948]. There are two basic errors correcting schemes the first one is FEC (the errors can be corrected automatically on its occurrence)and the second is Automatic Repeat Request (ARQ) (using stop-and-wait protocol, where the message is requested to retransmit whenever error is detected) have been employed in communications systems [Calhan *et al*. ,2007]. Choice one of these schemes depend on the application.

As an alternative to block codes, Elias in 1955[Vamshi,2005] introduced convolution codes. Convolutional codes perform encoding on serial data, one or a few bits at a time, while block codes perform encoding on relatively large message blocks. Compareing with the block coding, convolutional encoding performance is better error correction although it requires an extensive memory in decoding [Wayal *et*

al.,2015]. One of the FEC schemes is convolutional encoding which is used for the channel coding in digital communication systems as shown in Figure 1.The convolutional encoding technique is a strategy widely employed in numerous applications in order to achieve reliable data transmission, including radio, digital video, satellite communication andmobile communication [Kolakaluri *et al*.,2015].

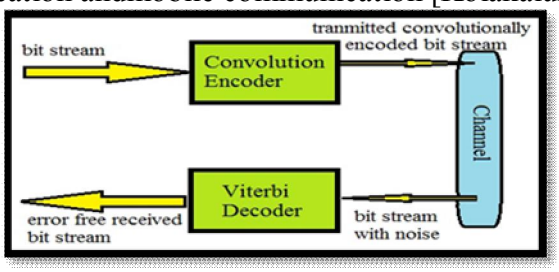

Figure 1. FEC Architecture

A convolution encoders are usually characterized in (n, k, m) format where n represents the number of outputs of bits of the encoder; k is the number of inputs of bits of the encoder and m is the number of memory elements. The organization of convolutional encoder is calculated in terms of rate code. The code rate is the ratio of input to output information in an encoder (k/n).Some further format of convolutional code chips indicate the three factors of code by (n, k, L), where L is the constraint length of thecode and defined as: L= m+1[Pednekar *et al*.,2013].Convolutional encoder is decoded by Viterbi Algorithm (VA) or Maximum A Postoriory (MAP) algorithm.For constraint length L<5, VA is used and for L>5MAP algorithm is employed [Maiya *et al*., 2012].VA is the most resource consuming, efficient and robust.

2. Convolutional Encoder and Viterbi Decoder Description.

A convolutional encoders is an instrument, where the output is a function of they currents state nand they current input. It consists of one nor more D flip flop and multiple Exclusive-OR gates. Exclusive-OR gates are joined to some stage of a number of shift registers memory and to the current input to form the output npolynomials[Calhan *et al*. ,2007].The model used to form the coded output data can be designed as binary strings so called Generator Polynomials (GP)[Wayal *et al*,2015].A convolution encoder is described with the help of state table, state ndiagramnand trellis diagram[Kumawat *et al*.,2012].There are different forms of convolutional encoding which convey different requirements to the decoder.

Based on the maximum likelihood algorithm, in 1967 A.J. Viterbi devised and analyzed Viterbi decoding [Mceliece *et al*.,1996].VA is a decoding process for convolutional codesnand it nuses maximum likelihood decoding ntechnique due to it is the most optimal algorithm for decoding of a convolution code [Sudharani *et al*.,2015; Dhanda *et al*.,2014]. Trellis diagram has been used to describe convolutional encoded data and Viterbi decodeddata at the receiver's end. VA has encoded knowledge of convolutional data and that enables it to perform its decoding[Sudharani *et al*.,2015].The difference of the number of bits between the received symbol bits at the decoder and the sent symbol bits fromn the encoder is defined as Hamming distance[Shukla *et al*.,2014]. Soft decision Viterbi decoding determines the distance between the observed symbol and the probable sent symbol and discoversoriginal bits. The basic performance of the viterbi decoder is branch metric, path calculation and survivor management unit[Selvi *et al*.,2015]. The architecture of the viterbi decoder is illustrated in Figure 2.

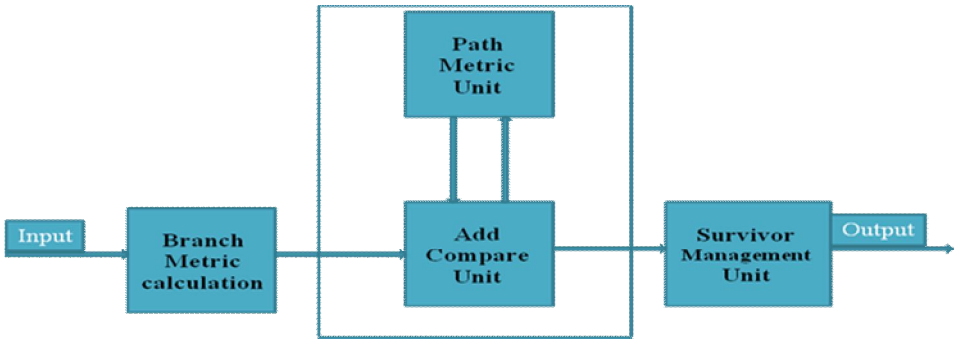

Figure 2. Viterbi decoder Basic building blocks [Shukla ,2014].

3. Design and Simulation of Convolutional Encoder and Viterbi Decoder Using MATLAB

The describe of the structure for convolutional encoder with rate[1/2]and code generators [7,5] is used. Figure 3 shows the structure for convolutional encoder. Table 1 shows the calculation of output bits for described convolutional encoder which has constraint length of 3 when input message is 1011011. Figure 4 shows the simulation result of convolutional encoder without flushing bits. The simulation result observes that the output bits are 11100001010001.Figure 5describes the trellis diagram of convolution encoder. Figure 6shows communication system with the simulation result of viterbi decoder. In order to verify the simulation results for convolutional encoder and viterbi decoder two cases are used. The calculated results show the coincidence with simulation results.

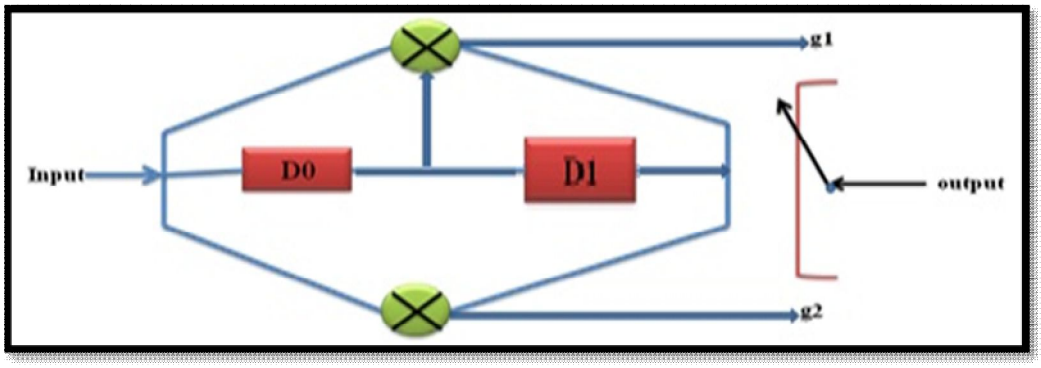

Figure 3.The structure for convolutional encoder.

Table 1: Output bits for the convolutional encoder when input message is 1011011

Input	Modulo 2 Adder Outputs	
	$g_1 = 111$	$g_2 = 101$
1	1	1
0	1	0
1	0	0
1	0	1
0	0	1
1	0	0
1	0	1
Output=11100001010001		

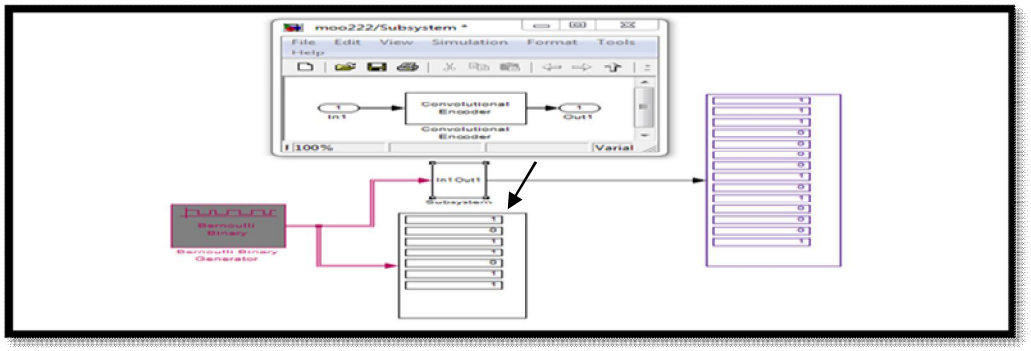

Figure 4. The simulation result of convolutional encoder.

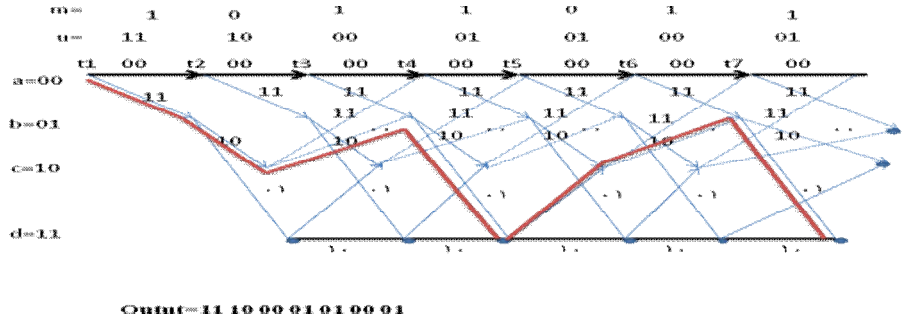

Figure 5.The trellis diagram of convolution encoder.

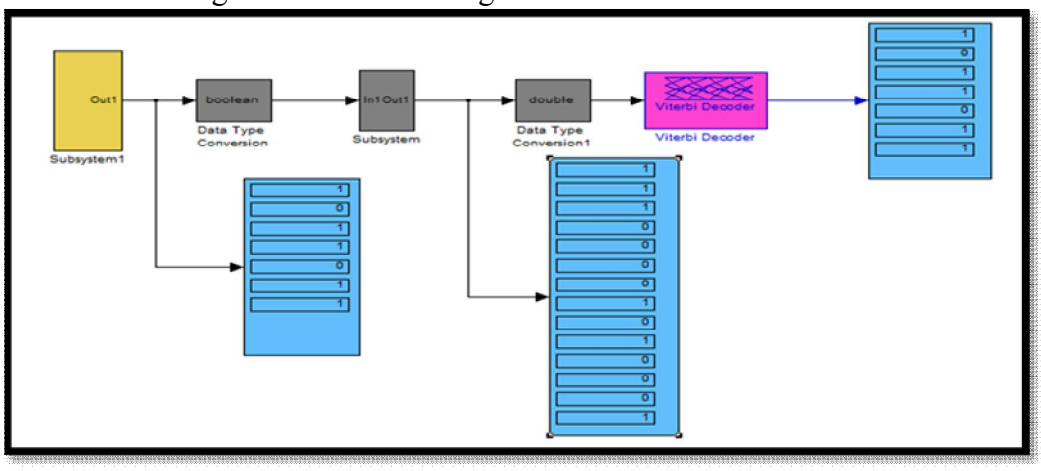

Figure 6. The simulation result of viterbi decoder.

4.The Register Transfer Level(RTL)implementation of Convolutional Encoder and Viterbi Decoder based on FBGA.

Figure (7)describes the procedure the design and implementation technique used .To perform the convolutional encoder and Viterbi decoder implementation RTL program has been used. Figure (8) describes the RTL implementation of the convolutional encoder based on FBGA. Figure (9) describes the RTL implementation of the viterbi decoder basedbased on FBGA.

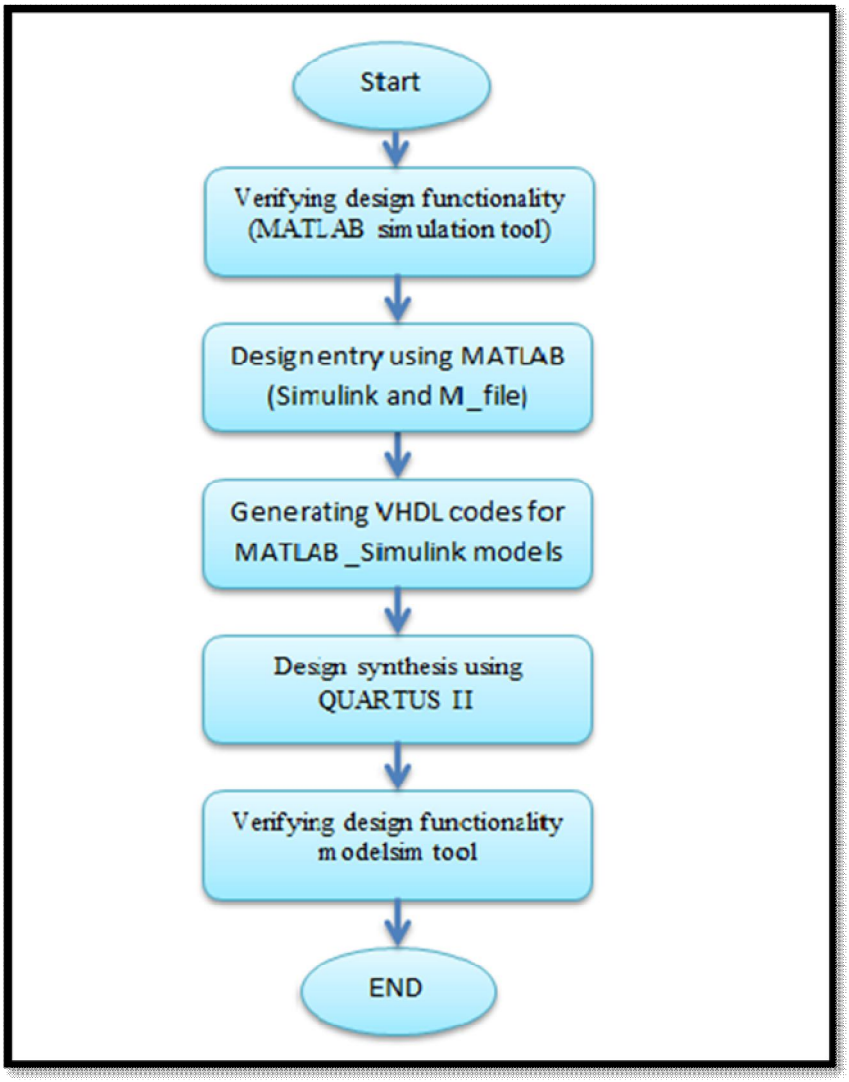

Figure 7.Flow chartdesign procedure.

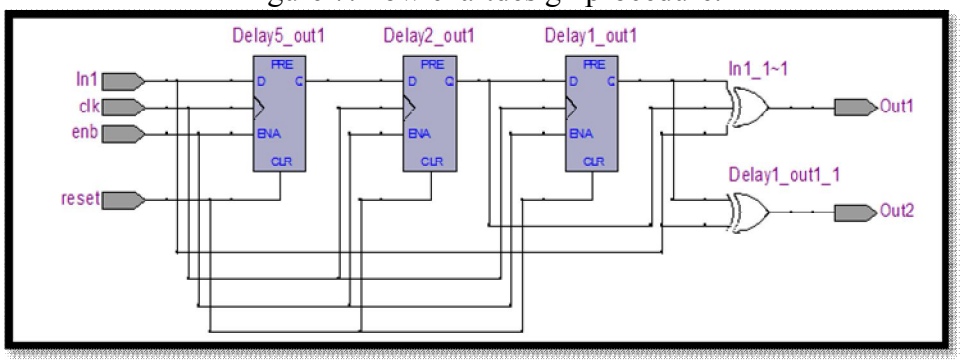

Figure 8.The RTL implementation of the convolutional encoder baseds on FPGAs.

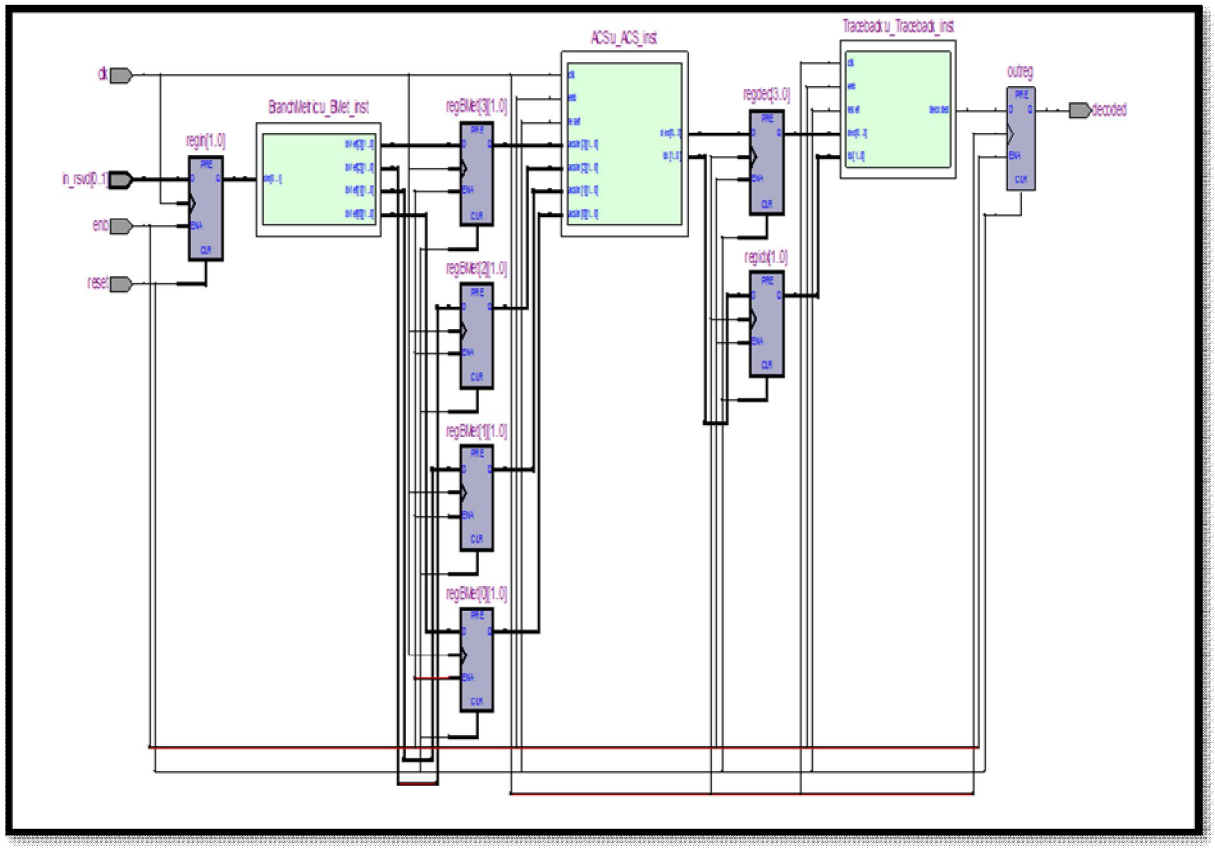

Figure 9.The RTL implementation of the viterbi decoder units based on FPGAs.

5 . Simulation of Convolutional Encoder and Viterbi Decoder based on Modelsim using FBGA.

Modelsim program is used to test the results of matlab simulation. Figure (10) shows the input and output signals for convolutional encoder with a rate of [1/2] based on FBGA. Figure (11) shows the input and output signals for Viterbi decoder based on FBGA.

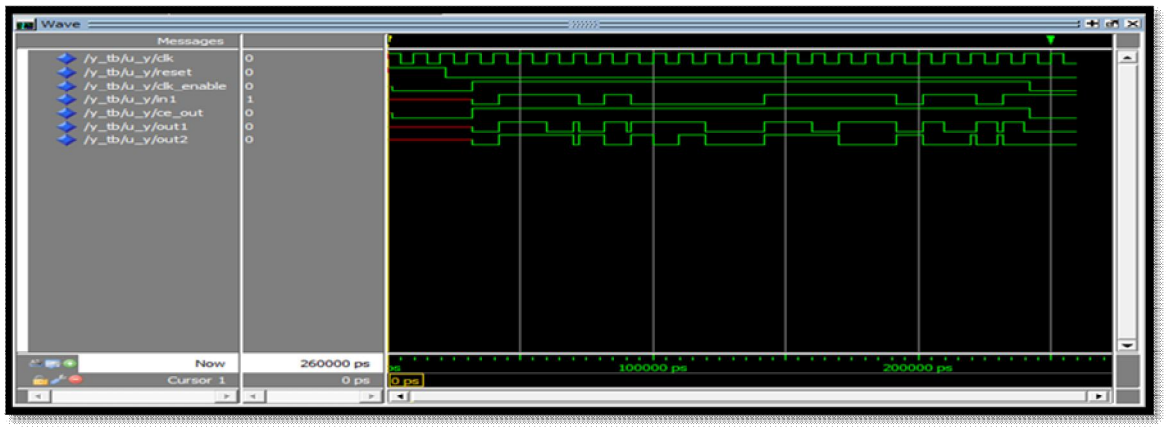

Figure 10.A rate of 1/2 convolutional encoder.

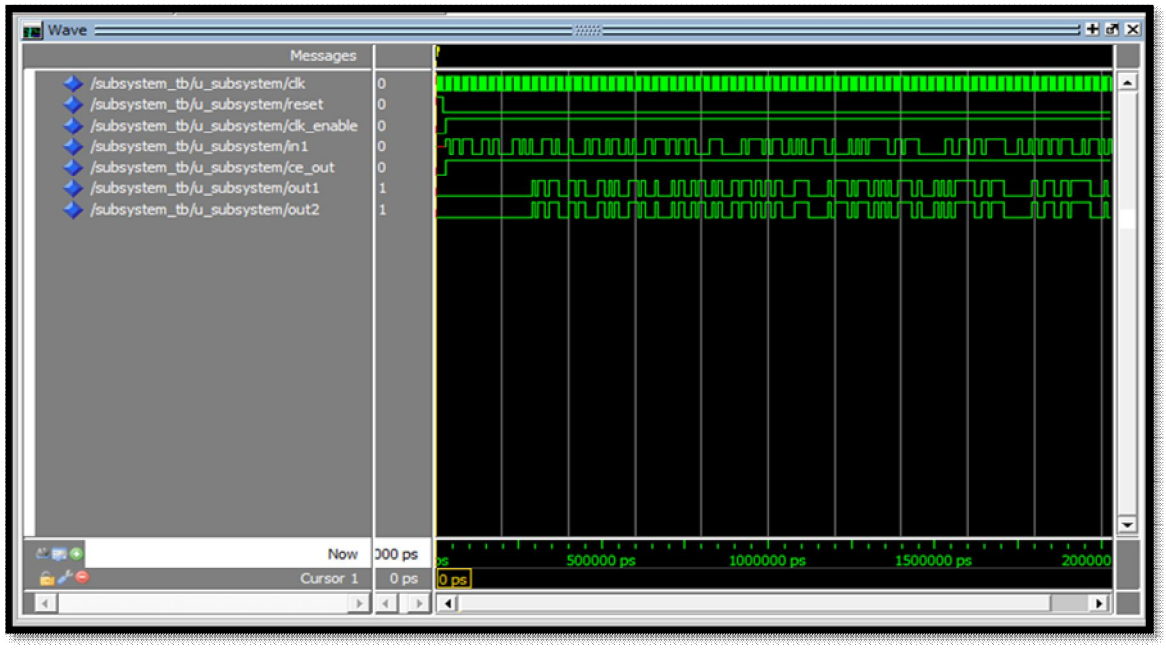

Figure 11. The input and output signals for viterbi decoder

6.Conclusions

Forward error correction (FEC) codes are an essential part of the digital communication systems. Convolutional codes are used symbols to perform encoding technology. The Viterbi algorithm has proven to be a powerful tool in the decoding technique for Convolutional codes. As well as MATLAB simulink has proved its ability to design and verify convolutional encoder and viterbi decoder. FPGA proven to be effective mechanism for the implementation of the system where it was send a signal after encoded using Convolutional codes and receiving and decoding using Viterbi algorithm.the simulation results confirm that the signal is received without the occurrence of errors in the transmitted signal, which provides FPGA high speed, and high level of integration, low development costs and require low energy.

Trade shows Oltara- CYCLON several DE2-70 second FPGA family is cabability efforts to implement the verification of the proposed system performance evaluation.

7.References

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