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THE EFFECTS OF PARASITIC INDUCTANCE AND AIR-COOLING ON PRINTED CIRCUIT BOARDS (PCBS)

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ABSTRACT

There is a need to increase the speed of the power converters for many applications. Nevertheless, one of the limiting factors for power device performance is the parasitic inductances as the switching speed becomes higher. These parasitic inductances act as reaction elements that affect the switching process, and generate high voltage spikes across the PCB. In other words, the advantages of low parasitic inductances in PCB are offered best switching performance for high efficiency and minimizing conduction losses.

In this paper the effect of the parasitic inductances for a synchronous buck converter has been analyzed. MATLAB simulations have been developed to show their effects on the performance of the synchronous buck converter. Furthermore, another MATLAB simulation has been built to show the thermal consideration. This simulation could predict the air cooling budget that the PCBs might need to reduce their operating temperatures.

KEYWORDS:

Buck Converter, MOSFETs, Parasitic Inductances, Power Converter, Printed Circuit Boards

تأثير الحث الطفيلي وتبريد الهواء على لوحات الدوائر المطبوعه

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الخلاصة

هناك حاجة لزيادة سرعة محولات الطاقة في العديد من التطبيقات. ويعد الحث الطفيلي واحد من العوامل التي تحد من أداء جهاز القدره في الوصول الى سرعه أعلى . يكون الحث الطفيلي بمثابة رد فعل العناصر التي تؤثر على عملية التحول، وتولد شرارة جهد عالية في لوحة الدوائر المطبوعه . وبعبارة أخرى، فإن مزايا تقليل الحث الطفيلي في اللوحه هي توفير أداء أفضل للمفاتيح بكفاءه عالية وتقليل خسائر التوصيل .

في هذه البحث تم تحليل تأثير الحث الطفيلي لمغيير خافض متزامن .واستخدمت المحاكاة MATLAB لإظهار تأثيرها على أداء المغير الخافض المتزامن .وعلاوة على ذلك، تم بناء محاكاة آخر MATLABلإظهار الاهميه الحراريه , هذه المحاكاة أمكنت التنبؤ بميزانية تبريد الهواء التي تحتاجها اللوحه المطبوعه لتقليل درجات حرارة الاشتغال.

1. INTRODUCTION

High efficiency becomes necessary in PCB devices. To achieve that, PCB devices should have very fast switching. However, the fast switching devices create critical issues on the PCB layout. A good PCB layout design should minimize thermal stress, reduce the noise interfaces among traces, and minimize the parasitic inductances. The parasitic inductances cause power losses and then affect the switching speeds [2-4].

In this paper a MATLAB simulation has been built for the synchronous buck converter to focus on the effects of the parasitic inductances and how these parasitic inductances can be minimized. Another MATLAB simulation has been developed for the PCB thermal consideration that can help to predict the air cooling size for the module

2. THE PARASITIC INDUCTANCE

The inductance can be defined as the ratio of the voltage across the inductor to the rate of change of its current as given [5]:

$$L = \frac{v}{\frac{di}{dt}} \tag{1}$$

The inductance can be classified in two types, which are self-inductance and mutual-inductance. They can be derived as in [6]:

$$L_s = \frac{Ml}{8\pi} \tag{2}$$

$$L_m = 0.002l\left[\ln\left(\frac{l}{d}+\sqrt{1+\left(\frac{l}{d}\right)^2}\right)-\sqrt{1+\left(\frac{d}{l}\right)^2}+\frac{d}{l}\right] \tag{3}$$

where l is the length of the wire ,M is mutual and d is the thickness of the cross-section area, respectively. It is obvious from (eq.2) that the parasitic inductance can be minimized by minimizing the current path length l and increasing the cross-section area.

3. THE PARASITIC INDUCTANCE OF THE WIRE BONDING

Power MOSFET losses during its operation can be written as in [2]:

$$P_T = P_{con} + P_s \tag{4}$$

$$P_{con} = I_{rms}^2 R_{on} \tag{5}$$

$$P_s = \left(E_{on} + E_{off}\right)f_s \tag{6}$$

where P_{con} is the conduction power loss, and P_s is the switching power loss. However, this approach may increase the devices losses. Because the lost energy is dependent on current and voltage waveforms during switching, faster switching causes a lower energy loss.

4. POWER SWITCHING CONVERTER AND PARASITIC

The parasitic inductance increases the switching transition time, as in (eq.1) because the turn-on and turn-off transient cause the parasitic inductances to act as a reaction element. Because the switching loss is dominant, this problem can be easily seen in the synchronous buck converter [2, 7], as shown in Fig. 1.

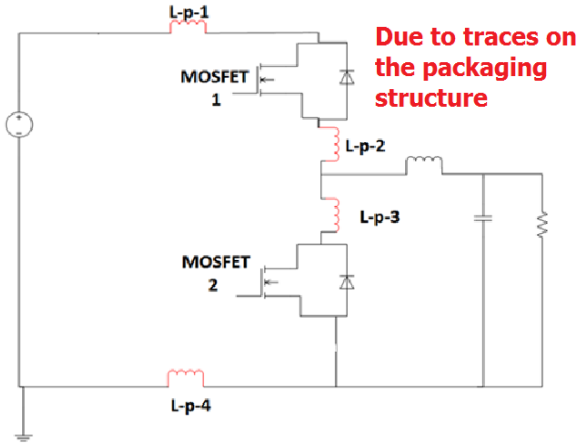

Fig. 1. Synchronous buck converter with parasitic inductances where L-p-1, L-p-2, L-p-3, and L-p-4 are the parasitic inductances

As shown in Fig. 1, L-p-1, L-p-2, L-p-3, and L-p-4 are the parasitic inductances. These parasitic inductances on the packaging structure (printed circuit board or module substrate) can be reduced by using a decoupling capacitance as illustrated in Fig. 2. This capacitance could minimize high switching loss. The decoupling capacitance would reduce the Delta-I-Noise caused by parasitic inductance [5].

To minimize the parasitic inductance, the pulsating current should be short and wide. Decoupling capacitance should be used to reduce the current loop.

As in equation (2), the loop area between the two MOSFETs (n-channel) and the capacitance should be as close to each other as possible as shown in Fig. 3. The decoupling capacitance should connect directly without bias, which means the decoupling capacitance should be as close as possible to their pins to reduce connection impedance [9].

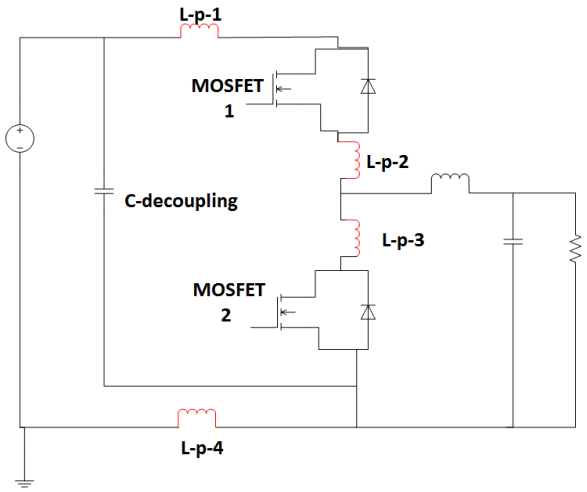

Fig. 2. A synchronous buck converter with decoupling capacitor

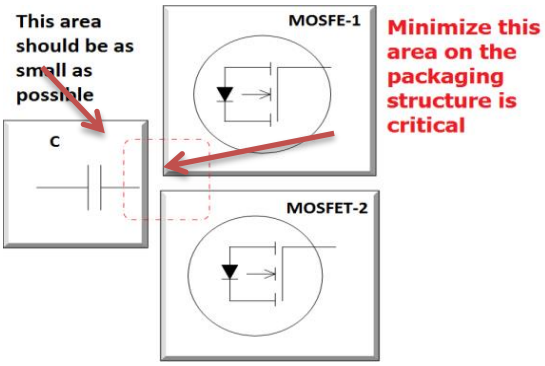

Fig. 3. The area that should be minimized in a synchronous buck converter

5. THERMAL CONSIDERATION FOR PCB

The thermal consideration has an important impact on the devices due to the fact that it decreases the failure rate and increases the chip density [6, 8]. The air cooling is simple, easy to maintain and has cost effective [6, 9]. The simulation for the overall thermal system including heat source, heat convection and air fan is developed. This simulation could predict the suitable air-cooling size for a PCB.

Heat convection is heat by random molecular motion such as air [10]:

$$q = Ah(T_s - T_\infty) \tag{7}$$

This equation is Newton's law of cooling, where q is the heat transfer in time (W), T_s and T_∞ are the surface and fluid temperatures, respectively, A is the cross-section area, and h is the convection heat transfer coefficient (W/$m^2.K$).

The heat conduction is heat transfer by conduction between two layers without any motion. The Fourier's Law is given as:

$$q = \frac{T_1 - T_2}{L/kA} \tag{8}$$

where K is the thermal conductivity (W/$m.K$), and L is the thickness. The expression L/kL is the thermal resistance for conduction.

The energy balance for the component as given in [10] is:

$$E_{st} = E_{in} + E_g - E_{out} \tag{9}$$

where E_{in} and E_{out} are the energy at the boundaries, and E_g is the heat that generates inside the component. However, if the component is treated as a lumped mass, there is a difference between the inside of the component and its outside. Therefore, the energy balance could be written as [11]:

$$E_{st} = mC_p(d_T/d_t) \tag{10}$$

where m is mass, C_p is the mass-average specific heat of all the masses that make up the component, and d_T/d_t is the rate of component change.

The following block diagram Fig. 4. explains how to use the above thermal concepts to model the heat consideration for a PCB. An ideal temperature source is used to consider the outside temperature, and the heat source represents the heat that may be added from another PCB device.

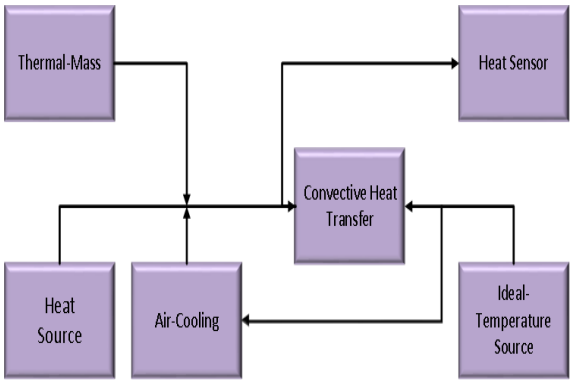

Fig. 4. Heat consideration block diagram for an overall system

6. EXPERIMENTAL RESULTS AND DISCUSSION

To achieve a synchronous buck converter by MATLAB simulation, its MOSFETs switches can be controlled by generating PWM signals. The results would compare the synchronous buck converter before and after adding the decoupling capacitor. For that reason, a MATLAB simulation has been built as shown in Fig. 5. Figs. 6 and 7 illustrate the drain to source voltage of the MOSFET-1 and MOSFET-2, which related to Fig. 1, which is without the decoupling capacitor. It is obvious from Figs. 6 and 7 the oscillation of the drain to source voltage in volt is very high. In addition, they have a very slow response, and high overshoot.

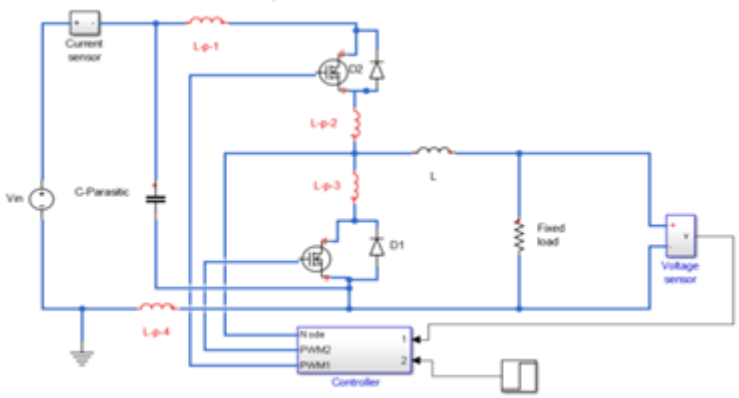

Fig. 5. A MATLAB simulation for synchronous buck converter with decoupling capacitor

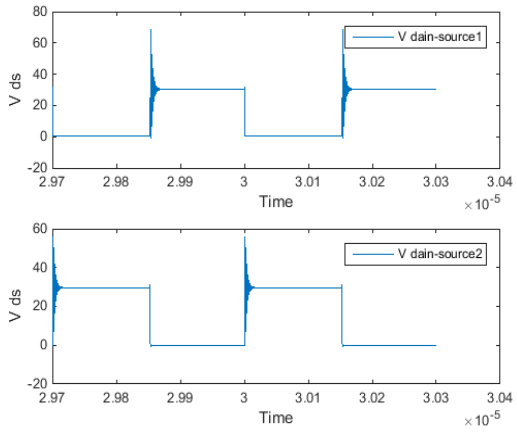

Fig. 6. Drain to source voltage for MOSFET 1 and MOSFET 2 before adding decoupling capacitor

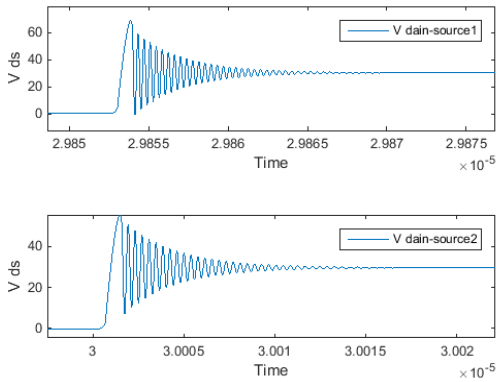

Fig. 7. Drain to source voltage for MOSFET 1 and MOSFET 2 before adding decoupling capacitor for sample time period from 3.00 * 10^{-5} to 3.002* 10^{-5} s

Figs. 8 and 9 show the voltage of the drain to source for both synchronous buck converter's MOSFETs after adding the decoupling capacitor. It is obvious from Figs. 6 and 7 the oscillation of the drain to source voltage is very high compared with Figs. 8 and 9. That is because the loop parasitic inductances become minimized.

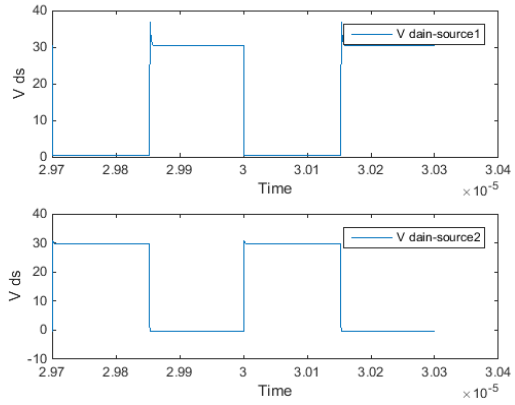

Fig. 8. Drain to source voltage for MOSFET 1 and MOSFET 2 after adding decoupling capacitor

The MATLAB simulation also includes a simulation for thermal consideration. The thermal consideration was simulated based on Fig. 4. The thermal consideration that is developed can be used to select the suitable fan cooling for the module. This simulation depends on the thermal consideration concepts for PCB. The temperature-time curve shows three temperature stages as shown in Fig. 10.

The first stage is due to environment heat, which acts gradually on the system. The second stage is the heat source that could affect the PCS causing the temperature to rise higher than the previous stage. The third stage is when the Air-Cooling system causes a quick reduction in the temperature. By knowing the thermal conductivity (k), the mass- average specific heat of all the masses for the component (C_p), the component mass (m), the surface area, and ambient temperature, the simulation can predict the suitable air cooling size for the PCB.

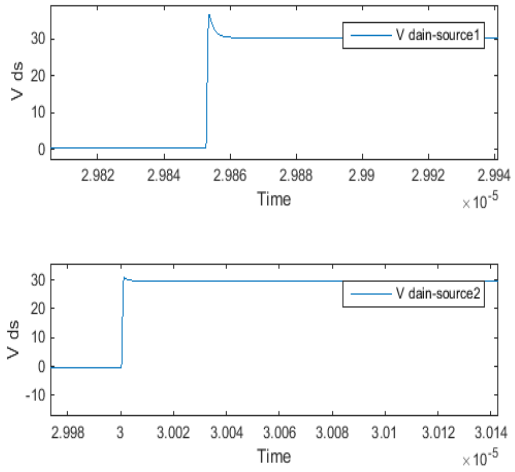

Fig. 9. Drain to source voltage for MOSFET 1 and MOSFET 2 after adding decoupling capacitor for sample time period from 2.998* 10^{-5} to 3.014* 10^{-5} s

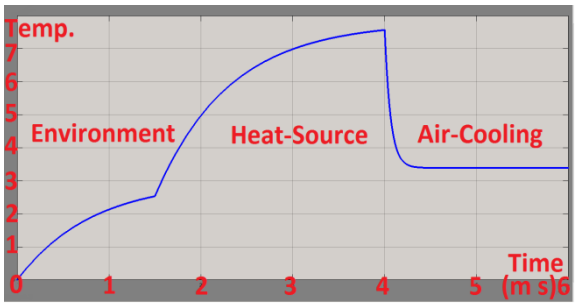

Fig. 10. The Temparture time curve due to environment heat, heat source, and air-cooling

7. CONCLUSION

The MATLAB simulation shows that the losses due to parasitic inductances could be reduced by using a decoupling capacitor. It also shows that the time response for the converter's MOSFETs become faster and smoother. The minimum parasitic loop,

which resulted in a fast speed converter, could be achieved by using a suitable size of capacitor. Thermal consideration also has been done by MATLAB simulation to predict the size of the air-cooling for the system.

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