Reducing the Impacts of Distributed Generation in Transmission & Distribution Networks Protection Using Fault Current Limiters

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ABSTRACT

Increase in power generation capacity of electric power systems has lead to increase in the fault current level. In some cases fault current levels are exceeding the interrupting capability of existing transmission and distribution substations circuit breakers. Since short-circuit currents contain extremely high energy and can damage electrical equipment, either requires the replacement of a large number of existing substation breakers with higher rating breakers or the development of some means to limit fault current. Different technologies have been employed to design Fault Current Limiters FCLs such as turn-off a solid state switch to using superconductors that respond with increasing resistance in event of fault current. A proper design of Modular Level Based Solid-State Fault Current Limiters is proposed in this paper, describes the functioning of FCL and the amount of impedance they are required to insert in series with transmission or distribution substation are discuses. This will allow near instantaneous breaking of bus ties in transmission and distribution substations to reduce the available short circuit current and allow existing circuit breakers to clear at lower fault current levels. Since FCL's are installed in each phase of the line, the fault is viewed in perspective of per phase. For the purposes of this study, we consider phase to ground fault & phase to phase fault scenarios.
Keywords: Distributed Generation, FCL

الحد من تأثير المولدات الموزعة (DG) في حماية شبكات النقل والتوزيع بإستخدام محددات لتيار العطل

الخلاصة

إن زيادة سعة التوليد لنظم القدرة الكهربائية يكون السبب في رفع مستوى تيار العطل. في بعض الحالات مستوى تيار العطل يتجاوز مقننات القطع لقواطع الدورة في عموم نظم نقل وتوزيع الطاقة , وحيث ان تيارات العطل تمتلك طاقة عالية لها القدرة على اتلاف معدات المنظومة الكهربائية كافة لذا تطلب الامر إما ابدال قواطع الدورة بإخرى ذات مقننات قطع اكبر(خيار غير اقتصادي) أو اللجوء الى استخدام محدد لتيار العطل.

العديد من التقنيات أستخدمت في تصميم محددات تيارات الاعطال منها مفتاح الحالة الثابتة ذو بوابة الاطفاء turn-off a Solid State Switch والتي اظهرت قدرة عالية في تقليل

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مستوى تيار العطل من خلال استجابته كموصل فائق التوصيل حيث يعمل على تحويل مسارالتيار الى عنصر ماص للطاقة (ممانعة) حال تحسسه لحدوث عطل. في هذا البحث تم اقتراح محدد تيارعطل بمستوى نسقي له قدرة على اضافة عدد من المستويات (الممانعات) وبشكل تتابعي ومناقشة كيفية تحديد مقدار الممانعة (عدد المستويات) الواجب اضافتها الى منظومة النقل والتوزيع لتقليل تأثير الزيادة الحاصلة في نسبة التوليد وما ترتب عليها من ارتفاع في مستوى تيار العطل وبما يمكن قواطع الدورة من العمل ضمن مقتناتها.

في النظم ثلاثية الأطوار يتم تنصيب محدد تيار العطل لكل طور, لذا تم مناقشة تأثيرة من خلال عطل أرضي (أحد الاطوار والارضي) وعطل طوري (طور مع طور آخر).

INTRODUCTION

In recent years, penetration of Distributed Generation (DG) into distribution systems has been increasing around the world. Major reasons for this trend are liberalization of electricity markets, increased demand for the electricity, constraints on building new transmission and distribution lines and environmental concerns [1],[2]. There is a wide range of terminologies used for "distributed generation," such as "embedded generation," "dispersed generation," or "decentralized generation". *DG* essentially means a small - scale power station different from a traditional or large central power plant [3]. At present, there are several technologies ranging from traditional to nontraditional used in DG application. The former is nonrenewable technologies such as internal combustion engines, combined cycle, combustion turbine, and micro turbines. The latter technologies include fuel cells, storage devices, and a number of renewable energy- based technologies such as photovoltaic, biomass, wind, geothermal, ocean, etc. Along with its benefits, (DG) may have negative impacts on the distribution system since it connected in parallel, so the equivalent source impedance of the expanded network decreases with each new supply that is added, and as a consequence the fault current increases since there is less impedance between the equivalent source and the point where the fault occurs. This issue is more acute where there is a high density of loads (e.g., large metropolis) [4],[5]. Several ideas have been introduced as possible solutions [6], [7]. These papers propose switchgears and protection coordination upgrade in systems consist of DG.

Although these solutions may technically operate, they are complicated and expensive. So, these solutions are not practical for existing distribution systems. A novel idea exists to limit the fault currents produced by DG and prevent switchgears upgrade is FCLs application [5]. The implementation of FCLs in electric power systems is not restricted to suppress the amplitudes of the short circuits; they are also applied in variety of performances such as the power system transient stability enhancement, power quality improvement, reliability improvement, increasing transfer capacity of system equipments and inrush current limitation in transformers [8-13].

'FCL' is a variable-impedance device connected in series with a circuit to limit the current under fault conditions [14].

SYSTEM REQUIREMENT FOR CURRENT LIMITERS

The commercial success of a fault current limiter at distribution or transmission levels depended on how cost effect it is as compared with highly competitive one. Ideally FCL should be design to operate under the following characteristics [15]

1- It should have a zero impedance and zero active and reactive power losses under normal system conditions.
2- It should detect, discriminate and respond to all types of short-circuit faults in less than 1 or 2 ms.
3- When it responds, it should insert very high limiting impedance to limit current flow.
4- It should automatically and quickly recover once the fault has been removed ready for another current limiting operation.
5- It should be capable of performing successive current limiting operations without replacement.
6- It should cause no unacceptable over voltages or harmonics in the power system.
7- It should have no adverse impact on power system protection performance.

TYPES OF FAULT CURRENT LIMITERS

Since a fault current limiter is a series device, it must present low impedance to current flow under normal conditions. When a fault occurs or (additional generators added to meet ever increasing load demand), this impedance must rapidly increase to limit the current flowing into the fault. Conceptually, all types of FCL may be viewed as a normally closed switch in parallel with a resistor. The type of switch, its control circuit, and the type of resistor may vary widely from one design to another. FCL(s) can generally be categorized into three broad types: [16]

1. Passive limiters: limiters that do not require an external trigger for activation.
2. Solid state type limiters: limiters use a combination of inductors, capacitors and thyristors or Gate Turn-off Thrusters (GTO) to achieve fault limiting functionality.
3. Hybrid limiters: limiters use a combination of mechanical switches, solid state FCL(s), superconducting and other technologies to create current mitigation.

In the past, many approaches to the FCL design have been conducted ranging from the very simple to complex designs.. Appendix A of this paper has a consolidated and more detailed list of the different FCL types.

SOLID STATE FAULT CURRENT LIMITER & ITS DESIGN CONSIDERATION

In this paper, solid state FCL [17] is used and its effect on fault current is analyzed. The most beneficial property of this configuration is simplicity of structure and control, low stead state impedance, fast response and high impedance fault. Fig.1 shows a general configuration of the solid-state current limiter. It consists of a fast solid-state switch, current limiting impedance, voltage limiting element (varistor) and series mechanical switch. The (GTO) are used as the fast solid-state switch and the current limiting impedance is connected in parallel with these. The GTO thyristors are used to interrupt a current instantly upon receiving a turn-off signal and the current limiter impedance is used as way for passing the fault current when the solid state switch interrupt a fault current. But a sudden interruption of current is likely to cause an overvoltage in the circuit, so the voltage limiting element is used to prevent this [17].The over current detector and control device detect a fault and produce turn-off and turn-on signals for the GTO thyristor. Figure (2) shows the control block diagram of this FCL. In steady state condition, the GTOs are gated continuously.

When a fault occurs a fault current must be detected rapidly. This is done by comparing the instantaneous current level with a predetermined value. After detecting fault occurred, the turn-off signal is given to the GTO. In this method, it is important to discriminate fault current from an in-rush current. This problem was solved by choosing a suitable detection level. The current limiter must continue to limit the current during fault and returns it to the normal condition automatically after the fault is cleared. Therefore, current magnitude has to be monitored all the time. When detector recognizes the current magnitude small for some period, clearance is assumed and turn-on signals are given to the GTO. Therefore, in steady state operation only switching loss appears which is very smaller than other losses in the network.

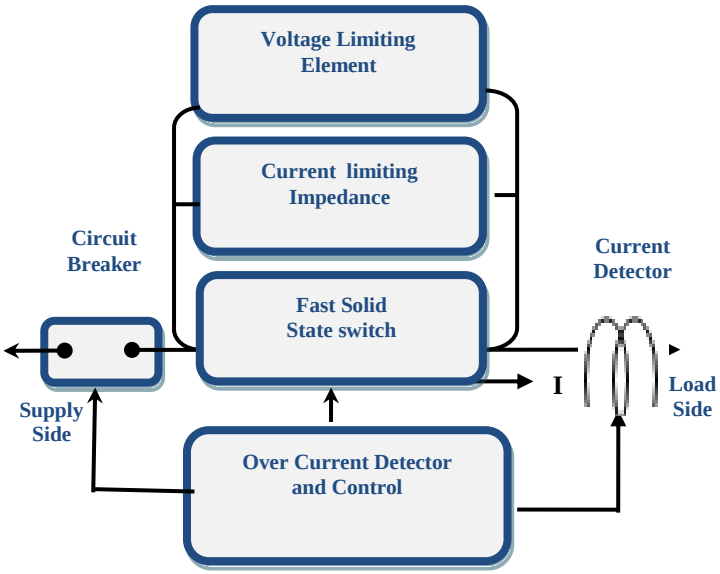


Figure (1) Block Diagram of S S F C L.

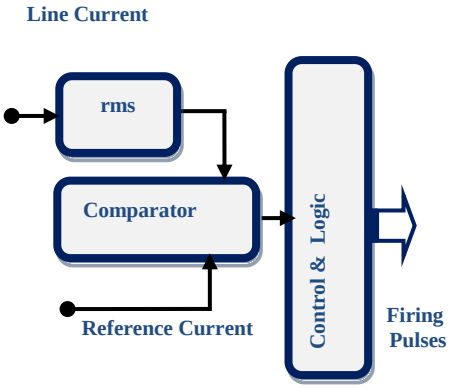


Figure (2) Schematic diagram of S S F C L.

CASE STUDY OF SINGLE LINE TO GROUND FAULT (SLGF)

Consider Figure (3), in which many power generating sources (represented by the single generator equivalent source impedance) connected to 69kv three-phase transmission line through a delta-wye transformer, which feed a static load. This is a general representation of a tie between two networks, into which an FCL can be placed. This tie line has a per phase to ground short circuit fault current of 40KA due to existing generation at the source, which is within the capability of the system fault control equipment (breakers, transformers, etc.). Mid-section in this diagram, the single line is transformed in to a three-line diagram to highlight the phase undergoing fault. The source impedances of all generating stations collectively determine the fault current value. It is possible, then, from additional generators added to meet ever increasing load demand, that the source impedance of the line could be significantly reduced, therefore leading to higher fault currents. The occurrence of a fault downstream can then lead to currents that exceed the ratings of currently installed 40kA rated circuit breakers. It is then necessary that the utility replace these breakers

with those of higher short circuit current ratings to avoid long term outage of the line. All this comes at an increased operational cost to the utility company.

By inserting an external impedance into the line, during fault, the short circuit current is brought down to a value that can be safely interrupted by the existing circuit breakers without having to replace them. This series impedance can be introduced incrementally into the line, depending on the condition of the source impedance of the line, i.e. whenever additional generation causes the source impedance to fall, increasing values of series impedance in the FCL can be inserted to match the fault current to the safe limit.

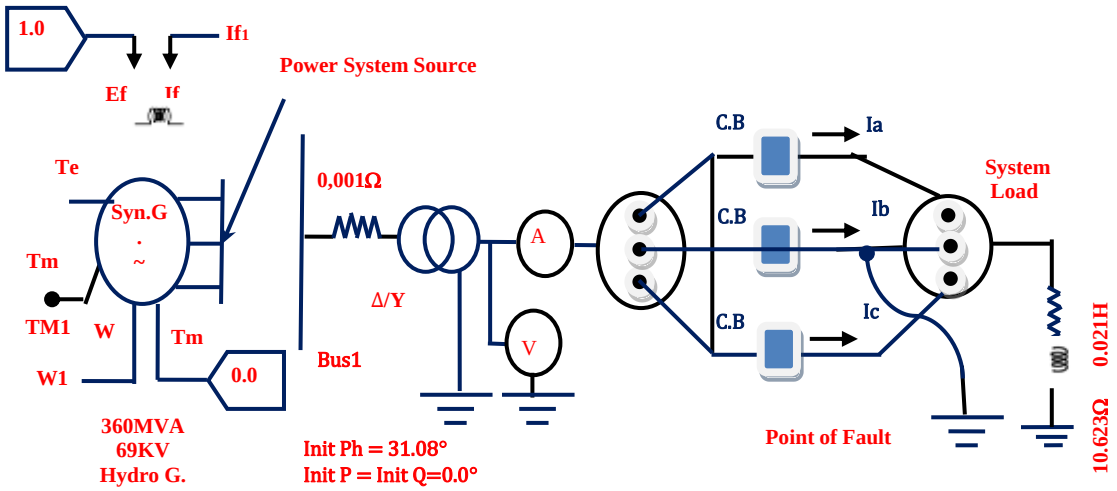


Figure (3) Diagram of a Tie-Line with A source & Load & Point of Line to Ground. Fault in the System.

It is calculated that the system impedance of this line is $Z_s = \frac{V}{I_f} = \frac{69KV}{\sqrt{3}*40KA} = 1\Omega$ Suppose the generation to this line is increased by 25%. We then have a short circuit current of 50kA and the source impedance is 0.8 Ω. Since this is beyond the SC rating of the breaker in place, the FCL would then have to insert an impedance of 0.2 Ω to limit the current back to 40kA. Table1 shows the decrease in source impedance and incremental FCL impedance needed to limit to 40kA, depending on percentage increase in generation.

Table (1)

Generation Source	IF (KA)	Equivalent Source Impedance Zs(Ω)	Impedance to be Added Za(Ω)
Existing Generation	40	$Z_s = \frac{V}{I_f} = \frac{69KV}{\sqrt{3} * 40KA} = 1\Omega$	Non

25% Increase Generation	50	$Z_{s1} = \frac{V}{I_f} = \frac{69KV}{\sqrt{3} * 50KA} = 0.8\Omega$	0.2
50% Increase Generation	60	$Z_{s2} = \frac{V}{I_f} = \frac{69KV}{\sqrt{3} * 60KA} = 0.667\Omega$	0.333
75% Increase Generation	70	$Z_{s3} = \frac{V}{I_f} = \frac{69KV}{\sqrt{3} * 70KA} = 0.57\Omega$	0.43
100% Increase Generation	80	$Z_{s4} = \frac{V}{I_f} = \frac{69KV}{\sqrt{3} * 80KA} = 0.5\Omega$	0.5

Figure (4) shows the vector diagram of impedance, which displays the amount of impedance to be added for the increase in generation highlighted in the table above.

Where :
*Zf is the original Zs @ 40kA
*Zs1, Zs2, Zs3& Zs4 are source impedance during increase generation of 25%, 50%,75%,100%
*Za1, Za2, Za3& Za4 are added impedance required in these four cases, then:
Zs1 + Za1 = Zf
Zs2 + Za2 = Zf
Zs3 + Za3 = Zf
Zs4 + Za4 = Zf

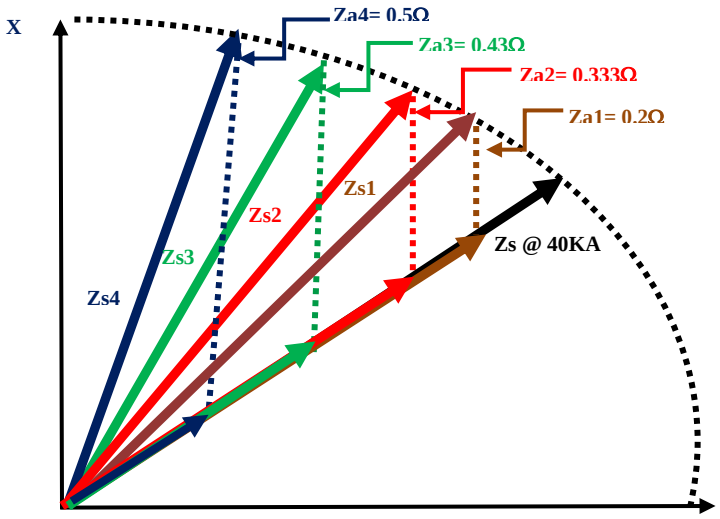


Figure (4) shows the vector diagram of impedance for the values of fault current shown in Table(1).

Figures (5-8) show how the short-circuit current is reduced with respect to the prospective fault current of the system for the 4 cases.

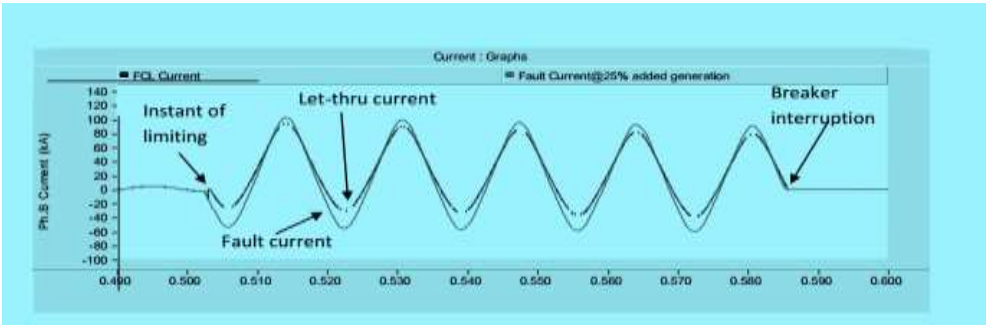


Figure (5) for 50kA fault current with and without inserting a 0.2Ω FCL impedance.

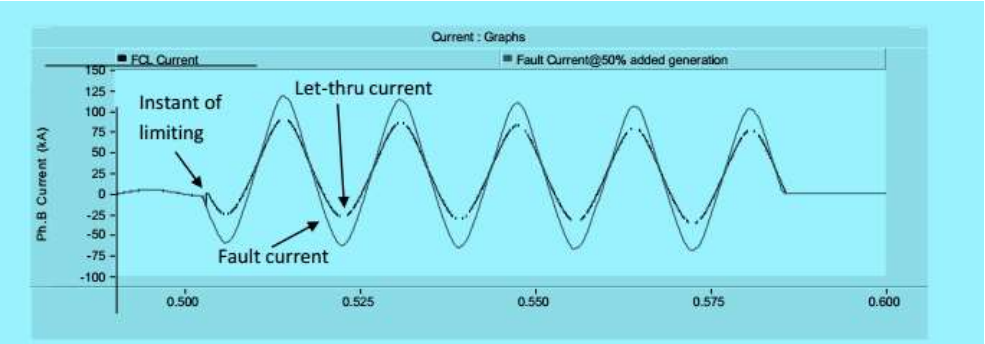


Figure (6) for 60kA fault current with and without inserting 0.33Ω FCL impedance.

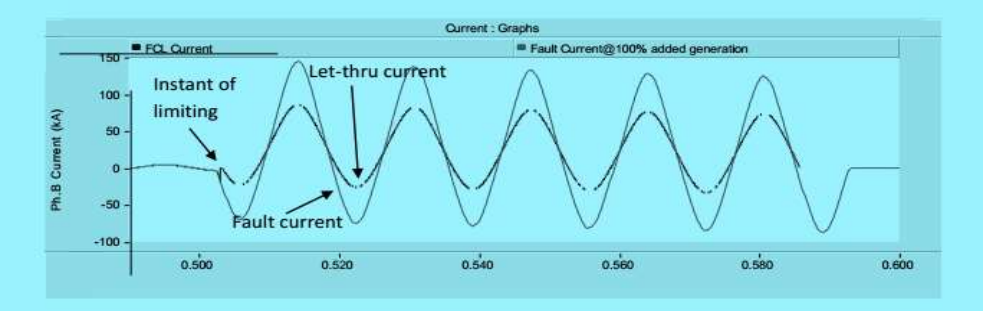
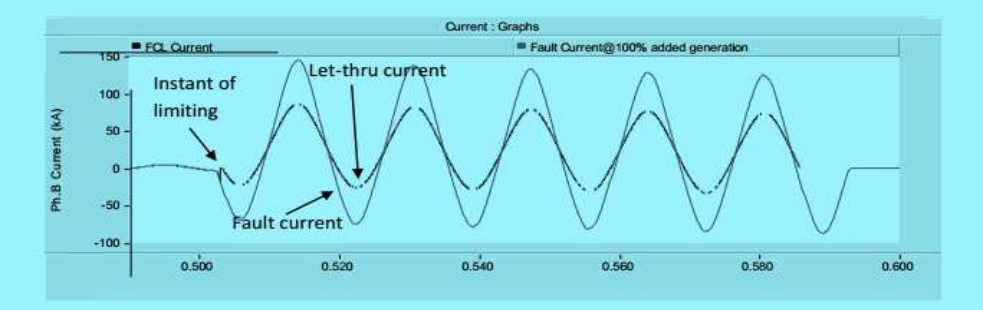


Figure (7) for 70kA fault current with and without inserting a 0.43Ω FCL impedance.



Figure(8)for 80kA fault current with and without inserting a 0.5Ω FCL impedance.

CASE STUDY OF A LINE TO LINE FAULT (LLF)

Consider Figure (9) in which case there is a line-to-line fault downstream of the circuit breaker. In this case both breakers on phases B and C have to trip. Then, knowing the system impedance, the fault current in these two phases is:

$$I_f = \frac{V}{Z_{equ}} = \frac{69KV}{1+1} = 34.5KA$$

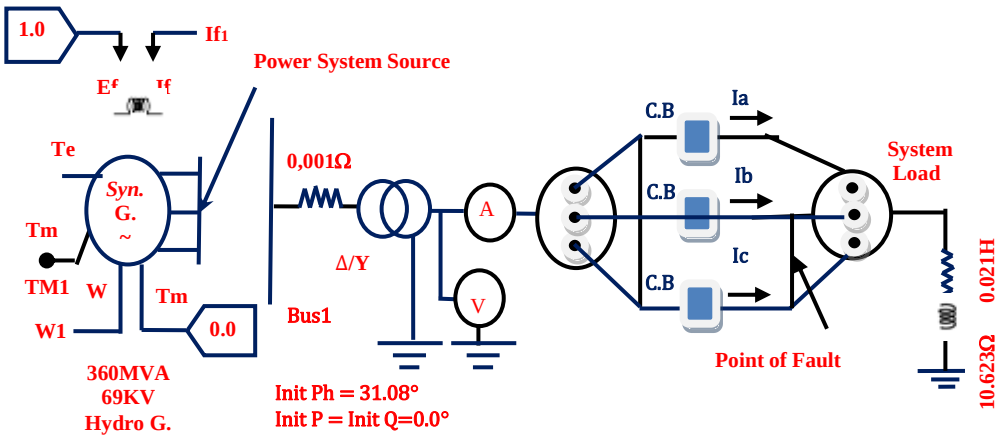


Figure (9) Diagram of a Tie-Line with A source & Load & Point of Line to Line Fault in the System.

Table (2) shows the decrease in source impedance and incremental FCL impedance needed to limit to 40kA, depending on percentage increase in generation.

Table (2).

Generation Source	Fault Current If (KA)	Equivalent Source Impedance Zs (Ω)	Impedance to be Added Za ((Ω)
Existing Generation	34.5	$Z_s = \frac{V}{I_f} = \frac{69KV}{34,5KA} = 2\Omega$	Non
25% Increase Generation	43.125	$Z_{s1} = \frac{V}{I_f} = \frac{69KV}{43.125KA} = 1.6\Omega$	Non
50% Increase Generation	51.75	$Z_{s2} = \frac{V}{I_f} = \frac{69KV}{51.75KA} = 1.34\Omega$	0.2
75% Increase Generation	60.375	$Z_{s3} = \frac{V}{I_f} = \frac{69KV}{60.375KA} = 1.12\Omega$	0.333
100% Increase Generation	69	$Z_{s4} = \frac{V}{I_f} = \frac{69KV}{69KA} = 1\Omega$	0.43

Suppose the generation to this line increased by 25%. We then have a short circuit current of 43.125KA, Zs = 1.6Ω. Theoretically, no series impedance needs to be added to limit fault current. However, since the FCL is configured to limit 50KA line to ground fault, an impedance of 0.2Ω is inserted anyway (see table1). This limit

fault current to 34.5KA. This is because the FCL limiting impedance inserted was based on the worst- case scenario which is the line-to- ground faults. Fig.10 shows the vector diagram of impedance for line-to-line fault case.

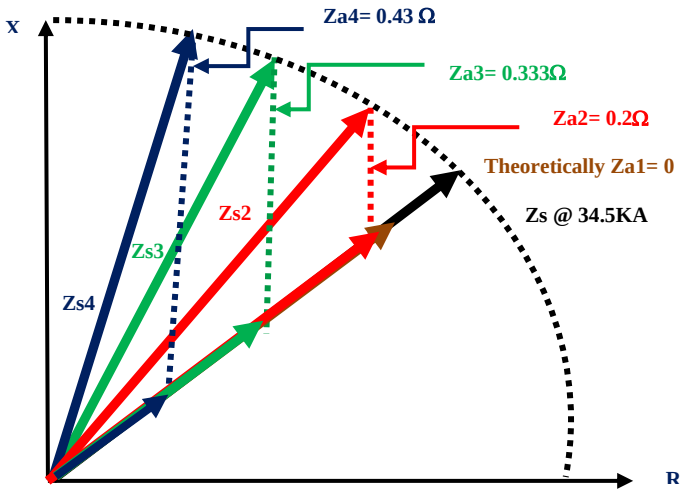


Figure (10) shows the vector diagram of impedance for the values of fault current shown in Table(2).

PROPOSED FAULT CURRENT LIMITER

FCL's are modular series blocks of AC switches. Each AC switch or level is capable of turning OFF and transferring short circuit current to a parallel impedance by itself. The required FCL impedance to be inserted can be broken down into a number of smaller blocks of inductors in series, each of which is in parallel to the level AC switch.

Each level consists of a limiting inductor that has a solid-state switch in parallel that is turned ON to behave like a transmission line and turned OFF during fault to transfer the short circuit current to the inductor. The level also has 4 parallel varistors to clamp overvoltage across the switch during turn-off.

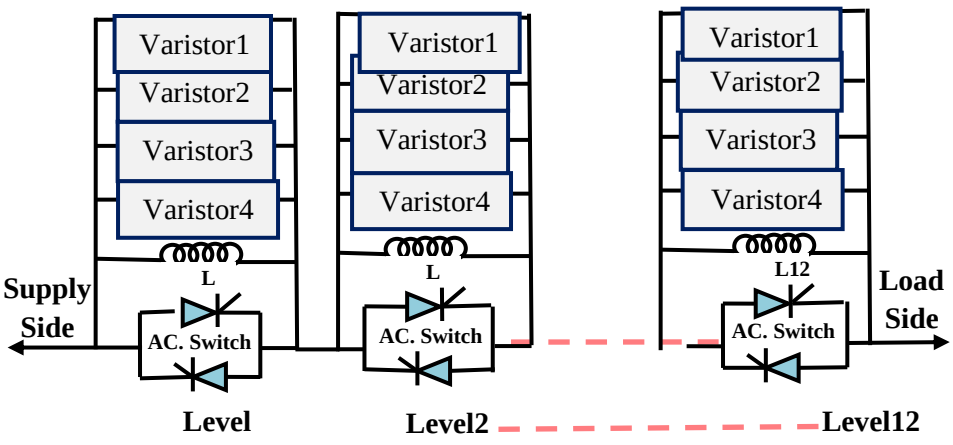


Figure (11) Show Modular Level Based Solid State Fault Current Limiter.

For each level, we look at the varistor's ability to clamp at a certain energy rating. Consider the case if there is 100% increase in generation that means from the above table that we need to insert 0.5Ω or 1.59 mH into the system. If we fix the number of levels at 12, then the inductance per level is 132.6 µH. In order to justify the amount of levels needed, we look at the voltage across inductor and see if the varistor ratings can match this. Each varistor has a rating of 3800J at 2ms and a clamp voltage of 3200V at 6000A. Therefore,

time taken to clamp during turn-off of 6000A is: t = $\frac{132.6\mu H}{3200V} * 6000 = 248.625\mu s$

energy during turn-off is: $E = P_{each\ varistor} * \quad t = \frac{6000A}{4} * 3200V * 248.625\mu s =$ 1192.8J at 248.625μs., which is well within the ratings of the varistor.

Since it is desirable to have redundancy in the system, in case of failed levels in the FCL system, we choose to have N+ 4 redundancies. This will round off the total number of levels to 16. It then follows that at different increases in generation, one or more installed levels might well be shorted by replacing the level inductor by a bypass, while still maintaining the ability to introduce sufficient impedance to limit to 40kA let-thru current. We can then have, for a 16 level FCL installed at a substation, the following amount of levels to be functional for effective current limiting as shown in Table (3) below.

Table (3).

Generation Source	Fault Current IF (KA)	Impedance to be Added (Za)Ω or equ. inductance	Functional Levels Required	
Existing Generation	40	Non	Non	Non
25% Increase	50	0.2Ω or 636.6µH	$\frac{636.6\mu H}{132.6\ \mu H} = 4{,}8$	5+4
50% Increase	60	0.333Ω or 1059 µH	$\frac{1059\ \mu H}{132.6\ \mu H} = 7.98$	8+4
75% Increase	70	0.43Ω or 1368 µH	$\frac{1368\ \mu H}{132.6\ \mu H} = 10.5$	11+4
100% Increase	80	0.5 or 1591 µH	$\frac{1591.5\mu H}{132.6\ \mu H} = 12$	12+4

DESIGN ANALYSIS & SIMULATION

To illustrate the operating principle of SSFCL, a simulation model is simulated using Matlab/Simulink . Simple models have been used.

FAULTS ON A DISTRIBUTION FEEDER

Many of the power quality problems that customers experience are the result of faults and disturbances on adjacent feeders on the same distribution bus. The use of SSFCLs on feeders can greatly alleviate this problem and enhance power quality in areas such as premium power parks. The following results are derived from computer

simulations for faulted conditions on the circuit shown in Figure (12). The circuit model is shown below the one line representation of the distribution feeder. This circuit was derived for simulation purposes to demonstrate the operational characteristics of the solid state breaker with current limiting proposed here.

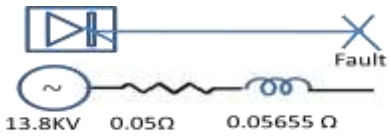


Figure (12) one line representation of the distribution feeder.

The most common fault that occurs on a distribution feeder is the single line to ground fault. A fault is simulated for this circuit and is shown in Figure (13) for a single line to ground fault on phase A of this circuit.

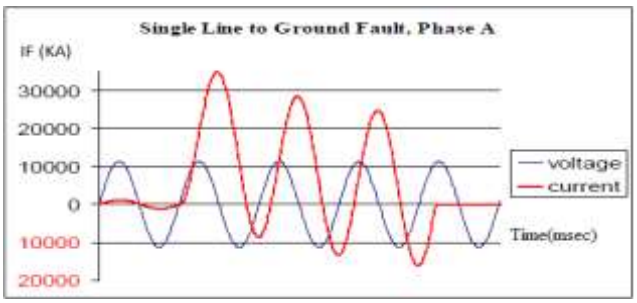


Figure (13) Single Line to Ground Fault, Phase A, Conventional Breaker.

Figure (13) shows the fault as interrupted by a conventional breaker after approximately three cycles after the fault. The fault was imposed after a zero crossing of the rising waveforms to generate the maximum asymmetrical currents. The asymmetrical current here is approximately 34 kA. The line to neutral voltage of a 13.8 kV feeder is shown for reference purposes.

The operation of the SSFCL for the same fault conditions as shown in Figures (12 and 13) is shown in Figure (14) using the same scale. An arbitrary selection for peak fault current limiting was made at 5 kA. Actual peak fault current limiting would depend on the circuit conditions.

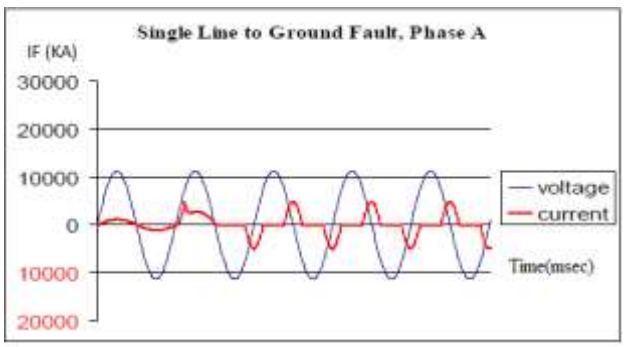


Figure (14) Single Line to Ground Fault, Phase A, SSFCL.

Shortly after the onset of the fault, when the current reaches the preset 5 kA level, the SSFCL that are conducting the fault current are force commutated and a current limiting impedance is switched into the circuit until the first zero crossing of the current occurs. A current limited fault is then maintained for downstream coordination for some predetermined period by phase controlling the SCRs as shown in Figure (14).

Breaker Comparison	
Conventional Breaker	**Solid State Fault Current Limiter**
Fault's current is almost interrupted with CB application approximately three cycles after the onset of the fault.	SSFCL can limit the fault current by series impedance is inserted for first half cycle.
Asymmetrical Fault Current = 34KA	Asymmetrical Fault Current = 34KA peak fault current limiting = 5KA (selective depend on the circuit conditions
Status post the fault, All three phases interrupted	Status post the fault, Other 2 phases uninterrupted

NEW INDEPENDENT GENERATION

To illustrate this situation, a computer simulation of an electrical network and the effect of new generation could have on it has been conducted. Figure 3 is a one line diagram of an electrical network to be analyzed for the effect of new generation and the SSFCL application. The system consists of an infinite source, a transmission line, a substation bus, and a distribution feeder. Under existing conditions, fault current for the fault shown is approximately 40 kA, peak asymmetrical.

Assume 50% increase in generation, the asymmetrical fault current has risen to 60 kA as shown in fig. 15 and could result in the feeder breakers and other equipment originally installed being considerably under rated and will need to be replaced with adequately rated equipment. Depending on the size of the network and the number of connections effected, this could be a substantial expense.

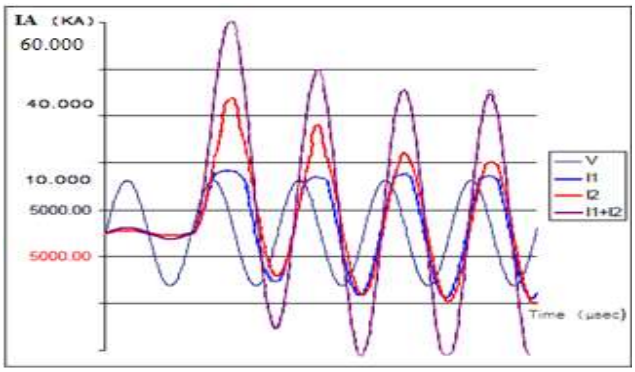


Figure (15) fault currents with 50% New generation and conventional breakers.

An alternative solution to the problem of equipment fault current withstand capabilities after new generation is interconnected into the system in locations that were previously unplanned, is to install a SSFCL with current limiting along with the new generation. Figure 16 show that but with a SSCL installed instead of a conventional breaker at the interconnection point.

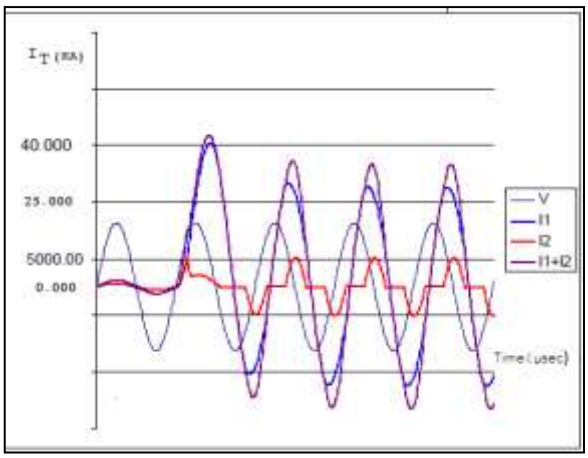


Figure 16, fault currents with 50% New Generation and SSFCL.

CONCLUSIONS

The fundamental challenge of Fault Current Limiters design is to simultaneously realize two conflicting objectives: good electrical performance and low cost. Presence of DG increases fault current levels and lead to protection problems.. Utilities usually predict how much fault current exists in the line and can forecast its increase over a period of time. By controlling the amount of impedance introduced in the line, we can say that a modular level based FCL can insert required impedance depending on existing fault current conditions on the line. This would reduce the number of levels needed to limit current. Additional levels can be incrementally added whenever line

conditions change that reflect higher short circuit current values. The result is a lower cost system that is smaller and has acceptable power loss (only switching loss).

The simulation results have shown that during the post fault period, the current is almost interrupted with CB application; which means that the load is no longer fed. On the other hand, the FCL will only limit the fault current to an acceptable value and the load will still be fed. This will therefore avoid multiple current interruptions or a huge variation of current within the power transformers. It is concluded that with FCL application, the life time of the power transformers & other component in T&D systems can be extended than using CB since they no longer undergo sudden variations (interruptions) of current each time when the fault occurs.

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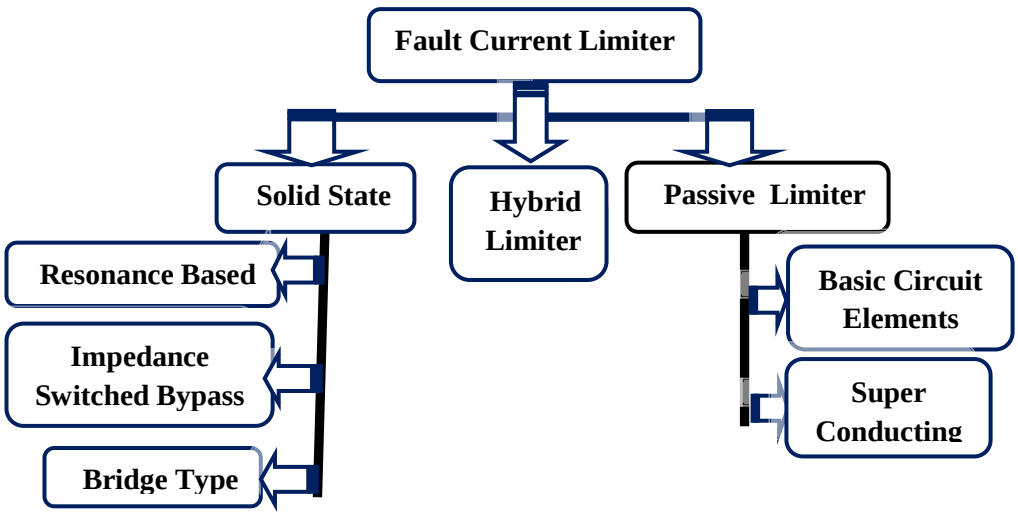
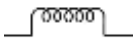
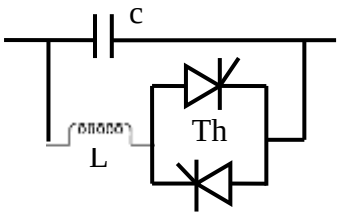
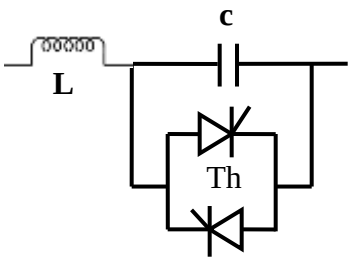
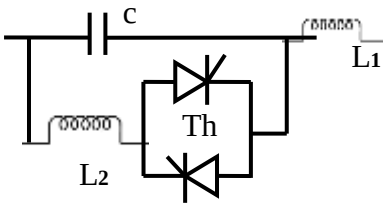
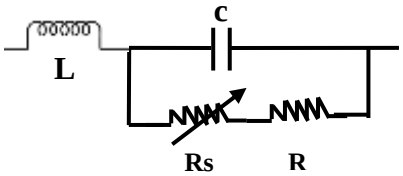
APPENDIX.A



A1 Categories of Fault Current Limiter.

A2. Passive, Solid State, Bridge & Hybrid Limiter

Type of Limiter	Circuit Diagram	Notes
1. Passive Basic Circuit Elements		The nature of the device reduces current by 2-3 times. Well research has disadvantages like lag pf. Voltage drop. Advantages are cheap, low maintenance.
2- Solid State Resonance Based Shunt Type		Steady State Th = OFF, C provides series comp. Fault State Th = ON, ZL > ZC = Limit Current $Z_{FCL(NOR)}=\frac{-J}{\omega c}$ $Z_{FCL(FLT)}=\frac{J\omega L}{1-\omega^2 Lc}$
Series Type		Steady State Th = OFF, L,C tuned for z = 0 and C provides series comp. Fault State Th = ON, C= shorted, L=> limit current. $Z_{FCL(NOR)}=J\omega L-\frac{J}{\omega c}$ $Z_{FCL\ (FLT)}=J\omega L$
Shunt Series Type		Steady State Th = OFF, L,C tuned for z = 0 and C provides series comp. Fault State Th = ON, C= shorted ,L=> limit current. $Z_{FCL(NOR)}=J\omega L-\frac{J}{\omega c}$ $Z_{FCL(FLT)}=\frac{J\omega L_1}{1-\omega^2 L_2 c}+J\omega L$
LC Resonant Link		Steady State; As before Fault State; Rs = saturable reactor which will operate when Vc reaches a set value. At sat $z_{rs} < z_{\circ}$ and L will limit current. R is used to smooth sub harmonic osc. Tested; 23kv,Rs shows abnormal behavior because of sat.curve.
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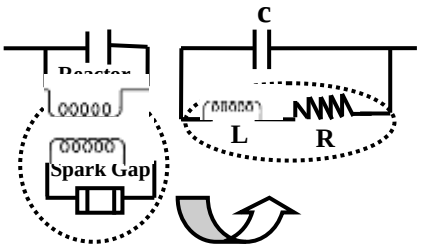
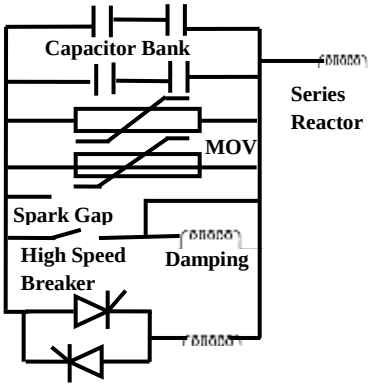
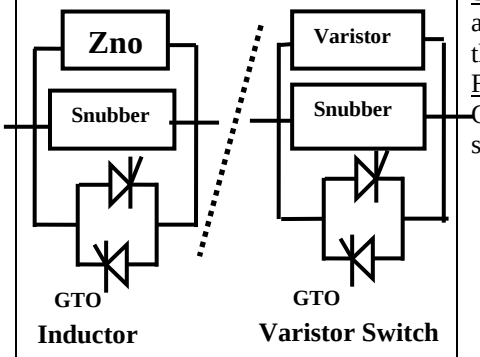
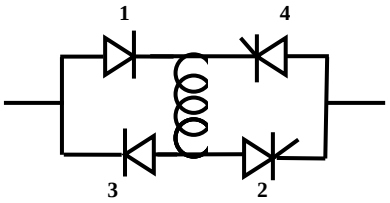
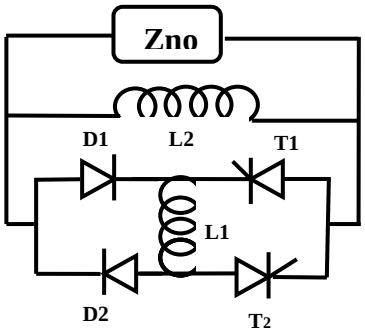
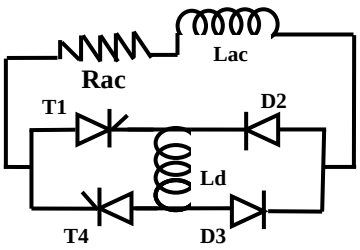
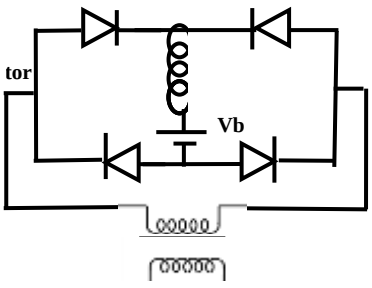
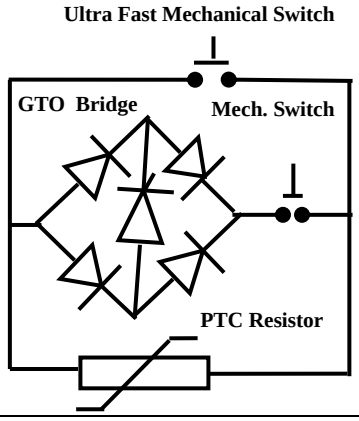
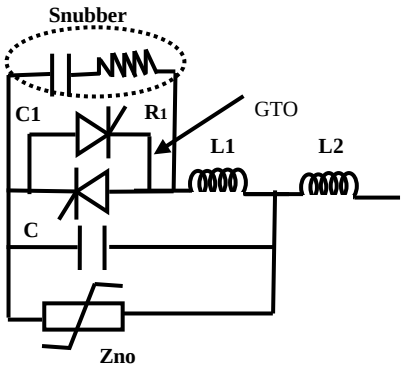
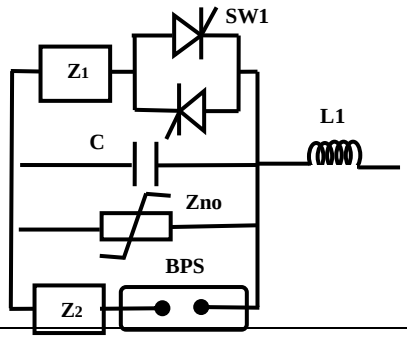
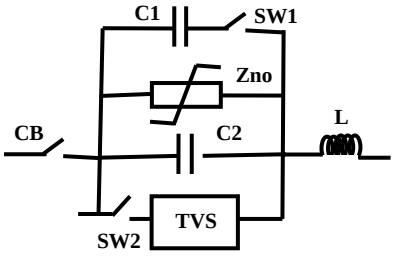
Spark Gap		Steady State; Vc and Vspark < < Vsys, no FCL effect. Fault State; $V_\circ$ and Vpri are high and spark breakdown happens resulting in Eqv ckt shown. Tested; 46% current reduction
Multi Bypass Series		Useful for EHV levels because of the sophistication of the device.
Impedance Switched Bypass		Steady State; GTO work in altemate half cycle to provide the low impedance path. Fault State; gating signals to the GTO are stopped and L can be seen in the circuit.

Type of Limiter	Circuit Diagram	Notes
3-Bridge Type Regular		Steady State; All thyristors are gate on and bias current estb in L . Fault State; since I cannot change inst. in L, current is limited. At that same time T1 and T3 are switched off so that current can flow out of the inductor through T4 and T2 untile fault cleared.
IGCT		Steady State; All diodes and **IG**CT are conducting and bias current estb in L . Fault State; switch off T1 and T2, current will flow through D1 and D2 and excess through L2. Zno is used for over voltage Protection.
SFCL		Steady State; All diodes and thyristors are conducting and bias current estb in Ld . Fault State; switch off T1 and T4, current will flow through D2 and D3 and excess through Lac and rac. rac+Lac = Z load
DC Reactor Using HTS		Steady State; Vb provides the bias current to the reactor which flows through the two loops. All diodes are in conduction. Fault State;Load current becomes greater than bias current and two diodes are reversed, switching the fault current to the reactor

Type of Limiter	Circuit Diagram	Notes
4- Hybrid **Using Solid State Switch / Mech. switch** **GTO+ Mech. switch**		Steady State; All mech. switch and GTO is ON. Fault State; UF. mech. switch opens with μs. after commutation and opening of the top path,GTO are OFF, forcing the current through the PTC resistor. Mech. switch opens after GTO = OFF to prevent over voltage across GTO. Tested; 15kv,1Ka steady state current.
Series Compensation		Steady State; GTO is OFF, C carries the current and provides compensation. Fault State; GTO turns ON, L1 starts conducting. If L1 and C have proper parameters, a high Z can be seen in series with L2.
Series Compensation		Steady State; SW1, BPS are OFF, C1 provides series compensation. Fault State; SW1 quickly closes forcing the current through its branch and L1does the current limiting. Z1 is used to limit inrush current. BPS and Z2 act as back up for SW1. Zno is OV protection.

Triggered Vacuum		Steady State; TVS, SW2 are OFF. Fault State; TVS Will turn ON and bypass C1,L will limit current. Zno is used for OV protection and C2,SW1 act as series compensation.