Analyses of Space Vector PWM Inverter under Fault Conditions

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ABSTRACT

The Space-Vector Pulse Width Modulation (SVPWM) technique has become a popular pulse width modulation technique. In this paper, performance investigation of space vector PWM inverter feeding three phase R-L load under fault conditions are presented.

The common faults occurred in the power switches of Space Vector PWM bridge inverter, such as; open transistor and misfiring transistor. These faults are implemented, built to get experimental and simulation results. The time and frequency domain analyze has been used to compare and analyze different fault cases with the normal operation in SVPWM inverter.

The obtained results show that the model is accurate, applicable and gives a good identification, information and diagnostic rules for the different faults.

Keywords: SVPWM, Open Transistor, Misfiring, Fault Cases.

تحليلات تقنية المتجهة الفضائي لتضمين عرض النبضة لعاكس في حالات العطل

الخلاصه

أن تقنية تضمين عرض النبضة للمتجه الفضائي أصبحت أكثرتقنيات التضمين النبضي شيوعا.تم في هذا البحث العلمي تحليل اداء العاكس المعامل بالتقنية المذكورة اعلاه في حالات العطل اثناء تغذيته لحمل (مقاومة مع محاثة).أن منال أعطال الشائعة التيتحدثف يمفاتيح القدرة المستخدمة في قنطرة عاكس تضمين عرض النبضةللمتجه الفضائي وتسمى: الترانزستورالمفتوح،فشل في تحفيزالترانزستور.تم تطبيق هذه الأعطال للحصول على النتائج النظرية والعمليه.

استخدمت التحليلات في الحقل الزمني وحقل التردد لمقارنة وتحليل حالات الاعطال المختلفة مع حالة الحمل الصحيحة للعاكس. ان النتأئج المستحصلة بينت دقة النموذج وامكانية تطبيقه واضحت كذلك قاعدة جيدة للتعريف والمعلومات واسلوب تشخيص الاعطال المختلفة.

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INTRODUCTION

The design and control techniques of the inverter system have matured to a certain degree. However, many kinds of unexpected inverter faults occur so often in industry fields. The (VSI) contain semiconductor devices, which are rugged but suffer from failure due excess electrical and thermal stresses that are experimental in many applications.

This failure can categorized as many type of faults. Therefore, the knowledge and information about the faults behaviors are very important to system design, protection and fault tolerant control.

The inverter faults may influence the operation of the whole system. Also, in order to prevent the harmful influence as well as to enhance the reliability of the system, the fault detection and diagnosis are need [1].

In this work MOSFET inverter as shown in Figure (1).The mentioned faults may cause the drive system shut-dawn depending on the state of the system. However, the system can also keep operating under the fault since it doesn't always result in the incapability of system operation. Therefore, it may lead to the secondary faults such as thermal defects of the other switches, control circuit, winding and bearing faults of the motor and so on.

SPACE VECTOR REPRESENTATION AND SWITCHES ANALYSIS

Healthy case SVPWM theory and axis transformation are given [1, 2, and 3]. Any three-phase quantities can be represented by two axes frames, like (qd) axes which are a complex axis frame, q-axis represents quadrature real axis and d-axis represents direct imaginary axis. The transformation procedure can easily be done by the following formula [1, 2]:

$$\begin{bmatrix} Vq \\ Vd \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} \quad \ldots(1)$$

The resultant voltage space vector is given by:

$$V_{qd} = V_q + jV_d = \frac{2}{3}\left[\left(V_a - \frac{1}{2}V_b - \frac{1}{2}V_c\right) + j\left(V_b + \frac{-\sqrt{3}}{2}V_c\right)\right]$$

$$= \frac{2}{3}\left[V_a + \left(-\frac{1}{2} + j\frac{\sqrt{3}}{2}\right)V_b + \left(-\frac{1}{2} - j\frac{\sqrt{3}}{2}\right)V_c\right]$$

$$V_{qd} = \frac{2}{3}\left[V_a + a V_b + a^2 V_c\right] \quad \ldots (2)$$

Where, $\mathbf{a} = e^{j120^\circ}$ and $\mathbf{a^2} = \mathbf{e}^{-j120^\circ}$.

By applying the phase of different states in equation (2) phase and (healthy) state can be illustrated in Table (1),[1,2].

Fault cases

The phase and magnitude of the eight switching space vectors voltage for inverter transistor open circuit fault and inverter transistor misfiring fault have been deduced, and are given in Table(2) and Table(3) respectively.

Assumptions:

The switch sequence analysis of space vector PWM inverter for healthy and faulty cases given in Tables (1,2 and 3),where the corresponding voltage wave forms are also given. These has been deduced under the following assumptions:

1-The dead time and pulse width modulation switching are neglected.

2-The small deviation of the space vector voltage ΔV_a , ΔV_b and ΔV_c which may be existing the transient moment from healthy to faulty case has been also neglected.

3-The phase angle between phase voltage is assumed constant.

The whole tables have been illustrated the important differences between the healthy (normal) case and each faulty(abnormal) case.

Inverter Transistor Open-Circuit Fault (Sw1 off and Sw2 on)

In SVPWM inverters shown in Figure (1), it is assumed that the upper and bottom switches of a leg are operated complementarily and the switches are assumed ideal. Figure (2) shows the operating modes of switches at the normal condition (a-n) and the fault condition (a-f). Figure (2) (a-f) shows the case that the current polarity is negative.

If the upper switch of a leg, for example, switch S1 of leg a, is in fault, the corresponding phase voltage is decided by the polarity of the current flow and the switching pattern of switch S4. In this case, the current is decreased to zero quickly through the diode D4 and maintained at zero as shown in Figure (2) (a-f), and the other two phase currents are in opposite phase [2, 3].

INVERTER TRANSISTOR MISFIRING FAULT (SW2 OFF, SW1 ON)

Misfiring in the inverter MOSFET is one of the possible faults. The misfiring can be caused by a number of conditions such as a gate drive open circuit fault due to control circuit element deterioration or degraded pulse signal. The drive can operate for a considerable period of time, even with sustained misfiring. This fault stresses over switching devices and degraded output voltage waveform. The fault occurring at the peak of the output voltage has a more significant effect than that when the reference voltage is crossing zero [4, 5].

Malfunctioning of gate drive circuit can result the transistor misfiring fault. Since MOSFET S1 has now open-circuit fault, the phase (a) of the induction machine is connected to the positive decrial through the diode D1. The motor phase (a) voltages then determined by the polarity of current and the switching pattern of MOSFET S4. The phase voltage (V_a) will be clamped to the negative rail if stator current phase (a), (i_a) is positive. On the other hand, the phase voltage (V_a) will be clamped to the negative rail when transistorS4 is switch on, and then of the positive rail when transistor S4 is off and D4 is on, if (i_a) is negative.

The phase currents will be balanced sinusoidal with DC offset after the fault because the phase voltages (V_a, V_b, V_c) are balanced with the SVPWM modulation before and after the fault. The dc offset current in phase a will be equally divided between phase b and phase c. This conclusion is only valid under the assumption of magnetic linearity and infinite rotor inertia [6, 7].

SIMULATION OF PROPOSED SYSTEM

The performance analysis, system implementation, and simulation has established using PSIM program package.

The blocks and their parameters of modified SVPWM for MOSFET inverter under healthy and fault cases are given in the followings:

1) Space Vector Calculation.
2) Vector Location.
3) Time Interval Calculation.
4) A Voltage Source Inverter Motor Drive System with localization of faults configuration. Figure (3) shows the structure of SVPWM inverter, A single phase (full wave rectifier) is used as input power supply. The simulation program and the total explanation of the blocks and their parameter of the drive system are given in [8].

Figure (4) shows the VSI (Voltage Source Inverter) fed R-L load drive system with switching fault. The terminal "abc" is the input terminals to the load. A switch "Sw1"& "Sw2" simulates either open transistor circuit fault or misfiring transistor fault.

RESULTS AND DISCUSSION

A practical tested and simulation are performed for the SVPWM inverter fed R-L load drive in the healthy and fault cases. Data of the R-L load are: R=136Ω and L=80mH. The output parameters of full-wave rectifier are; C=880μF, L=16mH and AC supply voltage is 220 volt with respect to the rated frequency (50Hz).The bridge inverter consists of six MOSFET transistors. The value of modulation index is 90% for all cases.

The following possible states are experimentally tested and compared with the simulation results.

1) Healthy
2) Open MOSFET fault.
3) Misfiring MOSFET fault.

The whole operation points of the results have been taken at steady state condition. The fault occurs at time equal to 0.4sec for all cases.

Phase current analysis

The time and frequency domain of phase current for 3-phase inverter fed R-L load are investigated and analyzed. All Figures indicated by (A) represent experimental values while all Figures indicated by (B) represent simulation results.

The time and frequency domain of 3-phase inverter current (Ia)is shown in Figure (5) for experimental and simulation healthy case.

Phase current of the other two phases (b) and (c) are approximately similar to the phase (a).

The presence of small DC and a little harmonics components in the current analysis shown in Figure (5) are due to the following reasons :

1) The three-phase output current inverter and the three phase load under tested are not perfectly balanced.

2) The dead-time of the MOSFET is not considered in the simulation program.

3) The variation of the voltage supply.

For more clearness the phase (a) can be named faulty phase which is connected to fault leg (A) of the bridge inverter, while the other phases (b) and (c) can be named unfaulty phases.

The time and frequency domain of 3-phase inverter current (I_a,I_b,I_c)are shown in Figure (6,7,8) for experimental and simulation open transistor case.

The time and frequency domain of 3-phase inverter current (I_a,I_b,I_c)are shown in Figure (9,10,11) for experimental and simulation misfiring transistor case.

From the current waveforms studies, it can be concluded that the most variation components at fault states are DC and the harmonics components which is nearest to fundamental (2nd, 3rd, 4th and 5th). The main effect is in the faulty phase (a) that the un faulty phases (b) and(c) besides the lower value of the fundamental in the faulty phase (a) than in the un--faulty phases (b) and (c) .

The DC component is increased in the faulty cases and the other harmonic components (2nd, 3rd, 4th and 5th) are also increased. The harmonic amplitude values from phase to phase are regularly varied.

According to the DC and harmonic components values are interaction between them, and with the fundamental values. These interactions depend on the type and location in addition to the priorities of the drive system.

Total Harmonic Distortion (THD)

The calculation of the THD for three- phase currents in experimental and simulation are given in Table (1.a,b,c) to healthy, open and misfiring cases. The THD of faulty phase current (I_a)have higher value corresponding to other two unfaulty phases (b and c).

CONCLUSIONS

The performance investigation of modern SVPWM inverter under fault condition is very important task. The most recent faults type, happened in the bridge inverter have been presented and analyzed.

1)Implementation and simulation method of SVPWM drive system using PSIM software for study of faulty cases has been developed. The results of simulation and experimental are consistent with theoretical studies and excellent , they indicate that the model is accurate and practicable.

2) Due to simulation and experimental results, the following important notes are concluded:

a. This is the most variation components at fault states are DC component and harmonics value which are nearest to fundamental (2nd,3rd,4th and 5th).
b. The highest effect is the faulty phase current that is connected to the faulty leg of bridge inverter.
c. The fundamental value of the current is clearly reduced in faulty case.
d. The nature and location of faults can be easily distinguished.

3) The proposed model can be extended to any inverter configuration types, using for any drive system. The model can be used with any type of switch like IGBT and GTO.

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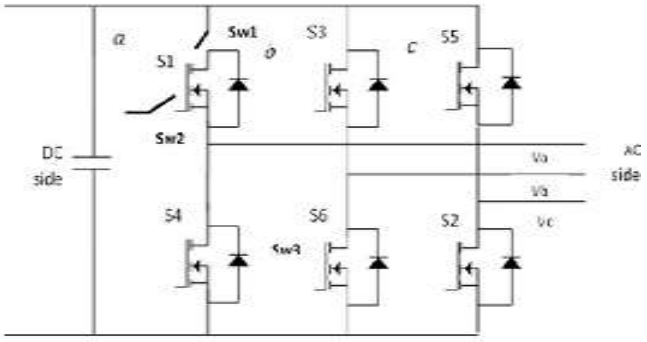


Figure (1)

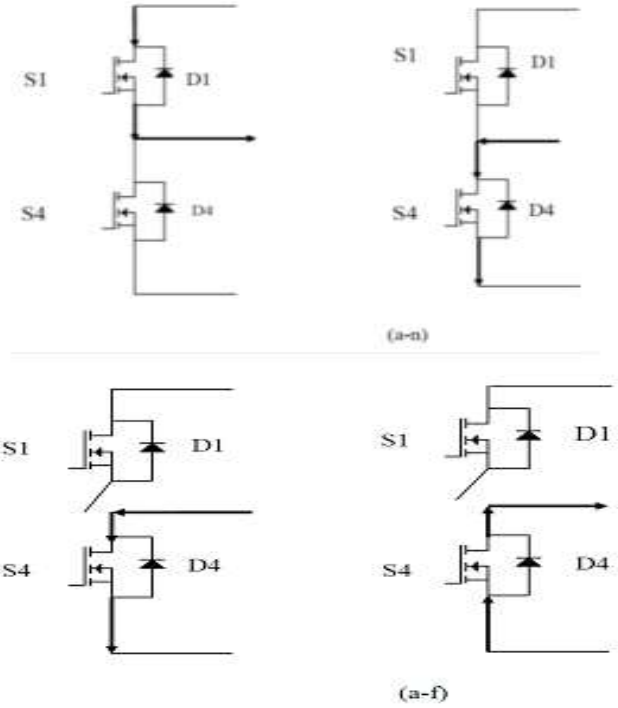


Figure (2)

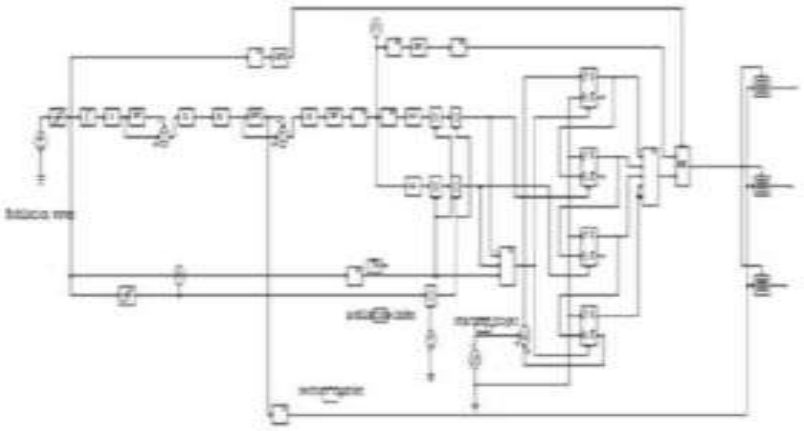


Figure (3)

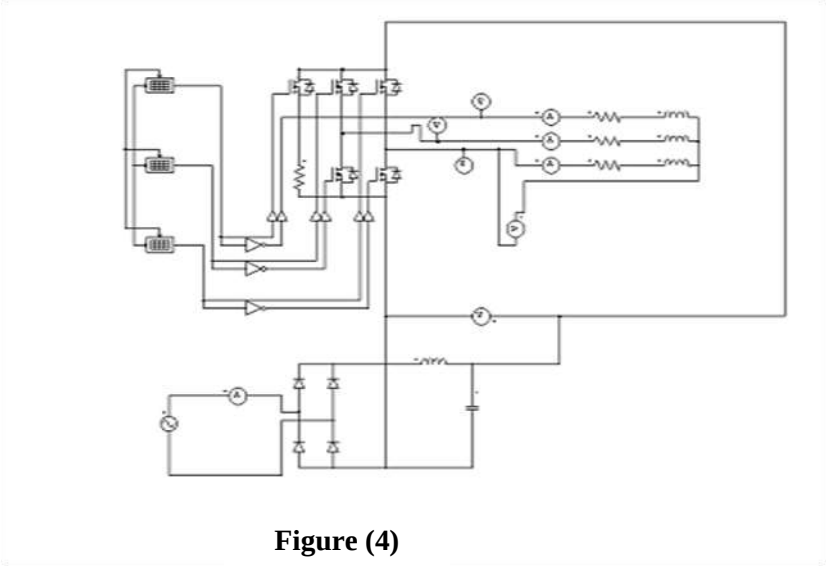
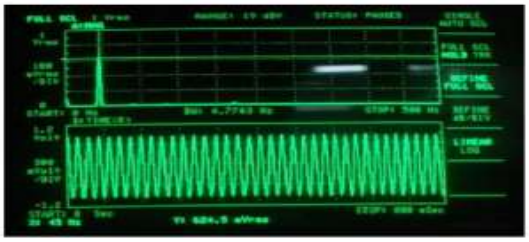
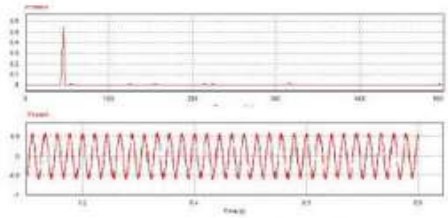


Figure (4)

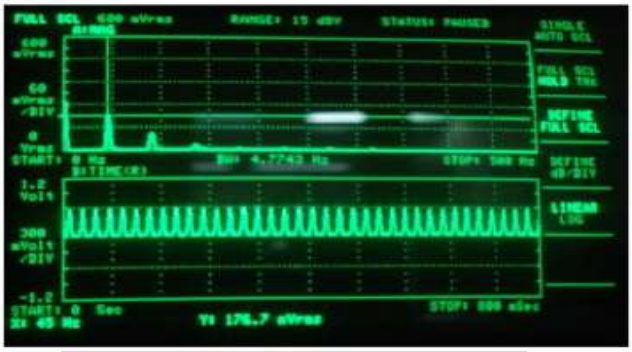


A-output current (healthy)

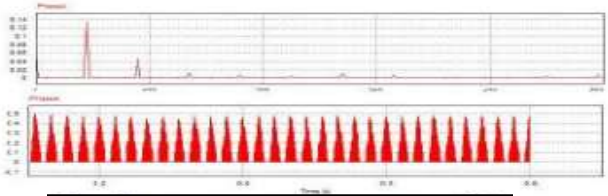


B-output current (healthy)

Figure (5)

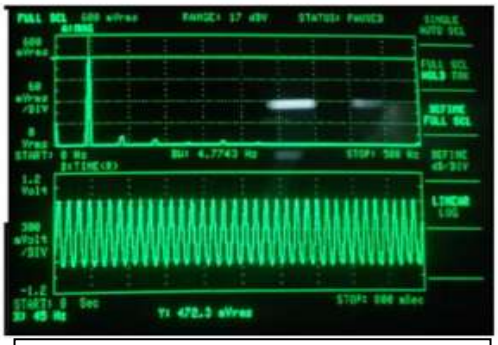


A-phase a current (open mosfet)

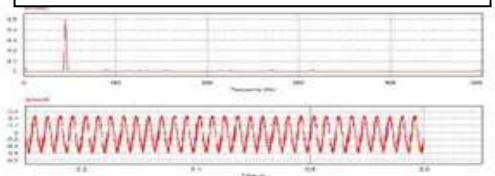


B-phase a current (open mosfet)

Figure (6)

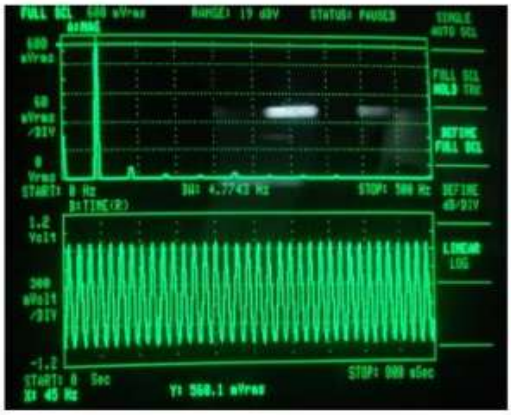


A-phase b current (open mosfet)

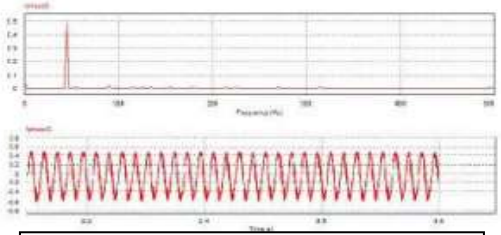


B-phase a current (open mosfet)

Figure (7)

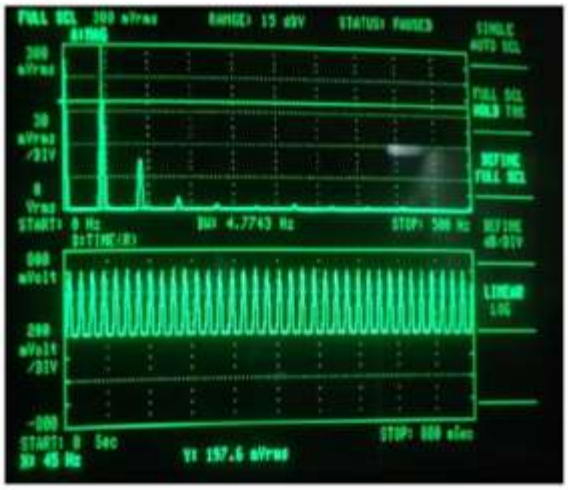


A-phase c current (open mosfet)

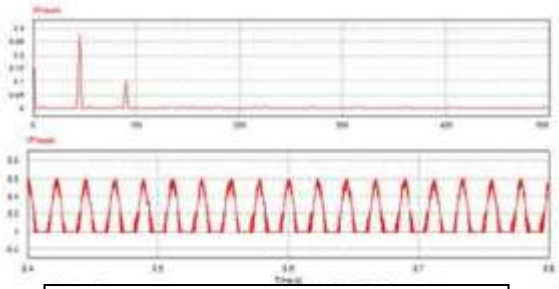


B-phase c current (open mosfet)

Figure (8)



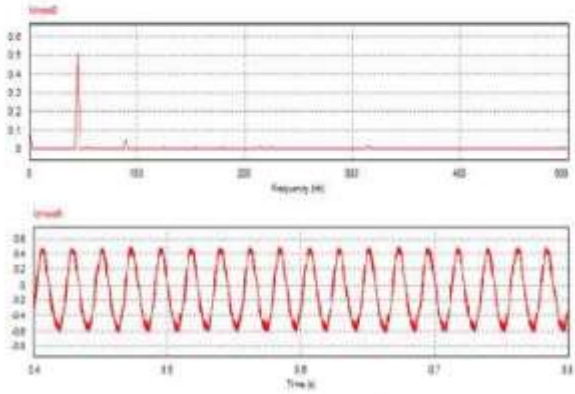
A-phase a current (misfiring)



B-phase a current (misfiring)

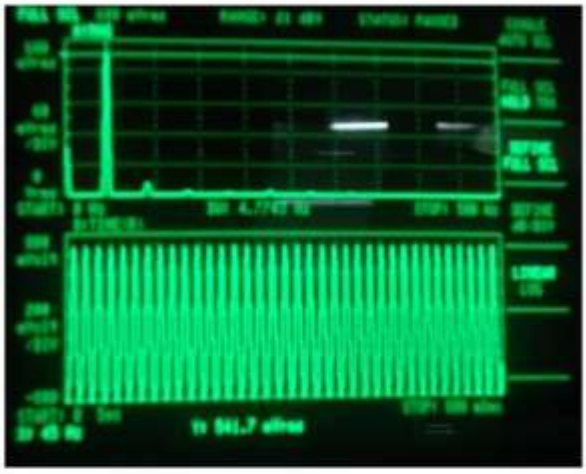
Figure (9)

A-phase b current (misfiring)

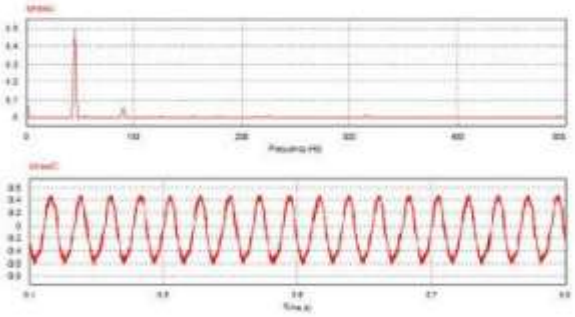


B-phase b current (misfiring)

Figure (10)



A-phase c current (misfiring)



B-phase c current (misfiring)

Figure (11)

Table (1) and voltage waveform (healthy).

SV switch	V_a	V_b	V_c
V_0(000)	0	0	0
V_1(100)	2/3V_d	-1/3 V_d	-1/3 V_d
V_2(110)	1/3 V_d	1/3 V_d	-2/3 V_d
V_3(010)	-1/3 V_d	2/3 V_d	-1/3 V_d
V_4(011)	-2/3 V_d	1/3 V_d	1/3 V_d
V_5(001)	-1/3 V_d	-1/3 V_d	2/3 V_d
V_6(101)	1/3	-2/3	1/3
V-(111)	0	0	0

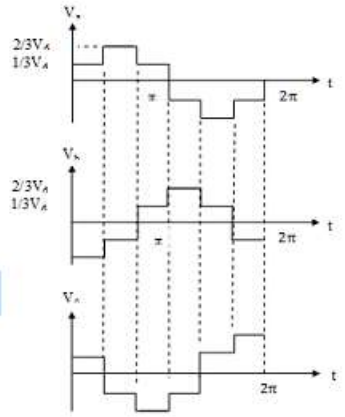


Table (2) and voltage waveform (open mosfet).

SV switch	V_a	V_b	V_c
V_0(000)	0	0	0
V_1(100)	2/3 V_d	-1/3 V_d	-1/3V_d
V_2(110)	1/3V_d	1/3 V_d	-2/3Vd
V_3(010)	0	1/2V_d	-1/2V_d
V_4(011)	0	0	0
V_5(001)	0	-1/2V_d	1/2V_d
V_6(101)	1/3V_d	-2/3V_d	1/3V_d
V-(111)	0	0	0

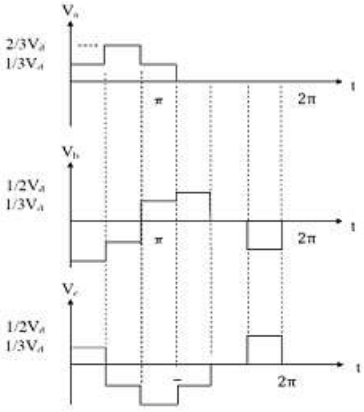


Table (3) and voltage waveform (misfiring)

SV switch	V_a	V_b	V_c
V_0(000)	0	0	0
V_1(100)	2/3V_d+Δv	-1/3 V_d+Δv	-1/3 V_d+Δv
V_2(110)	1/3 V_d+Δv	1/3 V_d+Δv	-2/3 V_d+Δv
V_3(010)	-1/3V_d+Δv	2/3 V_d+Δv	-1/3 V_d+Δv
V_4(011)	-2/3 V_d+Δv	1/3 V_d+Δv	1/3 V_d+Δv
V_5(001)	-1/3 V_d+Δv	-1/3 V_d+Δv	2/3 V_d+Δv
V_6(101)	1/3 V_d+Δv	-2/3 V_d+Δv	1/3 V_d+Δv
V-(111)	0	0	0

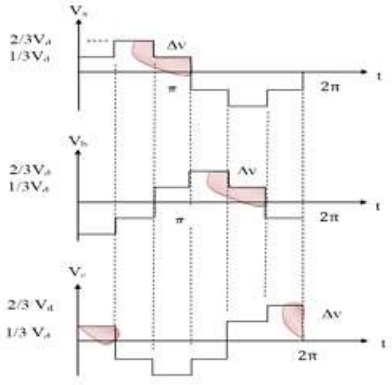


Table (4)

THD%	THD_{Ia}	THD_{Ib}	THD_{Ic}	THD_{Va}	THD_{Vb}	THD_{Vc}
healthy	10.19	8.24	8.52	14.26	11.95	10.053
Open transistor	153.4	27.15	32.7	133.3	22.6	23.3
misfiring	142	31.42	34.71	120.8	21.75	24.55