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Design and Improvement of a Reversible SISO Shift Register with Quantum dot Cellular Automata

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Abstract: Quantum dot cellular automata is one of the new nanotechnologies in computing systems having more potential for increasing speed, reducing the size and reducing power consumption in comparison with the current technology based on transistors. In this paper, we propose a novel reversible SISO shift register based on an optimized reversible D flip flop scheme in which the sequence of the flip flops is utilized to improve the evaluation criteria. The simulation results show that in comparison with previous works, the proposed reversible SISO shift circuits has been improved in terms of cell number, delay and area. In this design, the number of cells equals to 89, the area equals to 0.08 square micrometers, the delay is negligible, the number of inverter gates equals to three and the number of majority gates is eight.

Keywords: Reversible shift register, SISI, Quantum dot cellular automata, Quantum cost, Constant input, Additional output, Cell number and area.

1. Introduction

In 1965, Gordon Moore [1] predicted that the complexity of circuits approximately doubles every two years; since then, with the technology development, the size of transistors has become smaller and smaller; however, in nanometer transistors, many problems have arisen including short channel effects, leakage currents, variability issues, and reliability concerns. Besides, the size of transistors has become close to their quantum dimensions, which results in observing the effects of quantum particles in the circuits. To overcome these problems, it is required to use new technologies to devise a new generation of computers. One of the most important of such technologies is QCA (Quantum dot Cellular Automata) technology. QCA technology was first introduced by Lent et al. in 1993[2]. In the quantum-dot cellular automata (QCA) approach, binary information is encoded in the configuration of charge among redox-active molecular sites. In 1961, Landauer's Principle [3] stated that any operation performed by irreversible gates is always associated with a loss of energy, and this dissipation is due to information erasing in an irreversible process. In order to prevent this power dissipation, the circuit must be designed in a reversible manner [4]. Reversible circuits are divided into two categories: combinational and sequential circuits. In combinational circuits, the outputs at any moment only depend on the inputs at that moment. However, sequential circuits include memory elements, and their outputs at any moment depend on both the input at that moment and also the state of the circuit kept in memory elements. Less research has been carried out on reversible sequential circuits such as flip-flops, shift registers, and counters in comparison with combinational circuits [5,6]. In this study, shift registers are examined; a chain of flip-flops with a common clock pulse in which, upon asserting the active edge of the clock, the stored value in each flip-flop, which is available at its output, is transferred to the next flip-flop (the left or the right one based on the topology of the circuit). In this paper, we make improvements by replacing the gates and the quantum cost of each gate and the whole circuit, as well as the number of constant inputs, additional outputs in the final circuit of this problem,

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reducing the number of cells in clock0 to one cell, clock1 to two cells, clock2 to two cells, and clock3 to three cells so that we get a near-zero delay. This paper is organized as follows: In section 3, the related works (including reversible flip-flops and reversible shift registers) are reviewed. Section 4 and 5,discusses the design and optimization of the proposed reversible shift register and the achieved results are explained. Finally, the conclusion is given in section 6.

Basic concepts in QCA

Quantum cellular automata is a type of computing technology that is used in the construction of circuits in very small dimensions of the nano level, in which the cell in this technology consists of four holes and two electrons. Due to the repulsive force between the electrons, as a result, they are placed in the diameter of the cell and the farthest point relative to each other. It can be seen in Figure 2-1. In calculations, logical values zero and one are assigned to them respectively [6,7]. In calculations, logical values zero and one are assigned to them respectively [6,7].

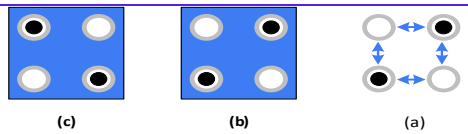


Figure 2-1

a) Tunneling path between quantum dots b) Logical one state c) Logical zero state

There are five types of cells in a QCA circuit. Input cell, output cell, normal cell and fixed cell with +1 and -1 polarity shown in Figure 2-2.

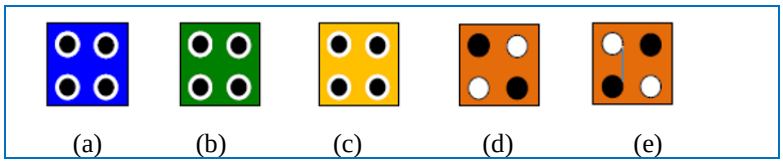
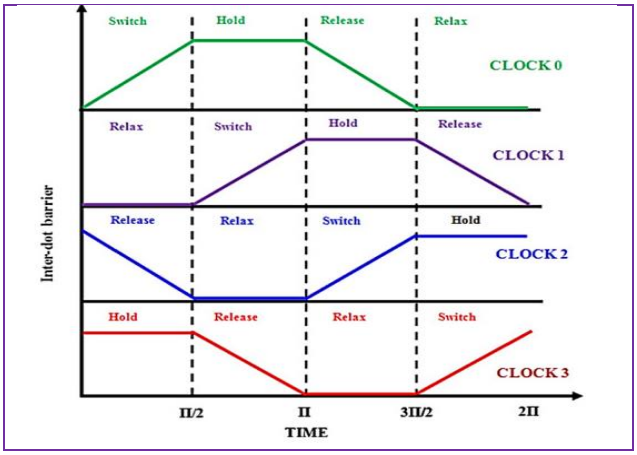


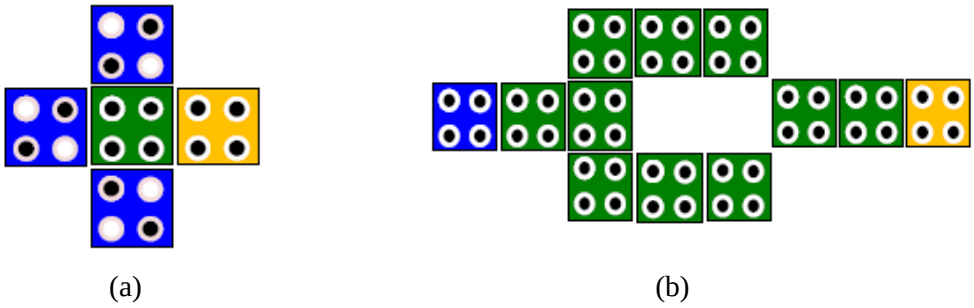
Figure 2-2. Display of cells

a) input cell, b) normal cell, c) output cell, d) fixed cell with 1 polarity, e) fixed cell with -1 polarity

The timing of QCA technology is different from CMOS technology, which only has two low and high states, and four timing regions are defined, which must be done at each stage of signal passage in one of these regions. These regions have a phase difference of 90 degrees, and all the cells of a region are under the same clock signal [8, 9]. Each clock includes 4 phases: Switch, Hold, Release, and Relax [10]. These phases are shown in Figure 2-3.



The basic logic gates in QCA are majority gate and inverting gate, all logic circuits in quantum cellular automata technology can be designed based on these two gates together and binary wire, Figure 2-4.



(a) (b)

Figure 2-4 shows a) majority gate, b) inverting gate

3. Related work

In this section, we first review and compare previous works on reversible D flip flops and then review the previous studies on reversible shift registers implemented and simulated by QCA cells.

3.1. The previous designs of reversible Flip flops with QCA Designer software

A flip-flop is a type of chip or digital integrated circuit that can act as a bit of memory. Each flip-flop contains two input signals, zero or one at the input base or bases, and we should not forget that each flip-flop has an output, a clock base, and two set and reset bases. Usually, in flip-flops, an inverse output of the main output is also taken into account so that the counters and registers can have the ascending and descending state. It should be noted that any change in the output state is simultaneously dependent on the pulse changes in the time base and the previous outputs. A flip-flop can be used as a memory element and is the most important element in sequential circuits. In this study, we examine D flip-flops previously designed in QCA software. In 2014, a D flip-flop was designed having 30 cells and an area equal to 0.03 square micrometers and a delay of 3 clock cycles [7]; however, there is no explanation about the number of majority gates and reversible gates. In 2017, another D flip-flop was designed in two schemes [9]. In the first scheme, the number of cells equals 74 and the area is 0.1 square micrometers and the delay is 1.5 clock cycles. In the second one, the number of cells is 28 and the area equals 0.02 square micrometers and the delay is 0.5 clock cycle, but there is no description about the majority and inverter gates for both of them [9]. In 2018, a D flip-flop was designed whose number of cells is 46, its area equals 0.05 square micrometers and its delay is 1.25 clock cycles. Again, the number of majority gates and the number of inverter gates have not been reported [8]. In 2016, a D flip-flop was designed, having 23 cells and an area

of 0.03 square micrometers and a delay of one clock cycle. It consists of three circuits of the majority gates and an inverter circuit, and we have used this flip-flop in this study [11]. A comparison of the above D flip-flops based on the evaluation parameters has been presented in Table 1.

Table 1 The comparison of D flip flops evaluation criteria measured in QCA software

Number of inverter gates	Number of majority gates	Delay	Area (um^2)	Number of cells	Reference	Year
-	-	3	0.03	30	[7]	2014
-	-	1.5	0.1	74	)I([9]	2017
-	-	0.5	0.02	28	)II([9]	2017
-	-	1.25	0.05	46	[8]	2018
1	3	1	0.03	23	[11]	2016

As it can be seen in this table, some designs are better than the others in one parameter and may be worse in other parameters. Therefore, based on the type of application, the appropriate type of the flip flop is selected for designing a given circuit.

3.2. The previous design of reversible shift registers with QCA Designer software

A designed flip-flop has a data input, a data output, and a clock input in a minimum state. If we connect the output of one flip-flop to the input of another flip-flop and repeat this for n times and connect the clock input of all these flip-flops to each other, then we will have an n-bit shift register. In other words, shift registers are a chain of flip-flops, and the arrangement of flip-flops in this chain determines the direction of the shift (right or left) [11,12,13]. The register that transfers its data to the right or left is called a shift register. Input and output data bits can be serially input or output to a shift register. Series means that data bits are entered or exited sequentially from left to right or from right to left. There is another mode where all the data are input or output together in one pulse, which is called parallel mode. According to how information is entered and exited, shift registers are divided into four groups: SIPO series input-parallel output, SISO series input-output series, PISO series parallel input-output, and PIPO parallel input-parallel output. In QCA Designer software, we must first select the appropriate flip-flop and then design the shift register according to the intended application. It is noticeable that each clock has four phases in QCA software, and it must be considered in the delay calculation. In 2017, using the QCA software, a three-bit shift register with D flip-flops was designed in one layer. For this design, the number of cells is 100, the area equals 0.065 square micrometers, and the delay is 0.75 clock cycles; it includes 11 majority gates and three inverter gates [11]. In 2014, using the QCA software, a three-bit shift register with D flip-flops was designed in one layer, and the number of cells is 150, the area equals 0.125 square micrometers, and there is no description about the delay and the number of majority gates and inverter gates [15]. In 2014, another three-bit shift register with D flip-flops was designed in one layer, and the number of cells is 142, the area is 0.122 square micrometers, and there is no description about the delay and the number of majority gates and inverter gates [16]. In 2018, a three-bit shift register with D flip-flops was designed in five layers, and the number of cells is 120, the area equals 0.03 square micrometers, and the delay is one clock cycle; the number of majority gates and inverter gates has not been reported [17]. In 2019, a three-bit shift register with D flip-flops was designed in one layer, and the number of cells is 115, the area equals 0.10 square micrometers, and the delay is 0.75 clock cycles; the number of majority gates and inverter gates has not been reported [18]. The comparison of the reviewed shift registers is given in Table 2.Table 2 The measurement of evaluation criteria for some SISO shift registers in QCA Software

Number of inverter gate	Number of majority gate	Delay	Area (um^2)	Number of cell	Reference	Shift register
3	11	0.75	0.065	100	]10[	2017
-	-	-	0.125	150	[15]	2014
-	-	-	0.122	142	[16]	2014
-	-	4	0.03	120	[17]	2018
-	-	0.75	0.10	115	[18]	2019

As it can be seen in this table, each design may be better than the others in one parameter and may be worse in other parameters. Therefore, based on the type of application, we use the appropriate type of the shift register should be used.

4- The design and optimization of a novel reversible shift register using the QCA Designer software

A shift register is a chain of flip-flops that have a common clock pulse and the output of each flip-flop is connected to the input of the next flip-flop and can shift the information stored in it by one unit to the left or right in each clock pulse. In the process of this transfer, one data is entered at the input and the last data at the output is lost, which is called the shift register system as a whole. Shift registers can be consecutive, in other words series or simultaneously (S), in other words parallel (P). In series mode, data is entered into

the shift register sequentially (SI) and in parallel mode, data is entered into the shift register simultaneously (PI). In other words, every time we apply a new data to the input, the data is moved to the output. In this research, SISO shift register is investigated to improve evaluation criteria. And the goal is to improve the evaluation criteria compared to the previous works in the SISO shift register. In this study, a novel Serial-In-Serial-Out (SISO) shift register is designed and simulated in QCA Designer software version (2.0.3) using the settings of Table3.

Table 3 Software settings

Value	Parameter
128000	Number of samples
(nm) 65	Radial effect
(nm) 11/5	Layer distance
1000	Most repetitions in sample

In our proposed 3-bit shift register, we have utilized the D flip flop proposed in [11] as a base and modified it for the first and the second flip flops so that the number of cells and the area have been decreased. This flip flop uses three majority gates and one inverting gate. Figure 1 shows the structure of it. Its number of cells is 23, its area is 0.03 micrometers and the delay is one clock cycle.

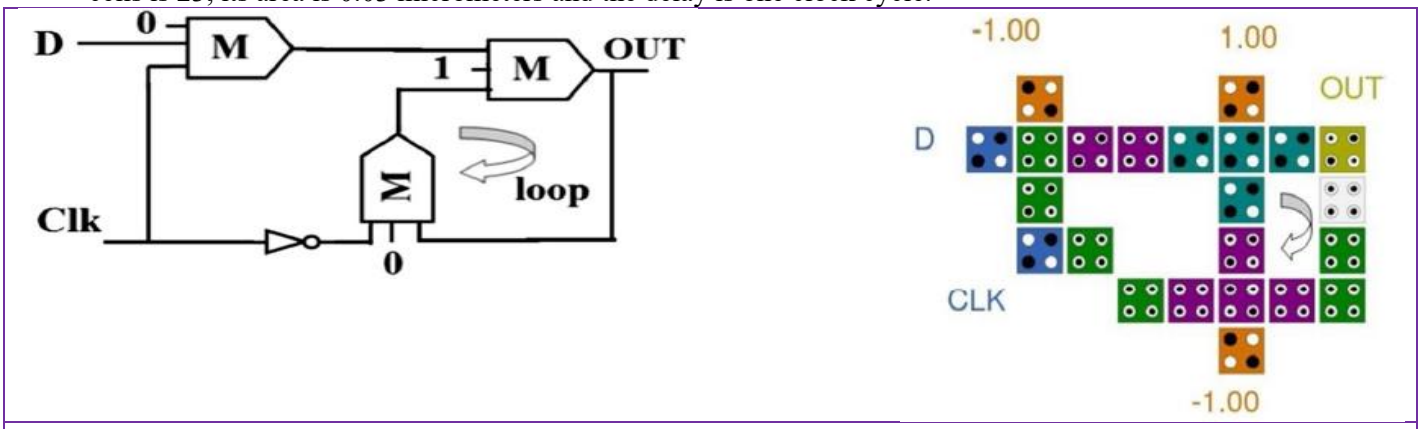
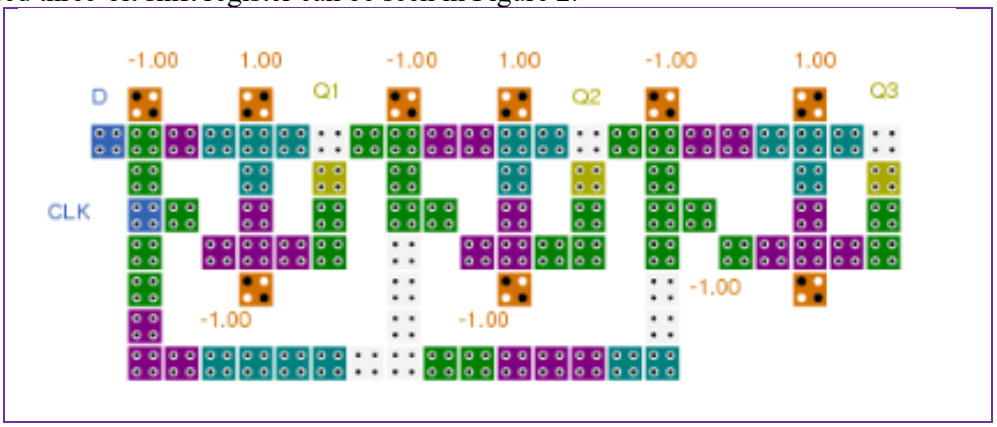


Fig.1 The Design of D flip flop in QCA software [11].

Our modifications in this flip flop have been made in such a way that the flip flop characteristic table has no change but evaluation criteria have been improved. As stated, the changes have been applied to the first and the second flip flops and the third flip flop is the same flip flop proposed in [11]. The final design of our proposed three-bit shift register can be seen in Figure 2.



(a)

(b)

Fig.2

(a) The proposed design of a three-bit shift register in QCA software

(b) The Design of a three-bit shift register in QCA software [11]

The simulation results of the proposed three-bit shift register in QCA software can be seen in Figure 3 (a).

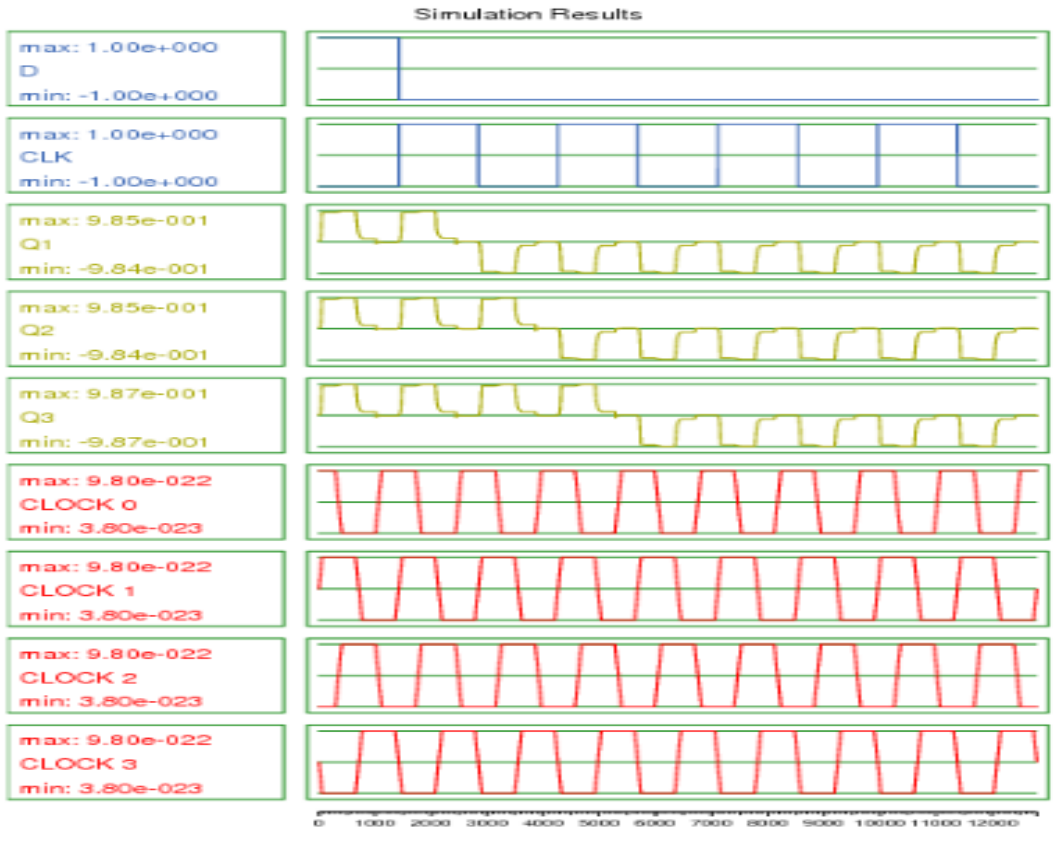
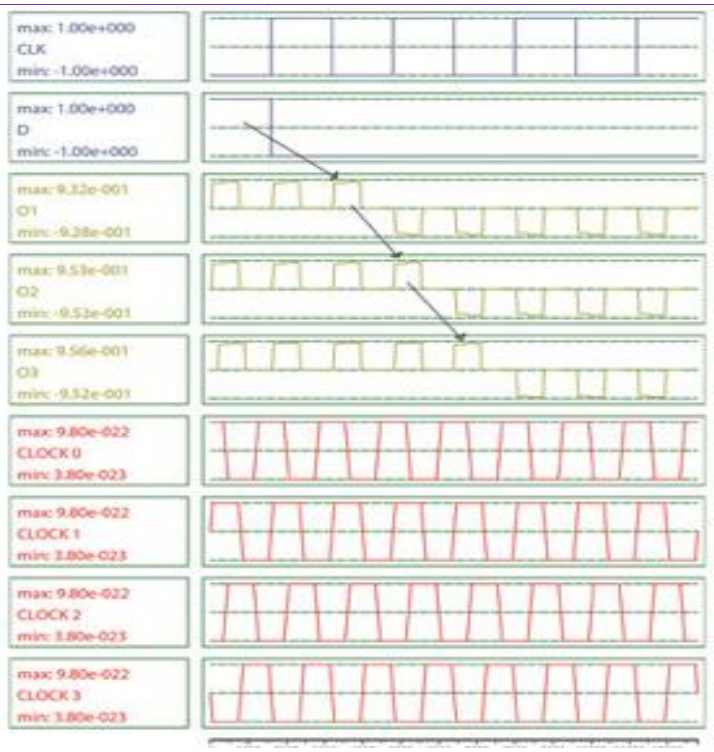


Fig.3

(a) The simulation results of a three-bit shift register in QCA software



(a) The simulation results of a three-bit shift register in QCA software[11]

In Table 4, the simulation results have been compared with the previous works. It can be seen that in our proposed design, the delay and the number of cells have been improved compared to the shift register in [17], but because this shift register was designed in five layers, it has smaller area than our proposed shift register that is designed in just one layer. It is noticeable that, in comparison with shift registers proposed in [15,16,18] all criteria have been improved in our design.

Table 4 The comparison of SISO shift register in QCA software with the proposed design

Number of inverter gates	Number of majority gates	Delay	Area (um^2)	Number of cell	Reference	Shift register
3	11	0.75	0.065	100	[11]	2017
-	-	-	0.125	150	[15]	2014
-	-	-	0.122	142	[16]	2014
-	-	4	0.03	120	[17]	2018
-	-	0.75	0.10	115	[18]	2019
3	9	0	0.08	89		Our proposed design

5- Results

In this study, the SISO three-bit shift register circuit is designed with QCA software, and the evaluation criteria have been improved compared to previous research in the number of cells and area, but it should be noted that there is a trade-off between the evaluation criteria, which we consider. Different designs can be used for the type of application that we want in the circuit, and in fact, the type of efficiency of the circuit determines for us which design to use for our circuit. In this research, we have reached the evaluation

criteria in terms of the number of cells to 89 and the area to 0.08 micrometer square, zero delay, and the number of reversing gates three and the majority gate eight. And the important point is that this technology is theoretical and has not yet reached practical use. It is hoped that with more detailed investigations in this technology, it can be replaced by CMOS technology, and currently, the most fundamental limitation for implementing this technology is in its construction. In order to realize an improved reversible circuit, we must approach the evaluation parameters to the best possible state. As the value of these measuring criteria decreases in a design, we will have a more improved circuit, and depending on the application of the circuit, the priority should be specified. According to the proposed new technologies and recent successes in the implementation of the logic circuits of quantum dot automata cells, it is considered a very suitable alternative to CMOS in VLSI circuits, and by using QCA-based technologies, it will be possible to build processors with low power loss and higher speed.

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Conflicts of Interest: The authors declare no conflict of interest

6- Conclusion

In this paper, a three-bit SISO shift register has been designed in QCA software, for which the evaluation criteria have been improved in comparison with previous works in terms of the cells number and the area. In our design, the number of cells equals to 89, the area equals to 0.08 square micrometer, the number of inverter gates equals to three and the number of majority gates equals to eight. Designing other types of shift registers with a different number of bits in single-layer or multi-layer can be considered as future work of this study. Design can also be implemented with Pro QCA software in order to calculate the power By calculating the total energy or loss during transportation, as well as the electrical voltage, and comparing the results with other designs

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