Structural & Electrical Properties of CdTe/Si Heterojunction Prepared by Flash Evaporation Technique

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Abstract

The present study is on the optoelectronic properties of CdTe/Si heterojunction photodetector made by deposition of CdTe by flash evaporation technique on clean monocrystalline phase of Si. Electrical and structural properties of grown CdTe film were investigated. The CdTe/Si junction exhibits fair diode rectification and the soft breakdown occurred at V_B>2 V. Dark *I–V* characteristics of the CdTe/Si photodetector are examined at room temperature.

Introduction

The interest in the growth of CdTe on Si systems results from the promising application of this system in optoelectronics integrating optic [1], hence this heterojunction was taken care of by studying its physical characteristics, whereas Kor and Panasjuk was the first to prepare this heterojunction in 1967, where they deposit of CdTe film at optimum substrate temperature on n- and p-type Si by vacuum evaporation and they studied I-V measurement of the junction [2,3]. However, the main interest in this junction started in the 1980s, when CdTe was used as a buffer layer for the growth of $Hg_{1-x}Cd_xTe$ for infrared detector application. The availability of high quality CdTe is generally recognized as one of the fundamental requirements for $Hg_{1-x}Cd_xTe$ epitaxy [1,4].

Experimental

The CdTe films have been prepared by vacuum flash evaporation technique with (1, 3, 5) μm thickness. We used CdTe granules made by reagent BDH chemical ltd. Poole England. It was 99.99% pure. After weighting the required amount of material, we put it into trough container connected to a vibrator. The molybdenum boat was mounted between two electrodes in the vacuum chamber. When the vacuum system reaches about the pressure (10^{-5}) mbar, then we turn on the heater of the substrate to reach the temperature (300^{o}C), then the

deposition processes by flash evaporation is carried out by instantaneous evaporation of the material by slow feeding with control the evaporation process by the vibrator.

The structure of the CdTe films has been examined by x-ray diffraction with CuK_{α}.The inter planer distance d(hkl) for plane was measured by using Braggs' law.

The electrical properties include C-V and I-V measurements in dark for samples deposited on wafer substrate with (In) electrode.

The current-voltage measurement in the dark of CdTe/n-Si heterojunction with different thickness of CdTe film. The dark current of heterojunction at bias voltage (0-2)V in the case of forward and reverse connections were measured.

The C-V measurement is done using LRC meter, from measuring the capacitance of CdTe/n-Si heterojunction with different thicknesses of CdTe films as a function of reverse bias (0-0.6)V, the value of (V_{bi}) can be found from the plots of the relation between $1/C^2$ and (V) as reverse bias. Then the interception of the straight line with voltage axis represents the built-in voltage.

Result and Discussion

The x-ray diffraction of CdTe films in different thickness deposited on Si wafers resulted in (111) orientation as shown in Figs. (1-3).

The x-ray diffraction pattern of CdTe films in (1μm-5μm) thicknesses has shown standard pinnacle which represents the reflectance x-ray from the plane (111) of CdTe film at diffraction angle (2θ=23.7 degree). It can be seen that the films have single crystalline structure as inferred from the one-diffraction peaks corresponding to the plane (111). Also the test shows existence of entity peak little strength representing the reflectance x-ray from the plane (111) of Si wafer at diffraction angle (2θ=28.3 degree). And returning to Bragg's law for the x-ray diffraction we can find amount of interplaner distance (d_{111}) that refers to the distance between two successive (111) planes.

For all CdTe films thickness the interplaner distance (d_{111}) can be used to calculate the lattice constant by using interplaner distance equation for square unit cell and the results are given in table (1).

Table (1) The lattice constant in the film in different thicknesses.

t(μm)	d(Å)	a(Å)
1	3.7	6.52
3	3.7	6.55
5	3.703	6.41

One of the important parameters of a detector measurement is a current-voltage characteristic, which explains the behavior of the resultant current with the applied forward and reverse bias voltage[5,6]. Fig. (4) show I-V characteristic for CdTe/n-Si heterojunction at forward and reverse bias voltage for different thicknesses of CdTe films. In general the forward dark current is generated due

to the flow of majority carriers and the applied voltage inject majority carriers which leads to decrease in the value of built-in potential, and decrease in the width of the depletion layer. The majority and minority carriers concentration is higher than the intrinsic carrier concentration ($n_i^2 < n_p$), which leads to generate recombination current at the low voltage region (0-0.3) V, because of the excitation electrons from V.B to C.B will recombine with the holes which are found in the V.B, and this is observed by little increases in recombination current at low voltage region. On the other hand, the tunneling current is represented at the high voltage region (>0.3), where there is a fast exponential increase in the current magnitude with increasing the voltage and this is called diffusion current, which dominates the process. In the reverse bias region the bias voltage leads to increase the width of the depletion layer which leads to decrease in the majority and minority carrier concentration in so much being lower than the intrinsic carrier concentration ($n_i^2 < n_p$). The reverse bias current which also contains two regions, in the first region (low voltage <0.3) the current slightly increases with increasing the applied voltage, and the generation current dominates, while at high voltage region (>0.3), the current is increasing progressively with the bias voltage or give soft breakdown voltage, and this behavior is general characteristic in the anisotype heterojunctions.

Also we can observe from these figures that the value of the current decreases many times with increasing of thickness of CdTe films, and that comes from the lattice mismatch between two materials, which would evolve defects and dislocations that have effect on mobility of charge carrier. Also these defects evolve allow energy levels within the energy gap, and these levels are within the depletion region and act as active recombination centers, and consequentially decrease current flow across the junction[7,8].

The inverse capacitance squared is plotted against applied reverse bias voltage for CdTe/n-Si heterojunction at different CdTe thickness film as shown in Fig. (7).The plots reveal a straight-line relationship, which means that the junction is an abrupt type. The intersection at $1/C^2 = 0$ of the straight line with the voltage axis represents the built-in voltage, also these figures show effect of the thickness of the film on the (V_{bi}) value, where we notice decreasing in (V_{bi}) value with increasing the thickness of the film, and that by increasing the defects concentration due to mismatch between the material, these defects act as recombination centers acting on extinguishing charge carriers and decreasing concentration on heterojunction sides, and that leads to decreasing the depletion region width and these results are in agreement with these of Farage and Raauf[9,10].

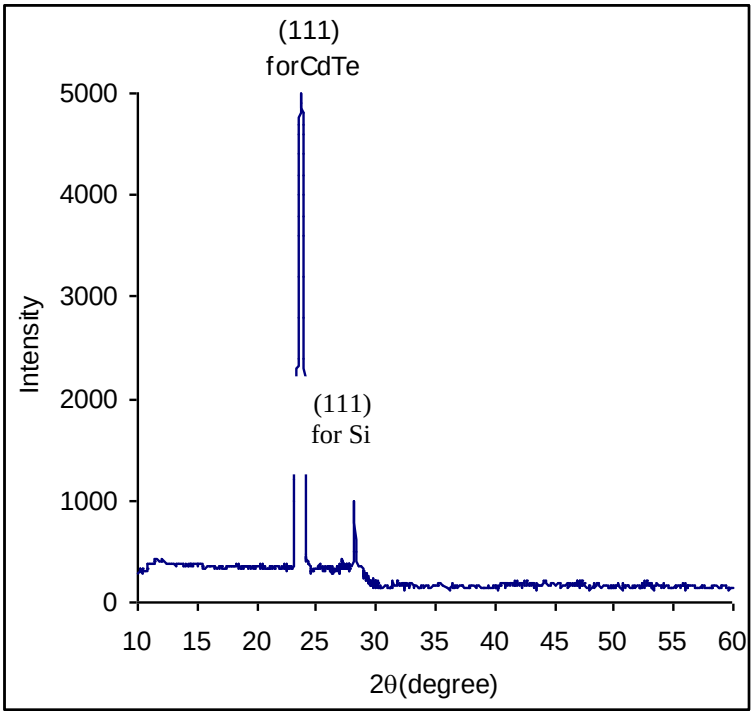

Fig.(1) The x-ray diffraction for t=1μm CdTe film.

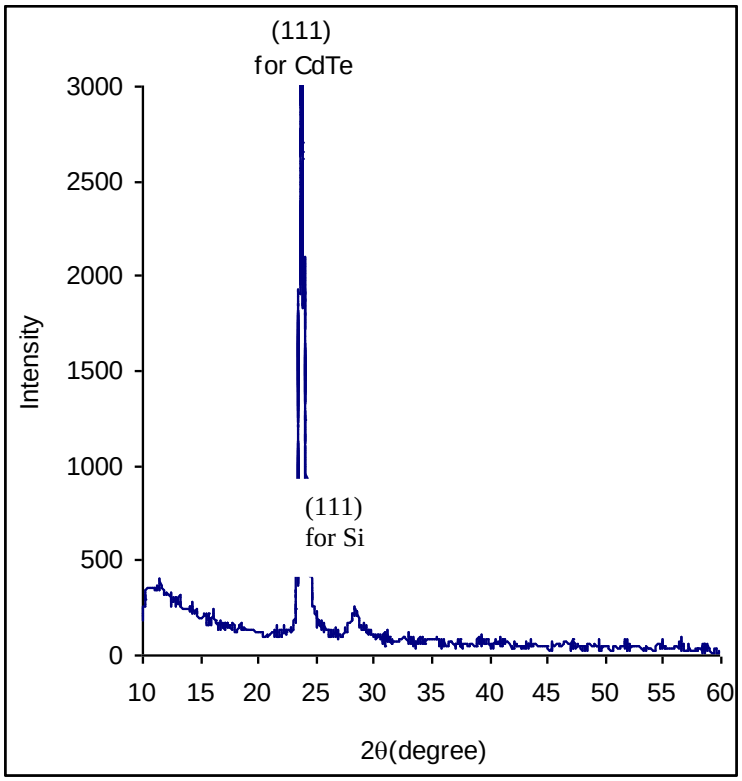

Fig.(2) the x-ray diffraction for t=3μm CdTe film.

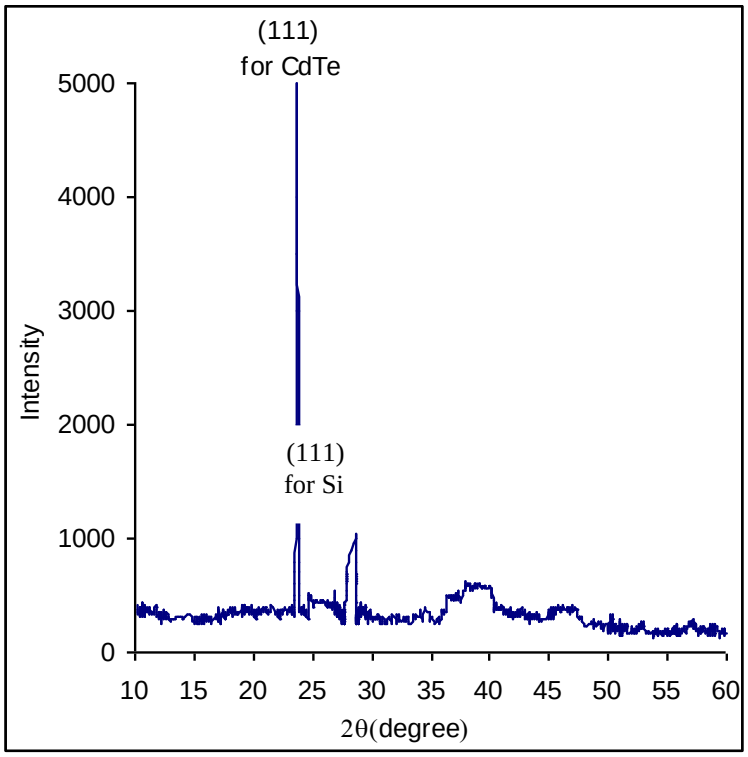

Fig.(3) the x-ray diffraction for t=5μm CdTe film

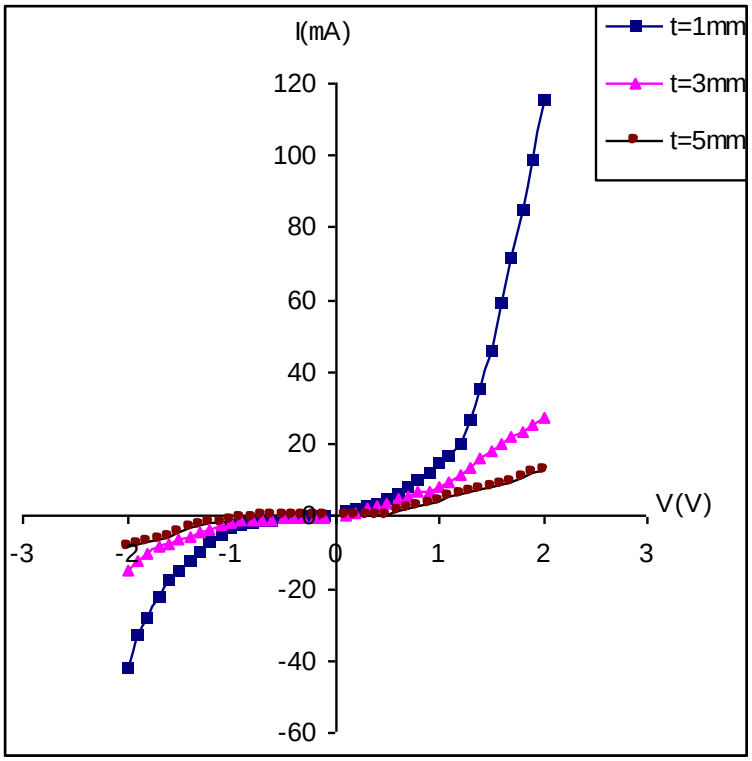

Fig.(4) the I-V characteristics in the dark for CdTe/n-Si heterojunction at forward and reverse bias voltage.

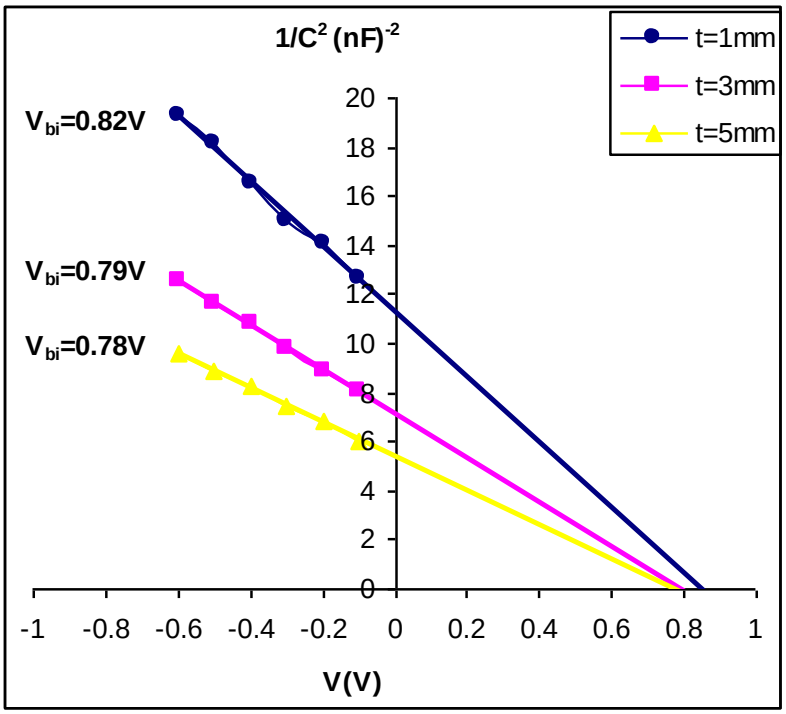

Fig. (5) the C-V characteristics for CdTe/n-Si heterojunction at forward and reverse bias voltage.

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الخواص التركيبية والكهربائية للمفرق الهجين CdTe/Si المحضر بتقنية التبخير الوميضي

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الخلاصة

يهدف البحث لدراسة الخصائص الالكتروبصرية لكاشف للمفرق الهجين CdTe/Si الذي تم تحضيره بترسيب مادة الكادميوم تلرايد بطريق التبخر الوميضي على قاعدة احادية الطور من مادة السيليكون. تم فحص الخصائص التركيبية والكهربائية للاغشية المحضرة. اظهر مفرق CdTe/Si تقويم ثنائي واسع و وحصول حالة انهيار غير حادة عندما V_B>2 V. اجريت فحوصات خصائص تيار الظلام للكاشف المحضر في درجة حرارة الغرفة.