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The performance of Hydrogenated Amorphous Silicon Charge Coupled Devices

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Abstract

From gas phase and by glow-discharge method Hydrogenated Amorphous Silicon Charged Coupled devices have been deposited. A detailed practical study has been carried out. The most important parameter , the transfer efficiency , was found to depend strongly upon the device gate number and the clock frequency. The best efficiency achieved was 97.7% and that was at frequency of 250 Hz.

Keywords : Amorphous Silicon , Charge Couple Devices

اداء عمل نبائط ازدواج الشحنة المصنعة من السليكون اللابلوري المهدرج

الخلاصة

باستخدام السليكون اللابلوري المهدرج المصنع من الطور الغازي و باستخدام طريقة التأين المتوهج ، تم تصنيع نبائط ازدواج الشحنة . و بعد ان اجريت دراسة تفصيلية للعامل الاكثر اهمية ، و هو كفاءة النقل ، وجد أنها تعتمد بصورة رئيسية على عدد البوابات المستخدمة و التردد المستعمل . ووجد أن أفضل كفاءة قد بلغت 99.97 % عند تردد 250 ذبذبة في الثانية .

الكلمات المرشدة : نبائط ازدواج الشحنة ، السليكون اللابلوري

Introduction

A charged coupled devices (CCD)is an electrical device that is used to create images of objects , store information or transfer electrical charge .It receives as input light from an object or an electrical charge. The CCD takes this optical or electrical input and converts it into an electrical signal at the output.

The electrical signal is then processed by some other equipment and software to produce an image to give valuable information.

In a CCD capturing images , there is a photoactive region (an epitaxial layer of silicon) , and a transmission region made out of shift register. A one

Dimensional array, used in line-scan cameras, capture a single slice of charge proportional to light intensity at that location, while a two- dimensional , used in video cameras , captures a two-dimensional picture corresponding to the scene projected onto the focal plane of the sensor[1] .

Hydrogenated Amorphous Silicon a-Si:H had attracted a great deal of attention for a various applications[2-5] ,such as solar cells and field effect transistors FETs . It had been

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extensively studied because of their favorable performance . i.e. high on-off current ratio, low leakage current and stable operation. The a-Si:H charged coupled deviceare one of the a-Si:H Metal-Insulator –Semiconductor (MIS) devices .

It is well known that single-crystal silicon CCDs are the most important image sensing devices , and various theoretical analyses have been reported . However , all previous works are based on the CCDs in single-crystal semiconductors and not applicable directly to the a-Si:H CCDs , because a-Si:H has so many localized states in the band gap compared with single-crystal semiconductors . When analyzing a-Si:H CCDs , it is necessary to take the effects of the localized states into account.

The main group in the world involved in a-Si:H CCD is at Tokyo Institute of Technology , some detailed studies of the a-Si:H CCDs mechanism were carried out by it [6-9]. Basically , there are two types of the a-Si:H CCDs from the charge transfer direction point of view. Firstly , when all gates are situated on one side relative to the active layer , the charge is transferred in a transverse mode . Secondly , the gates may be situated on both upper and lower sides of the active layer and the charge is transferred in a zigzag mode.

The transfer efficiency (which is calculated as the ratio between the transferred current on the corresponding and the current at the specified gate) depends strongly on the clock frequency(f) and the transfer time (i.e. clock pulse length) . The theories [7 , 10] have predicted that transfer efficiency will be improved by decreasing the clock frequency , because electrons have a sufficient time to be transferred , but the experimental results [9] are that the efficiency decreases gradually with the frequency in the low f region. The transfer efficiency was found to increase with increase in the transfer time [11]This discrepancy between theoretical and experimental results comes predominately from deep localized states [12] .

Sekina et al [12] calculated the deep states in a-Si:H /a-Si:N:H CCD. They had separated these deep states into an interface state density and a defect states density in the bulk 0f the a-Si:H layer. Their typical values for the lightly doped n-type a-Si:H layer were about 1.2×10^{11} cm^{-3} eV^{-1} and 7.0×10^{15} cm^{-3} eV^{-1} respectively .

Despite the relative low transfer efficiency of a-Si:H CCD compared with its crystalline silicon (C-SI) counterpart , the several advantages of the cheap and interesting material (a-Si:H) make it a good competitor to C-Si

Experimental Details and Results

Two –phase a-Si:H CCDs have been fabricated using Al as gates on the upper and lower sides of the samples . The widths of the lower gates were 60µm , with a separation of 80 µm . The upper gates had a width of 100 µm and a spacing of 80 µm ,giving an overlap between lower and upper gates. A-Si:N:H was used as an insulator with a thickness of 0.2 µm for both sides of the sample , with 0.7µm of a-Si:H sandwiched between the two layers .

Figure (1)shows a diagram of a circuit used to measure the CCD characteristics. A Farnell PG 102 pulse generator was used as a source for two signals to the upper and lower gates . A picoammeter was used as a current source. Two inverted AC signals were applied on both sides of the device to eliminate a vertical charge transfer in the bulk , and allow the charge to pass horizontally in the sample . By applying an external DC bias to the a-Si:H layer , the depletion regions on both sides of the a-Si:H layer should become close to overlap , to make transfer of the charge charge packet easir.

Figure (2) shows the input waveforms supplied to the upper and lower sets of gates and the output wave obtained from the metal contact on the right of figure (1) . The main feature of this wave is that it contains two output pulses for only one clock pulse. This might indicate multiple transfers between upper and lower electrodes or from both the last upper and lower electrodes to the metal contact on the a-Si:H layer . The time required to complete a charge transfer is equal to half the pulse width .

Trying to analyze this behavior , different I-V measurements have been carried out :

a. I-V characteristics obtained from the Al contacts on the a-Si:H layer showed a hysteresis loop between the increasing and decreasing voltages , which indicates trapped charges remaining somewhere along the a-Si:H layer interfaces with the upper and the lower a-Si:N:H layers.

b. The I-V characteristics measured between the upper gates and the channel showed that at 50 V the current was 1.3 x 10^{-10} amp. , while the current measured between the lower gates and the channel was 1.8 x10^{-8} amp at the same gate voltage . This indicates that the lower dielectric has a leakage bigger than that of the upper dielectric.

We believe that both the remaining charges in the interface and the leaky interface contribute to the multiple pulses obtained from the CCD . The transfer efficiency (which is measured from the height of the output signal) was measured as a function of the number of the gates (which were 15 for all the samples) ,in contrast with other reports [11-12]. We found that the dependence of the transfer efficiency with the gate number was not linear. Figure (3) shows the this transfer efficiency dependence on the number of gates . The degradation in efficiency with more gates is explained in terms of the residual charge left on each gate during the charge transfer, this might be reduced by implement a donor impurities at the back channel [13] .

Figure (4) shows the variation of the transfer efficiency with the clock frequency for a range of 100-1000 Hz .The maximum efficiency was 97.7% for a clock frequency of 250 Hz . As the frequency was increased over 1 KHz the efficiency dropped to 90%.

As the CCD in general is highly sensitive to transfer efficiency , further improvement and modifications in the growth conditions of channel and the gate dielectric [14] . This may improve the CCD characteristics for a better efficiency.

References

[1]Janesick J. ,Scientific Charged Coupled Devices , (2001), SPIE Press Book .

[2] Snell A. J. , Mackenzie K. D. , Spear W. E. , LeComber P. and Hughes A.

"The Characteristics and Properties of Optimised a-Si FETs and their Application in Integrated Image Sensors" . Appl. Phys. 24 ,(1981) , 357 .

[3] Matsumura M. , Hayama H. , Nara Y. and Ishibashi K. " Amorphous – Silicon Image Sensor ICs" , IEEE , EDL -1 , (1982) , 182.

[4]Wilson J. I. B. , Qayyum A. , Al-Sabbagh S. , Jubber M. and John P. " Photo –Oxidation of Amorphous Silicon Carbon Alloys and its use in Field Effect Transistors" , J. Non-Cryst. Solids ,115 ,(1989) , 84-86 .

[5]Ibrahim K. ,Wilson J. I. B. and Al-Sabbagh S. K . " Density of States in Compensated Hydrogenated Amorphous Silicon Films" , J. Non-Cryst. Solids . 107 , (1988) , 61-64 .

[6]Ishibashi K. and Matsumura M. Appl. Phys. Lett. " Amorphous-Silicon / Silicon- Oxynitride Field – Effect Transistors" ,41 , (1982) , 454 .

[7]Kishida S. ,Nara Y. , Kobayashi O. and Matsumura M . " Amorphous-Silicon Charge- Coupled Devices" , Appl. Phys. Lett., 41 , (1982) , 1154.

[8]Naruke Y..kishida S., Uchida Y. ,and Matsumura M. " Theory of Amorphous –Silicon Charge –

Coupled Devices" , IEEE Trans., Elect. Devices , ED-31 , (1984) , 362 .

[9]Matsumura M , "Application of Hydrogenated Amorphous Silicon in Charge – Coupled Devices" , Presented at 41 Device Research Conference III B-7, Burlington, (1983).

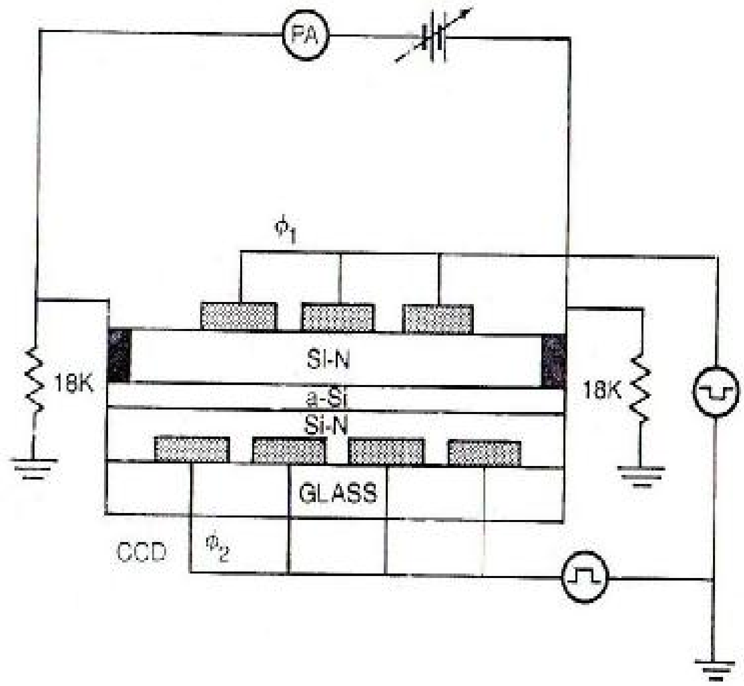
[10]Chen I. " Theoretical Analysis of Charge Transfer in Thin Film Charge Coupled Devices" ,Solid State Electron . 30, (1987) ,759 .

[11]Takeuchi Y. , Uchida Y. and Matsumura M. " Theory of Charge Transfer in Amorphous – Silicon Charge – Coupled Devices" , Jap. J. Appl. Phys. ,24,8, (1985) , 1056.

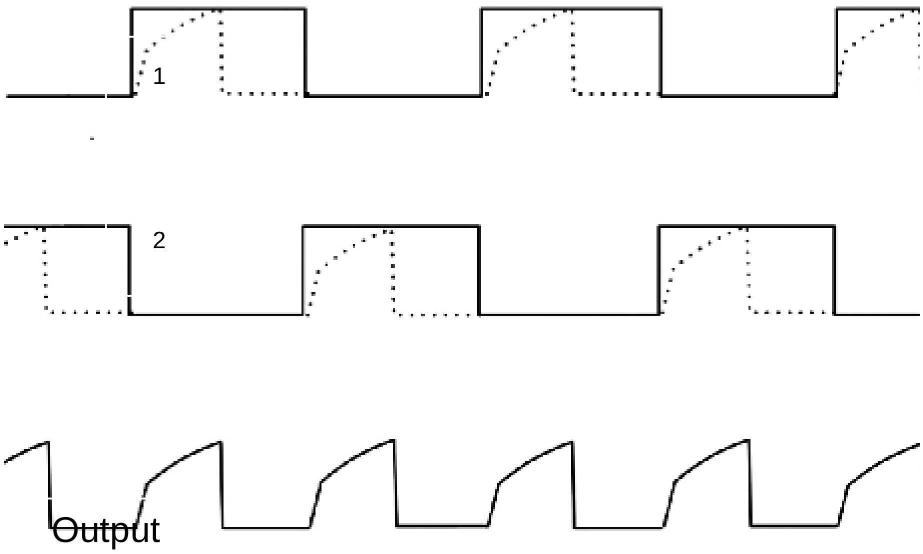
[12]Sekina S. , Nakamura S. , Oda S. and Matsumura M. "Evaluation of Deep states in Amorphous – Silicon / Silicon – Nitride System from Charge – Coupled Device Characteristics" , Jap. J. Appl. Phys. , 27 , 7 , (1988) , L1337 .

[13]Shannon J. M. and Gerstner E. G. "Compensated Back – Channel TFTs in Hydrogenated Amorphous Silicon" , IEEE , EDL , 24 ,1 . (2003) .

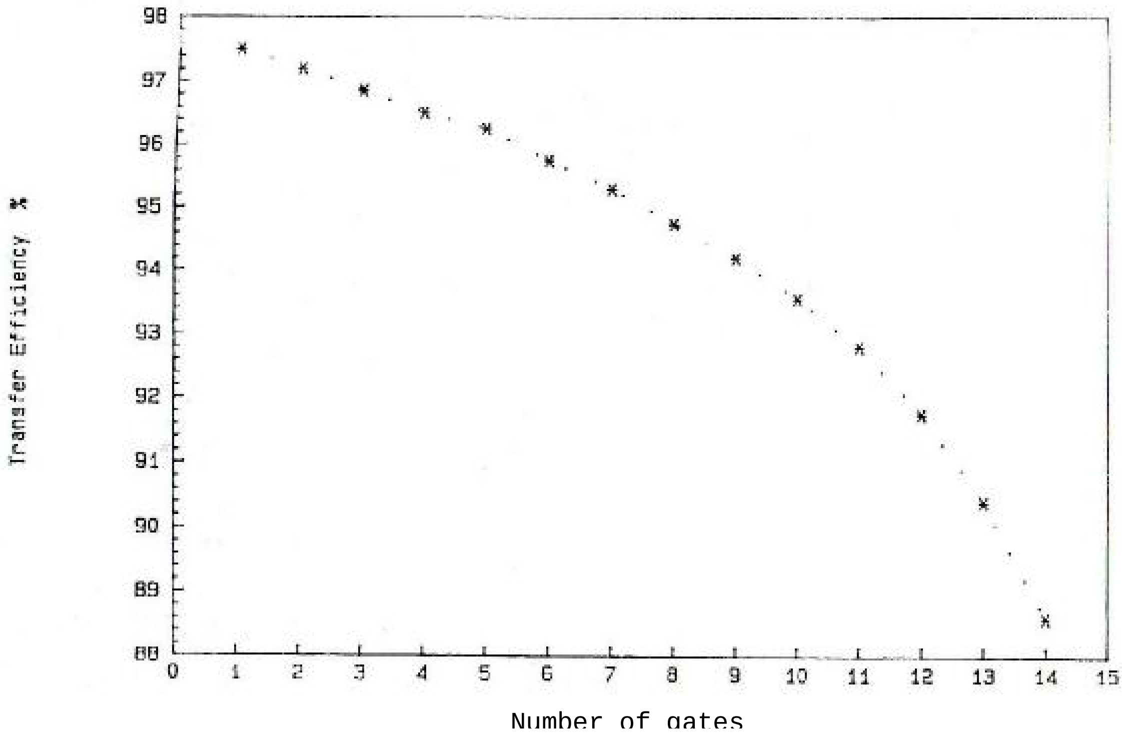
[14] Hekmatshoar B. "Highly Stable Amorphous Silicon Thin Film Transistors and Integration Approaches for Reliable Organic Light Emitting Diode Displays Clear Plastic", Ph D Dissertation , Electrical Engineering Department , Princeton University, (2010) .



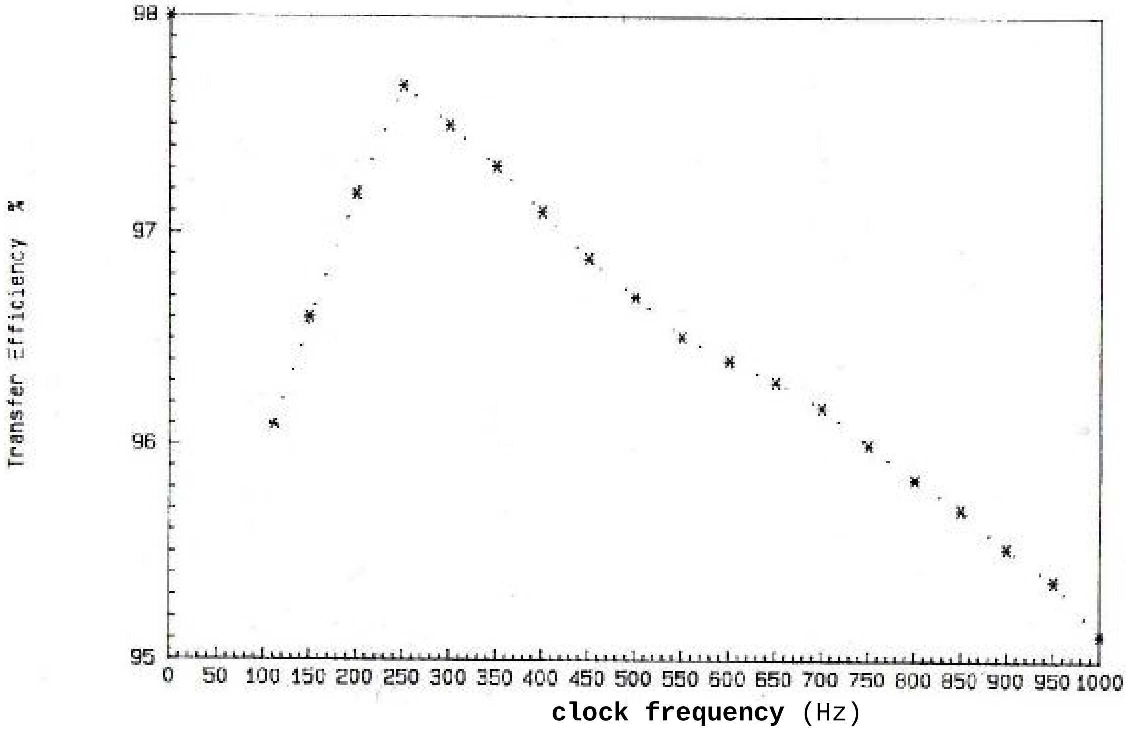
Figure(1) Circuit used in the CCD studies



Figure(2) The input waveform (rectangular) and the output waveform (broken line) obtained from the upper and lower gates . which resulted in the output waveform shown below



Figure(3)Transfer efficiency dependence on the number of gates for a-Si:N:H CCD Gate number =8



Figure(4) Transfer dependence on the clock frequency for a-Si:N:H CCD Clock frequency = 500 Hz