Design and Simulation of A New Proposed Single-Slope Integrating Analog-to- Digital Converter System Based on Non-Linear Amplifiers

Azzad B. Saeed*

Received on:18/5/2009
Accepted on: 3/12/2009

Abstract

In this paper, a unipolar single-slope integrating analog-to-digital converter(ADC) is discussed, designed, and simulated, whereas, its conversion time is less than that of the dual-slope integrating ADC.The proposed system consists of logarithmic amplifier,anti-logarithmic amplifier, integrator, counter, control logic unit and two timers stages.

The proposed design characterizes some of significant properties which make it distinguished from the other previous designed systems, such as, it has good noise immunity because of passing of the analog input signal through the integrator circuit which it considered as a low pass filter. This system is capable to convert an analog voltage of range of (0.0 – 0.6) volt using non-linear amplifiers. At last, this system has very good forward linearity relation between the output digital number and the analog input voltage value which is realized later by theoretical calculation and simulation results.

This system is simulated and tested using software package Electronic Workbench version V9, and one can see that simulation results approach to the theoretical results, so for this reason, this system possesses acceptable design and performance.

Keywords: ADC, amplifier, anti-logarithmic, comparator, counter, filter, flip-flop, Integrator, logarithmic, monostable, timer.

تصميم ومحاكاة دائرة مقترحة جديدة لمغير الاشارة التماثلية الى رقمية نوع تكامل الانحدارالمنفرد مبنية على أساس مكبرات الغير خطية

الخلاصة

تم في هذا البحث, مناقشة وتصميم وتنفيذ منظومة جديدة احادية القطب لتحويل الإشارة التماثلية إلى رقمية نوع تكامل الانحدار المنفرد(Single-slope integrating),حيث أن وقت تحويل الاشارة الخاص لهذه المنظومة هو أقل بكثير من الوقت الخاص للتحويل لمنظومة تكامل الانحدار المزدوج(Dual-slope integrating). إن المنظومة المقترحة تحتوي على مكبر لوغارتمي ,مكبر معاكس لوغارتمي,مكبر تكامل,عداد, وحدة سيطرة منطقية ومرحلتي مؤقتين.

ان المنظومة المقترحة تمتاز بعدة خواص مهمة والتي تجعلها ممبزة عن المنظومات المصممة مسبقا, فمثلا, انها تمتاز بمناعة جيدة ضد الضوضاء وذلك بسبب مرور اشارة الدخول التماثلية عبر دائرة المكامل والتي تعد بمثابة مرشح للترددات المنخفضة. كما تمتاز هذه المنظومة بأنها قادرة على تحويل الاشارات التماثلية الواطئة بمدى (0.0-0.6) فولت باستخدام المكبرات الغير خطية. وكذلك تمتاز بدقة العلاقة الخطية بين الرقم الناتج

***Electrical & Electronic Engineering Department, University of Technology/Baghdad**

https://doi.org/10.30684/etj.28.6.16
2412-0758/University of Technology-Iraq, Baghdad, Iraq

(قيمة العداد) وقيمة اشارة الدخول التماثلية والتي سوف يتم لاحقا اثباتها بالحسابات النظريـــة ونتائج المحاكاة.

نفذت هذه المنظومة وأختبرت باستخدام الرزمة البرمجية Electronic Workbench V9حيث تمت مقارنة نتائج المحاكاة مع النتائج النظرية وكانت متقاربة جدا وبذلك اصبحت المنظومة مقبولة من حيث الأداء والتصميم.

Introduction

One of the important type of ADCs is the single-slope integration system. This converter has greater noise immunity and errors are minimized.

The proposed designed system which is named single-slope A/D converter is an improved dual-slope A/D converter system, whereas, the longer integrator output slope of the dual-slope system is canceled. So the conversion time of the proposed system is less than the dual-slope system.

Fig.(1) shows the block diagram of the proposed system. The input voltage V_a is fed to the input of the logarithmic amplifier, the result is the output signal V_1 which is equal to $-K_1.ln(K_2.V_a)$, then this signal is fed to the anti-logarithmic amplifier, so the output signal is V_2 which is equal to $-K3/V_a$, this signal is integrated by the integrator unit to give the output signal V_3 , which is equal to $(K4.n.V_a)$, where K_1,K_2,K_3,K_4 are constants, and n is the number of clock pulses of Timer1 that enter to the counter unit. Then the comparator gives a pulse (of HIGH state) for a period of time equal to (nT), where T is the one clock cycle period of Timer 1.Therefore, the AND gate passes n of pulses to the N-bit counter, whereas the number of these pulses is linearly proportional to the input voltage V_a.

The following reports are related to systems that serve similar objectives as those of the system proposed in this work.

In 2003, Tony R. Kuphaldt [1] proposed a system that consists of an integrator to generate a saw tooth waveform which is then compared against the analog input by a comparator. The time it takes for the saw tooth waveform to exceed the input signal voltage level is measured by means of a digital counter clocked with a precise-frequency square wave(usually from a crystal oscillator).This system uses IGFET capacitor and discharging transistor connected in parallel in the feedback of the integrator circuit. There is no noise immunity in this system because the analog input voltage is not integrated.

ST Co.[2] described in 2005 a technique for implementing an ADC for measuring both positive and negative input voltages while operating from a single (positive) supply. This converter is based on a Voltage-to-time Conversion technique. The measured time is inversely proportional to the input unknown voltage. An additional comparator with a voltage reference is used to improve conversion accuracy.

In 2008, *MAXIM* Co.[3] suggested simplest form of an single-slope integrating ADC uses an integrator and comparator circuits, without discharging switches. Here,

an unknown input voltage is integrated and the value compared against a known reference value. The time it takes for the integrator to trip the comparator is proportional to the unknown voltage. This system has good noise immunity.

The dual-Slope integration A/D converter

This system is widely used in the practical field, which is shown in Fig(2).Consider unipolar operation with $V_a>0$ and $V_r<0$.The voltage controlled switch VSC1 has 2-way single pole switch (S1), while VSC2 has one way single pole switch S2. initially (at $t=t_1$) [see Fig.(3)]one can apply a pulse at the start of conversion input of the control circuit, then the monostable circuit is ignited by the positive edge of this pulse, therefore , a very narrow pulse is generated at the output of the monostable circuit which is used to clear instantly the N-bit counter, and to short the switch S2 to discharge the capacitor C instantly. At this time the JK flip-flop of the control circuit is activated at SET state (Q=1) to connect the switch S2 to V_a.The sampled analog voltage V_a is now integrated for a fixed number n_1 of clock pulses. If the clock period is T, the integration takes place for a definite known time $T_1=n_1.T$, and the waveform V at the output of the integrator is indicated in Fig(3)[6].

If an N- stage ripple counter is used and if $n_1=2^N$, then at time $t=t_2$(the end of the integration of V_a) all FLIP-FLOPS in the counter read 0. For a four –stage ripple counter where, after $n_1=2^4=16$ counts, the output bits $Q_0=0$, $Q_1=0$, $Q_2=0$, and $Q_3=0$. In other words, the counter automatically resets itself to zero at the interval T_1. Generally after 2^N pulses, the state of Q_{N-1} (MSB), changes from 1 to 0 for the first time[6]. This change of state can be used as the control signal for the RESET input of the JK flip-flop.

Because of the counter operation described in the preceding paragraph, then (at $t=t_2$) the JK flip-flop is cleared (Q=0) by the RESET signal from the most significant bit[Q(N-1)] of the counter to connect the switch S2 to the reference voltage V_r which is connected to the input of the integrator , at which time the counter reads zero. Since V_r is negative, the waveform V has the positive slope shown in Fig (3).

We have assumed that $|V_r| > V_a$, so that the integration time T_2 is less than T_1, as indicated. As long as V is negative, the output of the comparator is positive and the AND gate allows clock pulses to be counted. When V falls to zero, at $t=t_3$, the AND gate is inhibited and no further clock pulses enter the counter[3,4,5,6].

We now show that the reading of the counter at time t_3 is proportional to the analog input voltage. The value of V at t_3 is given by[6]:

$$V=\frac{-1}{RC}\int_{t_1}^{t_2} V_a\,dt+\frac{1}{RC}\int_{t_2}^{t_3} V_r\,dt$$

$$=0 \qquad \text{..... (1)}$$

With V_a and V_r constant,

$$-V_a(t_2-t_1)+V_r(t_3-t_2)=0$$

or $V_a=|V_r|T_2/T_1$

If the number of pulses accumulated in the interval T_2 is n_2, then $T_2=(n_2T)$.

Since $T_1=(n_1T)=(2^NT)$, then[6,7,8]:

$$V_a = \frac{T_2|V_r|}{T_1} = \frac{n_2|V_r|}{n_1} = \frac{n_2|V_r|}{2^N} \quad \ldots\ldots (2)$$

Since $|V_r|$ and N are constant, we have verified that V_a is proportional to the counter reading n_2. Note that this result is independent to the time constant RC.

This technique can be very accurate; six-digit digital voltmeters employ such signal processing. The counter feeds a decoder / lamp driver so that the output is visible. For each cycle of operation a new voltage reading is obtained.

The dual-slope system is inherently noise-immune because of input-signal integration, i.e., the ubiquitous 50-Hz can be all but eliminated by choosing the integration time to be an integral of power line periods. This statement also brings to light the obvious disadvantage of the system, namely, the conversion time is long since1/50 s = 20 ms[6,7].

The proposed circuit operation and theoretical calculations

This unipolar ADC system contains of eight units (circuits) as shown in Fig(4), whereas, the first three units perform a mathematical operations to the analog input voltage (V_a).

Primarily, one can start with the limitation range of the analog input voltage (V_a), whereas, $0 < V_a <$ 0.6 for silicon diode, which is the non-linearity region range of the ideal diode.

The sampled analog input voltage (V_a) is applied at the input of the logarithmic amplifier to generate the signal voltage (V_1) at the output of UNIT 1 [see equation (A.5) in the appendix(A)] ,which is applied to the input of the anti-logarithmic amplifier to generate the signal voltage (V_2)at the output of UNIT2[equation (A.10) in the appendix(A)],at last, the signal voltage (V_2) is applied to the input of the integrator to generate (V_3) at the output of UNIT3[equation (A.12) in appendix(A)].

At the first moment of time t_1 as shown in Fig(5), the control unit (UNIT7) gives a very narrow pulse to clear instantly the N-bit counter, and its JK flip-flop is activated (Q=1) to switch off the (voltage controlled switches) S2,S3 and switch on S1,S4 which is shown in Fig.(4), so the capacitor C_2 is shorted (discharged)and disconnected to the feedback of the integrator UNIT3 and the capacitor C_2 is opened(i.e. ready to charging) and connected to the feedback of the integrator, the state of the switches is shown in the timing diagram Fig.(7). At this time the signal V_2 is integrated over the integration period, and the capacitor C_1 charges with time constant R_3C_1 which is equal to period of the input signal (V_2) to be integrated, while the output voltage V_3 ramp increases with time until the Op-Amp integrator (UNIT3) saturates (at $V_3=+V_{cc}$)[7], where the saturation period is finished at the beginning of the next clock(t_3) of the Timer2(UNIT6) as shown in Fig(5).When the capacitor C_1 is start to charge whereas $V_3<V_{ref}$, the output of the comparator (UNIT 4) is (0), so the clock pulses of the Timer 1(UNIT 5) enter to the input of the counter through the AND gate. The counter counts the pulses until

the voltage V_3 reaches to the value of V_{ref}, at this time the output of the comparator is changed to (1) then the counter is stopped to count,and this last count number represents the analog input voltage (V_a).So one can say that the comparator gives a LOW pulse of a period nT at its output, which activates the AND gate to pass n of clock pulses of Timer 1 to the input of the N-bit counter.

One can analyze the circuits of UNIT1,UNIT 2, and UNIT3 in Fig.(4) and estimate the analog input voltage (V_a) as shown in the appendix(A), where,

$$V_a = \frac{MN}{R_3 C_1 V_3} nT \qquad \text{..... (3)}$$

If V_3 is equal to the constant reference voltage V_{ref} of the non-inverting input of the comparator UNIT4 then:
V_3, M, N, R_3, C_1, T are constants and known in the appendix(A), then

$$V_a \propto n \qquad \text{..... (4)}$$

One can see that the changing of the analog input voltage is direct (linearly) proportional to the changing of the number of clock pulses that enter the N-bit counter.

The conversion is repeated at the next cycle of clock signal of the Timer2(UNIT6)(i.e. $t>t_3$) see Fig.(5) ,whereas the switches S1,S4 are in OFF state and S2,S3 are in ON state,so the capacitor C_1 is shorted and disconnected to the feedback of the integrator while C_2 is opened and connected to the feedback of the integrator, then it will be charging and the operation is repeated , so V_a can be calculated as follows :

$$V_a = \frac{MN}{R_3 C_2 V_3} nT \qquad \text{..... (5)}$$

where $C_1 = C_2$

One can see that the input analog voltage V_a *is* dependent on the time constant (R_3C_1) or (R_3C_2).

This system is also has a noise immunity because the existing of the integrator amplifier (UNIT3), which acts as a low pass filter, its cut-off frequency is calculated as follows[3,4]:

$$f_C \le \frac{1}{2pR_3C_1} \qquad \text{..... (6)}$$

If we let the cut-off frequency is 50 Hz for the power lines noise signals that exist everywhere, then:

$$R_3C_1 \le \frac{1}{2p\,50} \qquad \text{..... (7)}$$

The control logic unit (UNIT7) that shown in Fig.(6), consists of two circuits, they are, one-shot-to circuit and JK flip-flop circuit. The first one is a monostable circuit which it consists of AND gate, NOT gate, and the capacitor C_3.This circuit generates a narrow HIGH pulse for clearing the N-bit counter.The clock input of this circuit is fed from the output of the Timer2 unit, which is ignited by the positive edge of the Timer2 clock signal, that is shown in the timing diagram of Fig.(7).

The second circuit is the JK flip-flop, which controls the voltage controlled switches (S1,S2,S3 and S4)of the integrator unit, the clock input of this circuit is fed from the output of the Timer 2 unit ,and it ignited by the positive edge signal too. The Q output of the JK flip-flop

controls the switches S1and S4 at the same moment, and the Q́ output controls switches S2,S3.

Finally, in Fig.(7) one can see the synchronization of six important signals for two analog input voltage V_{a1} and V_{a2} (where $V_{a2}>V_{a1}$ and $n_2>n_1$).

The proposed system design and results

Initially we must calculate R_3 for cut off frequency≥ 50 Hz (noise immunity) and let C_1,C_1 have capacitance values of 1µf,[6,7] then:

$$R_3 = \frac{1}{2pfC_1} = \frac{1}{2p50\times10^{-6}} = 3.183\times10^{3}\Omega$$

where R_3C_1 or

$R_3C_2 = 3.183 \times 10^{-3}$ sec

One can use the diode 1N 4153 which has reverse saturation current(I_S) of 20 nA and let $R_1=R_2=$ 5 MΩ.

Let the maximum input voltage $V_{a(max)}$ is equal to 0.6 volt and the maximum output reading of the 8-bit counter is$(FF)_H$ or $(255)_{10}=n$

Let the the frequency of Timer1 is 1kHz, so the single cycle period is T=0.001 sec.

Now by using equation (A.13)[in the appendix (A)], one can calculate the fixed reference voltage V_{ref}, as follows:

$$V_{ref} = \frac{MN}{R_3C_1}\frac{nT}{V_a} = \frac{I^2R_1R_2}{R_3C_1}\frac{n_{\max}T}{V_{a(\max)}}$$

$$= \frac{400\times10^{-18}\times25\times10^{12}}{3.183\times10^{-3}}\cdot\frac{255\times0.001}{0.6}$$

=1.3352 volt

Now let R_4=10KΩ , then the current that passes through R_4 and R_5 is equal to:

$$i_5 = \frac{5-1.3352}{10\times10^{3}}$$

$$= 3.6648\times10^{-4}\ Amp$$

therefore,

$$R_5 = \frac{1.3352}{3.6648\times10^{-4}}\Omega$$

$$= 3.6433K\Omega$$

At this point the design is completed. The theoretical results are shown in Fig.(8) whereas, the relation between the counter output number (n) versus the analog input voltage (V_a) is linear, and that's what do we want and supports the theoretical calculations. As shown in Fig.(8), at (0.6 volt) analog input voltage the counter reads $(FF)_H$ or $(255)_{10}$, and at (0 volt) input analog voltage, the counter reads $(00)_H$ or $(0)_{10}$.

The simulation results are shown in Fig.(9),which shows the line that passes through 24 reading points which represents the relation between the analog input voltage (V_a) versus the counter output number(n).As shown , at (0.6 volt) analog input voltage the counter reads $(AA)_H$ or $(170)_{10}$, while at (0 volt) analog input voltage the counter reads $(00)_H$ or $(0)_{10}$.

There are some deviations between the theoretical and simulation readings, this due to the changing between the theoretical and simulation values of the diode reverse saturation current (I_s). whereas the theoretical value is 20 nA, while the simulation value is

≈30nA, so the error ratio is 30/20=(1.5).As shown in equation (A.13)[in appendix (A)] this error ratio is transferred to the maximum counter output reading (n), where it is divided by 1.5 to make the fixed reference voltage V_{ref} with no change, so 255/1.5=170 which is the maximum counter output reading.

Comparison between the proposed system and dual-slope integration ADC

The proposed system has single voltage slope at its integrator output, but the dual-slope system has two[2].

The conversion time of the proposed system is less than the dual- slope system, because the counter of the dual-slope system counts to reach to the maximum count (for 8-bit is FF_H) and then start to count again while the proposed system is not.

The analog input voltage of the proposed system depends on R and C of the integrator circuit but the dual-slope system is not[5,6,7].

Dual-slope system needs a reference voltage (V_r) with minus (-) value on its input but the proposed system is not[2].

Both speed of these systems are limited by the values of R , C of the integrator unit,and, both of the systems have good noise immunity, because the existing of the integrator circuit(Low Pass Filter)[1,8].

At last, the circuit components of the proposed system is more than that of the dual-slope system.

Conclusions

From the review to the theoretical and simulation results, several features arise that are of importance to state.

The analog input voltage is linearly proportional to the number of the clock pulses that enter the input of the counter.

The resolution of the proposed system is 8-bit.

The accuracy of the proposed system is 3.53×10^{-3} Volt.

For 50Hz noise immunity,the speed of conversion is limited , because the time constant(conversion time) R_3C_1 or R_3C_2 must be more than $\frac{1}{2p \times 50}$.

If we ignore this noise immunity we can increase the speed of conversion by using high frequency Op-Amps and digital ICs and by increasing the frequency of Timer1 and Timer2.

References

[1].Tony R. Kuphaldt , "Digital Analog Conversion ", Chapter 13, 2003, © Op/Amp Electronics.

[2].*ST* Corporation, "A High Precision Low Cost, Single Supply ADC for Positive and Negative Input Voltages", 2005.

[3].*MAXIM* ntegrated products Co.,"Understanding Integrating ADCs", 2008, © Maxim Integrated Products, Dallas Semiconductors.

[4].Intel Co., "Analog Data I/O Solutions For Intel 8×C196NP Microcontrollers", December 2000, © Intel Corporation.

[5].Exstrom Laboratories LCC

,"Analog to Digital Converters",2007, © Exstrom Laboratories LCC.

[6].Jacob Millman & Arvin Grabel, "Microelectronics", 1987, © Mc Graw-Hill.

[7].K.V. Ramanan, "Functional Electronics",1987, © McGraw-Hill.

[8].Engineering Staff of Analog Devices Inc., "Analog to Digital Conversion", 1986, ©Analog Devices Inc., Norwood,MA02062.

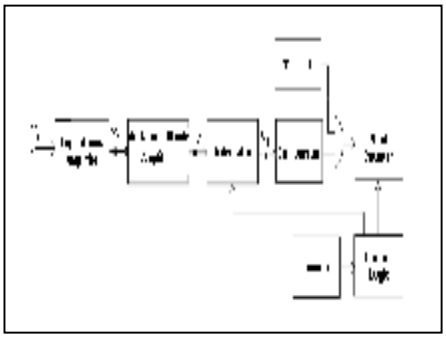

Figure (1) Block diagram of the single- slope integrating ADC.

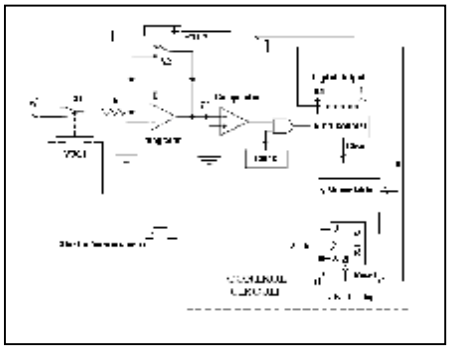

Figure (2) Circuit diagram of the dual-slope integrating ADC[2]

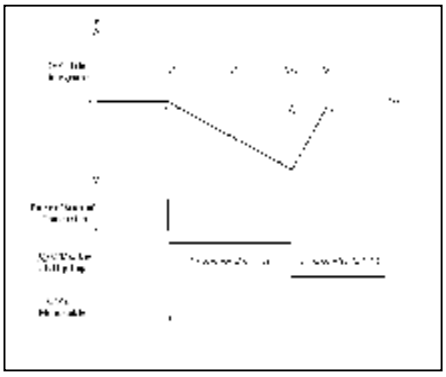

Figure (3) The output waveform of the integrator unit and timing diagram

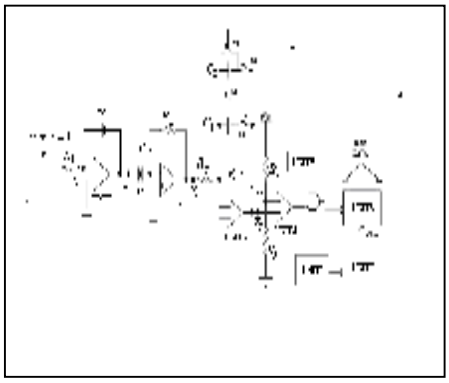

Figure (4) Circuit diagram of the single-slope integrating ADC

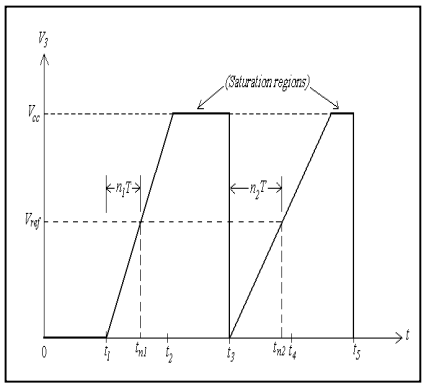

Figure (5) Integrator output waveform of the single-slope integrating ADC

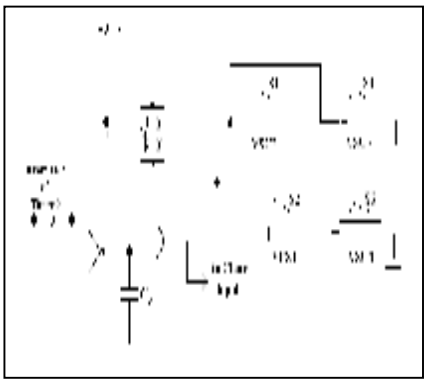

Figure (6) Circuit diagram of the control logic unit

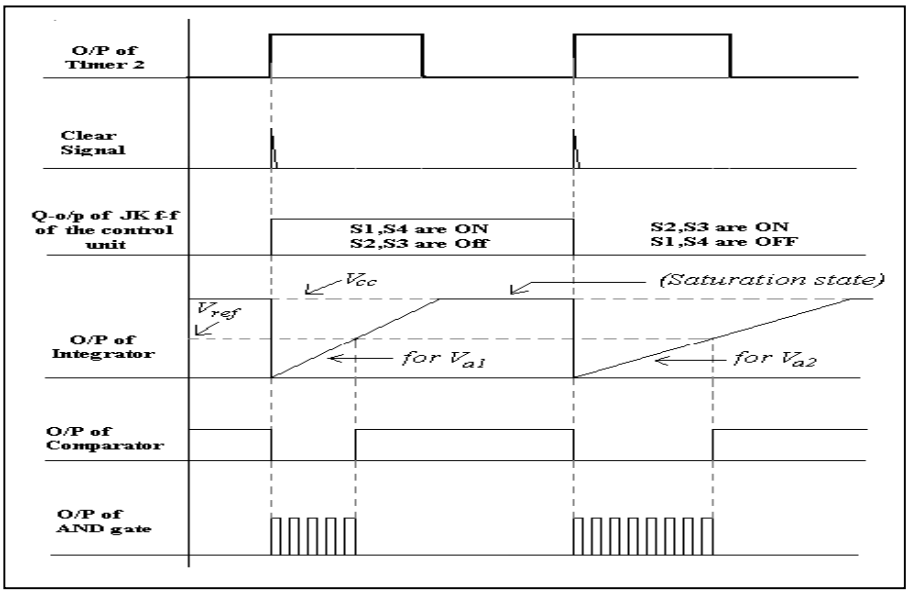

Figure (7) Timing diagram for most important signals of the proposed system

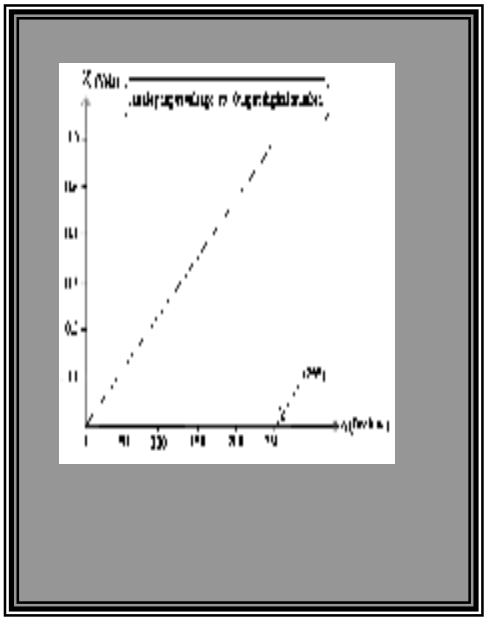

Figure (8) Theoretical results of proposed system.

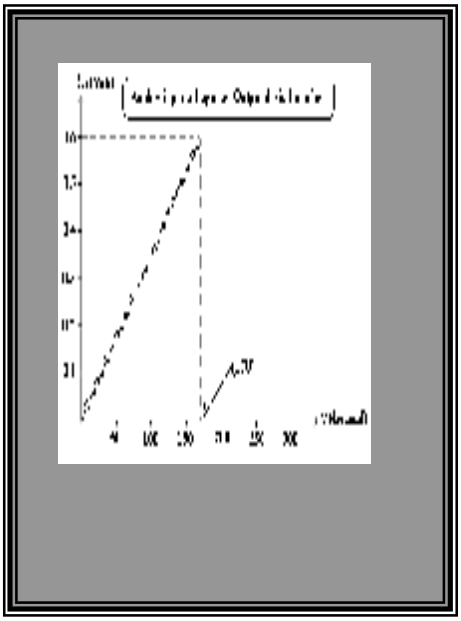

Figure (9) Simulation results of the proposed system.

Appendix(A).

Derivation Details of Equ.(A.12)

One can derive the analog input voltage equation of the single-slope integration ADC (the proposed system) as shown below, see Fig.(4).

1- Circuit of UNIT 1

(Logarithmic Amplifier)

$$V_a = i_1 R_1 \qquad \text{..... (A.1)}$$

$$V_1 = -V_{D1} \qquad \text{..... (A.2)}$$

$$i_1 = i_{D1}$$

where V_1 is the output voltage of UNIT1.

The diode current equation is:

$$i_D = I_S e^{\frac{qV_D}{KT}} \qquad \text{..... (A.3)}$$

by substituting equation (A.3) in (A.1), we get,

$$V_a = R_1 I_S e^{\frac{qV_{D1}}{KT}} \qquad \text{..... (A.4)}$$

by substituting equation (A.2) in (A.4) we get,

$$V_a = R_1 I_S e^{\frac{-qV_1}{KT}}$$

Let $L = \frac{q}{KT}$, $M = I_S R_1$, therefore ,

$$\frac{V_a}{M} = e^{-LV_1}$$

then $$\ln \frac{V_a}{M} = \ln e^{-LV_1}$$

so, $$V_1 = -\frac{1}{L} \ln \frac{V_a}{M} \qquad \text{.....(A.5)}$$

2- Circuit of UNIT 2

(Anti-logarithmic Amplifier)

$$V_1 = V_{D2} \qquad \text{.....(A.6)}$$

$$V_2 = -i_2 R_2 \qquad \text{.....(A.7)}$$

where V_2 is the output voltage of the Anti-logarithmic amplifier (UNIT2),
using equation(A.3), we get

$$V_2 = -R_2 I_S e^{\frac{qV_{D2}}{KT}} \qquad \text{....(A.8)}$$

by substituting equation (A.6) in (A.8), we get

$$V_2 = -R_2 I_S e^{\frac{qV_1}{KT}}$$

let $I_S R_2 = N$ so,

$$V_2 = -N e^{LV_1} \qquad \text{.....(A.9)}$$

by substituting equation (A.5) in (A.9) we get

$$V_2 = -Ne^{-\ln\frac{V_a}{M}}$$

$$V_2 = -Ne^{\ln\frac{M}{V_a}}$$

finally, $V_2 = -\frac{NM}{V_a}$ .....(A.10)

3- Circuit of UNIT 3 (Integrator Amplifier).

$$V_3 = \frac{-1}{R_3C_1}\int_{t_1}^{t_n} V_2\,dt$$

$$V_3 = \frac{-1}{R_3C_1}V_2(t_n - t_1)$$

where V_3 is the output voltage of the Integrator amplifier(UNIT 3).

Let $(t_n - t_1) = nT$, see Fig.(5) where n is the number of clock pulses of Timer 1 (UNIT5) that enters to the input of the N-bit counter (UNIT8), and T is the period of one clock cycle of the Timer 1.

so, $V_3 = -\frac{1}{R_3C_1}V_2 nT$

$$\frac{V_3}{V_2} = -\frac{1}{R_3C_1}nT \quad .....(A.11)$$

by substituting equation (A.10) in (A.11)

$$\frac{-V_aV_3}{MN} = \frac{-1}{R_3C_1}nT$$

$$V_a = \frac{MN}{R_3C_1V_3}nT \quad .....(A.12)$$

which is the output voltage equation of the integrator circuit of the proposed system.

When the value of V_3 reaches to the value of fixed (constant) reference voltage(V_{ref}) applied at the inverting input of the comparator (UNIT4),then:

$$V_a = \frac{MN}{R_3C_1V_{ref}}nT \quad .....(A.13)$$

Where, V_3=V_{ref}. in this condition.