Design and Implementation of a New Proposed Electronic Clock System Based on The Integrating Amplifiers

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Abstract

In this paper, a new proposed system of electronic clock is discussed, designed and implemented, it consists of digital electronic components such as, logic gates and decade counters, and analog electronic components such as, integrating amplifiers. These integrating amplifiers converts the digital output signal of the minutes and hours counters to an analog triangular signal.

Two signal indicators are used in this design to measure the minutes and hours output signal, which they are scaled in desired and proper manner.

This system has vary good forward linearity between the measured time and the output signal of the integrating amplifiers.

This system is practically implemented and tested using software package Electronic Workbench version V9, whereas, the practical, simulation and theoretical results were approximately identical, therefore, this system has successful design and implementation.

Keywords: Counter, divider, integrator.

تصميم وتنفيذ منظومة مقترحة جديدة لساعة الكترونية مبنية على أساس المكبرات التكاملية

الخلاصة

تم في هذا البحث, مناقشة وتصميم وتنفيذ منظومة جديدة مقترحة لساعة الكترونية, حيث انها تحتوي على مكونات الكترونية رقمية, كالبوابات المنطقية والعدادات العشرية, وكذلك تحتوي على مكونات الكترونية تماثلية, كالمكبرات التكاملية.حيث ان هذه المكبرات التكاملية تحول اشارة الخرج الرقمية لعدادات الدقائق والساعات الى اشارة مثلثية تماثلية.

تم استخدام اثنان من مبينات الاشارة في هذا التصمبم لقياس اشارة خرج الدقائق والساعات, بحيث تم تدريج هذه المبينات بالصورة المرغوبة والصحيحة.

كما تمتازهذه المنظومة بدقة العلاقة الخطية الطردية بين الوقت المقاس واشارة خرج المكبرات التكاملية.

نفذت هذه المنظومة عملياً وأختبرت باستخدام الرزمة البرمجية Electronic Workbench V9, حيث ان النتائج العملية والمحاكاة والنظرية كانت تقريباً متماثلة, لذلك فان هذه المنظومة تمتلك تصميم وتنفيذ ناجحين.

1-Introduction

There are several types of clock(watch) instruments in the scientific history, these are, sandglass(the oldest), mechanical, electromechanical, and digital types.

The mechanical type contains of circled spring, and 18-21 gears (toothed wheels) they are connected in serial form, which it depends on the continuity of the circle motion of the small spring.

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The electromechanical type is widely used, it consists of several gears, an electronic circuit, and a solenoid coil, whereas, the electronic circuit contains of a crystal oscillator, divider, and driver circuits which generate 1 Hz clock pulses to drive the solenoid coil. The solenoid circulates the gears with the same frequency to make the clock acts with proper manner.

The second widely used type is the digital clock, it consists of crystal oscillator, divider, counters, decoders, and seven segment display, the last one may be LCD or LED types. The showing of the seconds, minuets, and hours numbers is done by the decoders and displays. This type has very low power consumption, so it is widely used in cars, aeroplane, steamships, spaceships,…etc.

The proposed system is a new type of the clock circuit that is shown in Fig.(1), it consists of a crystal oscillator that generates 1 MHz clock pulse signal, which it divided by the divider by 10^6 stage to generates 1 Hz clock signal, then this signal is divided by 60 to generates 1/60 Hz clock signal, which is divided by 60 again to generates 1/3600 Hz clock signal, then the last signal is fed to the input of the monostable (1) circuit, that generates narrow pulses (with pulse width =3μsec) with frequency 1/3600 Hz(i.e. a narrow pulse is generated every 1 hour).This narrow pulse is used to discharge the capacitor of the integrator(1) at stage 6(integrator means integrating amplifier) ,whereas, this stage is included in the proposed circuit, and it generates a ramp signal (triangle wave signal) restarted from zero level every 1 hour, then this signal is fed to the minutes indicator at stage 7(that shows minutes output), which is scaled from 00 to 60 minutes with steps of 5 minutes.

The output clock signal of the second divider by 60 at stage 4 (with frequency 1/3600 Hz) is fed to the input of the divider by 24 (stage 8),so the last one generates a clock signal with frequency 1/86400 Hz, which is fed to the input of the monostable (2) at stage 9, then this stage generates narrow pulses(with pulse width = 3 μsec) every 24 hours (1 day) with the same frequency(1/86400 Hz).This narrow pulses are used to discharge the capacitor of the integrator amplifier (2) at stage 10 every 24 hours(1 day),whereas, this stage is used to generate ramp signal(triangle wave signal) restarted from zero level every 24 hours(i.e. when the monostable(2) generates the narrow pulse), then the output signal of the integrator amplifier (2) is fed to the hours indicator at stage 11 (that shows the hours output),which is scaled from 00 to 24 with one hour steps.

The following reports are related to systems that serve similar objectives as those of the system proposed in this work.

In 2009, Fatton Jean-claude [1] proposed an electronic watch circuits for the measurement and the display of time and for measuring a reaction time, and which further includes circuits controlling the display of a signal determined by comparing the measured reaction time with a reference time.

Portman Hubert [2] produced in 2009, an electronic battery-powered watch including an oscillator followed by a chain of frequency divider stages, said chain being

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composed of two parts with an interface circuit between said two parts, said interface circuit multiplying by a predetermined amount the voltage of the battery and the amplitude of the pulses issued from the last stage of the first part of the division chain in order to feed and control the second part of the chain and the decoding and display circuits of the watch.

In 2009, Flaig Hans[3] suggested a time-controlled tone signal is produced by electronic clock circuitry for a clock having chimes and/or an alarm system. In order to provide fully electronic storage and release of tone signal sequences, their data, such as tone frequencies and tone lengths, are stored in digital form in a memory circuit. The data is recalled from the memory with regard to time and is transformed by means of an electro-acoustic transducer into the desired sequence of tone signals.

2-The Proposed Circuit Operation and Theoretical Calculations

The proposed circuit design is illustrated in Fig.(2),the first stage in this design is the circuit of ICs (U1, U2),which is the crystal oscillator (astable multivibrator), its output frequency f_o depends on the resonance frequency of the crystal component (XTAL), which it equals to 1 MHz in this proposed design. The connection of the U1,U2 (which are NAND gates 74LS00 connected as inverters) form a positive-feedback circuit, where the phase shift between the output of U2 and the input of U1 is 360^o or 0^o. R_1,R_2 are equalled resistors and are connected as a negative-feedback resistors to limit the gain of the inverters U1,U2(each inverter has phase shift 180^o between its input and output),which they equal to 1 KΩ in this proposed circuit. VC_1 is a variable capacitor of 60 pF, it is used to accurate the output frequencyf_o to 1 MHz exactly. U3 is a NAND gate which is connected as a buffer inverter that is used for isolation and protection of output of the crystal oscillator from the input of the next stage (divider by 10^6 circuit U4-U9).

The second stage is the divider by 10^6 circuit(U4-U9), it consists of six cascaded decade counters(i.e. six dividers by 10), the type of these six ICs is TTL 74LS90(the clock input of this IC is negative edge triggered)[4,5,6] ,and they operate by +5Volt power supply. The signal frequency of the input of this stage(which it fed from the output of the crystal oscillator) is 1 MHz at point (*A*), while the output signal frequency is 1 Hz (i.e. 1 clock cycle per second) at point (*B*).The (CKB) input (pin1) is connected to the (QA) output (pin12) for each IC of this stage. The (QD) output(pin11) is connected to the (CKA) input (pin14) of next IC. The reset inputs (R01),(R02),(R91), and (R92) are grounded.

The third stage is the circuit of the first divider by 60, it consists of two cascade counters U10,U11(type TTL IC 74LS90), the first is a decade counter(U11), while the second is a divider by 6 counter(U10), which is achieved by connecting (QB,QC) outputs of U10 to the inputs of the AND gate (U12)(IC TTL 74LS08), then the output of this gate is connected to the reset inputs (R01,R02) of the two counters (U10,U11).The input signal frequency of this stage(which is fed from the output of the divider by 10^6

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stage) is 1 Hz at point (*B*), while the output signal frequency is 1/60 Hz at point (*C*).This stage counts the seconds from (00_D) to (59_D) then it reset itself again to(00_D) and so on.

The fourth stage is the circuit of second divider by 60, and it consists of same components and connection circuit of the third stage, where ICs U13,U14 are used in this stage as shown in Fig.(2).The input signal frequency of this stage(which is fed from the output of third stage) is 1/60 Hz, while the output signal frequency is 1/3600 Hz at point (*D*).This stage counts the minutes from (00_D) to (59_D) then it reset itself to (00_D) and so on.

The fifth stage is the monostable(1)(one-shot-to) circuit, which is combined from U16(inverter),U17(NOR gate) and C_1,its input(point *D*) is negative edge triggered by the QC output of the fourth stage(second divider by 60) with clock frequency of 1/3600 Hz. A narrow positive pulse is generated at the output of this stage(point *E*), which is used to close the shunted switch of the sixth stage to discharge the capacitor(C_2) at the start of every one hour(60minutes), which is illustrated in Fig.(3).The width of the generated pulse depends on the value of C_1(practical pulse width is 3 μsec when C_1 value is equal to 0.1 μF).The type of U16 is TTL IC 74LS04,while U17 is TTL IC 74LS02.

The sixth stage is the integrator(1) circuit, IC LM 358 is used in this stage[7,8], this circuit integrates the DC input voltage that is applied at point (*F*),so the output voltage linearly increases with the time, whereas R_4C_2 is the time constant of the integrator(1) ,see Fig.(3) (in this design $R_4C_2 \geq 3600$ second),the maximum output voltage of this stage must not exceed the power supply voltage +Vcc (if it exceeds +Vcc, it reaches to the not desired saturation state), which it depends on the value of input voltage V_F, the resistor R_4 and the capacitor C_2. The capacitor C_2 is shorted by the switch VCS_1 for a period of 3μsec (which is the period of the output pulse of monostable(1)) at each start of the clock cycle of the fourth stage(the second divider by 60), so the output voltage of the integrator(1) is zero for this period of time (that represents the starting point for the output voltage increasing).When the switch is opened, then the output voltage is started to increase linearly(ramp increasing) until it reaches to the maximum value at the end of the clock cycle(the clock cycle period is 60 minutes or 1 hour). At the next cycle the operation is repeated. One can calculate the output voltage of the integrator (1) V_G by using the following formula[9,10]:

$$V_G = \frac{-1}{R_4 C_2} \int_0^t V_F \, dt \quad \text{.....(1)}$$

Since V_F is the DC input voltage and it is constant, therefore

$$V_G = \frac{-V_F t}{R_4 C_2} \quad \text{.....(2)}$$

V_F,R_4,andC_2 are constants, so one can say that the integrator output voltage (V_G) is direct(linear) proportional with the time (*t*), so

$$V_G \propto t \quad \text{.....(3)}$$

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For maximum output voltage value, one can get,

$$V_{G(max)}=\frac{-V_F\, t_{(\max)}}{R_4 C_2} \quad \ldots\ldots(4)$$

where R_4C_2 is the time constant.

The variable resistor VR_1 is used to set the desired DC input voltage at point (F), while the variable resistor VR_2 is used to match the output voltage range ($0 - V_{G(max)}$) to the reading voltage range (0 – 500mV) of the minutes indicator (stage 7).The minutes indicator has a scale of 12 steps (00 – 60), each reading step is 5 minutes, which is shown in Fig.(6).

The eighth stage is the divider by 24 circuit, two decade counters are used in this stage (TTL IC 74LS90), the QB output of the first counter and QC output of the second counter are fed to the two inputs of the AND gate U21(IC 74LS08), while the output of this AND gate is connected to the reset (reset to zero) inputs of the two counters (R01,R02).The reset inputs (reset to nine) of the two counters are grounded. The input of this stage is fed from the output of the stage 4(second divider by 60) with signal frequency (1/3600Hz),while the output signal frequency at point H is 1/86400Hz. The two counters of this stage reads from (00_D) to (23_D) then they reset themselves again to (00_D) and so on.

The ninth stage is the monostable(2),which is combined from U22(inverter),U23(NOR gate), and C_3 ,its input (at point H) is activated by the negative edge of the output clock of the divider by 24 circuit(stage 8) with frequency 1/86400 Hz. A positive narrow pulse(pulse width is 3μsec in this design) is generated(every 24 hours) with the same frequency at the output of this stage (at point I) as shown in Fig.(4). The output pulse width depends on the capacitance value of C_3.The IC type used for U22 is 74LS04, while for U23 is 74LS02.

The tenth stage is the integrator(2) circuit, see Fig.(2), its operation and connection circuit is similar to that of the sixth stage(integrator(2)).Also IC LM 358 is used in this stage[7,8], it integrates the DC input voltage(constant) at point (J)with a time period of R_6C_4 (where $R_6C_4 \geq 86400$ second in this stage),so the output voltage (V_K) is a ramp signal (linear increasing),see Fig.(4).The switch VCS_2 discharges the capacitor C_4 at start of every 24 hours, which it ignited by the output of the monostable(2).When the switch VCS_2 is switched on then the capacitor C_4 is discharged, so the output voltage of the integrator(2) is started with zero voltage and then it increases linearly. The relation between the output voltage V_K and input voltage V_J is[7,8]:

$$V_K = \frac{-1}{R_6 C_4}\int_0^t V_J\, dt \quad \ldots..(5)$$

Since V_J is the DC input voltage and it is constant, so

$$V_K = \frac{-V_J\, t}{R_6 C_4} \quad \ldots\ldots(6)$$

Since V_J,R_6,and C_4 are constants, so

$$V_K \propto t \quad \ldots\ldots(7)$$

and for maximum output voltage value, one can get,

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$$V_{K(\max)} = \frac{-V_J t_{(\max)}}{R_6 C_4} \quad \ldots\ldots(8)$$

where R_6C_4 is the time constant.

The variable resistor VR_3 is used to set the desired DC input voltage at point (*J*), while the variable resistor VR_4 is used to match the output voltage range ($0 - V_{K(max)}$) to the reading voltage range (0 – 500mV) of the hours indicator (stage 11).The hours indicator has a scale of 24 steps (00 – 23), each reading step is 1 hour, which is shown in Fig.(7). The final timing diagram of the proposed system is shown in Fig.(5), which it shows the most important seven signals of the system.

3-The Practical Design and Results

One can design the proposed system by using some formulas and equations which they are discussed in the previous section.

At first, the designer must determine the values of R_3 , R_4 , VR_1 , C_2, of the integrator (1) (which is the integrator of the minutes part).

From the previous section one can see that $R_4C_2 \geq 3600$ sec.
Now let C_2= 1000μf , R_4= 3.9MΩ.So,

$R_4C_2 = 3.9 \times 10^6 \times 10^3 \times 10^{-6}$ = 3900 sec, which is ≥ 3600 sec.

And one can let $V_{G(max)}$ = 1 Volt, which is ≥ 500 mV(this is the maximum reading voltage of the minutes signal indicator), so by using equation (4) ,one can calculate V_F , where,

$$V_F = \frac{-V_{G(\max)} R_4 C_2}{t_{(\max)}} \quad \ldots\ldots(9)$$

Where, $t_{(max)}$ = 3600 sec, R_4C_2 = 3900 sec,

$$\text{So, } V_F = \frac{-3900}{3600} = -1.0833 Volt$$

Now let R_3 = 10KΩ, one can calculate the value of VR_1 by using the voltage divider rule at point (*F*),with ignoring the branch of R_4 that is in series with the high impedance of the inverting input of the integrator(1)[8,10,11], so,

$$V_F = \frac{-5VR_1}{R_3 + VR_1} \quad \ldots\ldots(10)$$

So,

$$VR_1 = \frac{-V_F R_3}{V_F + 5}$$

$$= \frac{1.0833 \times 10000}{-1.0833 + 5}$$

= 2.766KΩ

By using a standard variable resistor 3.3 KΩ for VR_1 and set it at 2.766KΩ.Then set the variable resistor VR_2 to a value that make the minutes signal indicator to read the maximum reading at $V_{G(max)}$ =1 Volt.

Similarly one can determine the values of R_4 , R_6 , VR_3 , C_4 of the integrator(2) (the integrator of the hours part).

From the previous section one can see, $R_6C_4 \geq 86400$sec.
Let C_4 = 10000μf and R_6 = 9.1MΩ, so .

$$R_6C_4 = 10000 \times 10^{-6} \times 9.1 \times 10^6$$

= 91000 sec

, which is ≥ 86400 sec.

Now let $V_{K(max)}$ = 1 Volt, this value is ≥500mV (this is the maximum reading voltage of the hours signal indicator), so one can calculate V_J by using equation (8),where,

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$$V_J = \frac{-V_{K(\max)} R_6 C_4}{t_{(\max)}} \quad \text{.....(11)}$$

where $t_{(max)}$ here is equal to 86400 sec, and R_6C_4 = 91000sec. So,

$$V_J = \frac{-91000}{86400} = -1.053\,Volt$$

Now let R_5 = 10KΩ, so one can calculate the value of VR_3 by using the voltage divider rule at point (J), by ignoring the branch of R_6 that is in series with the high impedance of the inverting input of the integrator(2)[8,10,11], so,

$$V_J = \frac{-5VR_3}{R_5 + VR_3} \quad \text{.....(12)}$$

So, $$VR_3 = \frac{-V_J R_5}{V_J + 5}$$

$$= \frac{1.053 \times 10000}{-1.053 + 5}$$

=2.668KΩ

By using a standard variable resistor 3.3 KΩ for VR_3 and set it at 2.668KΩ.Then set the variable resistor VR_4 to a value that make the hours signal indicator to read the maximum reading at $V_{K(max)}$ = 1 Volt. At this point the design is completed.

The theoretical results are indicated in figures (8), (9), which show the linear relationship between the signal outputs of the integrators (1),(2) with the time, whereas, Fig.(8) shows that the output voltage of the integrator(1) is forward linearly related to the time, where at zero volt the time is zero, while at maximum output voltage ($V_{G(max)}$) which is 1 Volt, the time is 3600 sec (or 1 Hour).Fig.(9) shows that the output voltage of the integrator (2) is forward linearly related to the time, where at zero output voltage the time is zero, while at maximum output voltage ($V_{K(max)}$) which is 1 Volt, the time is 86400 sec (or 24 Hours).

The practical results are indicated in figures (10),(11), whereas, Fig.(10) shows the forward linear relation between the signal output(voltage) of the integrator(1) versus the time, as shown, there are 27 reading(measurement) points in this figure, which it so approaches to results of Fig.(8).The linear relation between the signal output of the integrator (2) versus the time is shown in Fig.(11), and there are 18 reading(measurement) points in this figure, which it so approaches to results of Fig.(9).

The practical results and the theoretical results are approximately identical, but there are a few deviations due to the existence of the electromagnetic field (50 Hz) that surrounds the practical circuit board, and the output DC voltage of the power supply(+5 ,-5 Volt) is not pure 100%.

Finally, the complete designed system is made on the printed circuit board with the minutes and hours signal indicators, which is shown in the figures(12),(13).

4-Conclusions

From the review to the practical, simulation and theoretical results, several features arise that are of importance to state.

TTL ICs are used in the digital part of the proposed system, which they operate with 5Volt power supply.

The proposed system has a digital part that consists of logic gates, counters and monostable multi-vibrators, and it has an analog part

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that consists of integrating amplifiers.

The proposed system is fed by split power supply (+5 , 0 , -5) Volt, and it consumes (≈ 0.55 Watt).

Timing accuracy of the proposed system can be adjusted by varying the trimmer capacitor VC_1.

The proposed system uses the military system {(00-23) hours} for showing the hours output.

The proposed system is implemented on a printed board has an area of $(12 \times 12) cm^2$.

Minutes and hours outputs only are shown in the proposed system , while the showing of the seconds output is ignored.

5-References

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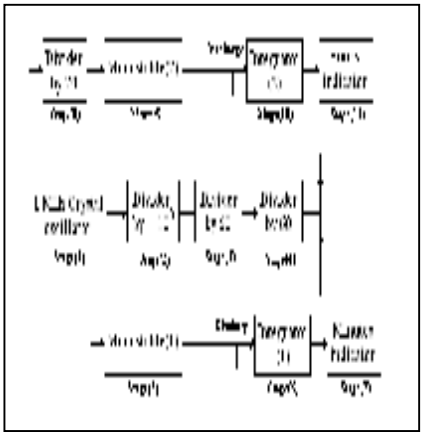

Figure (1) The block diagram of the proposed system.

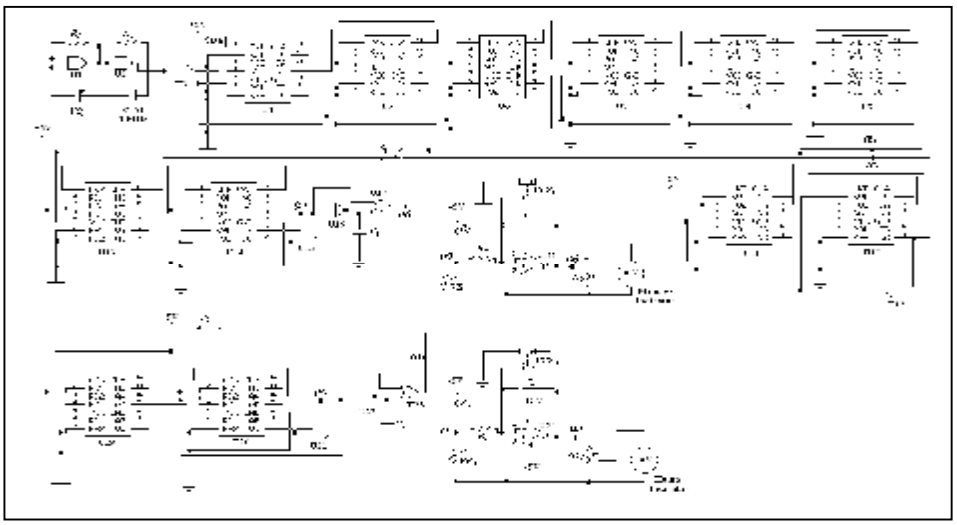

Figure (2) The complete circuit diagram of the proposed system.

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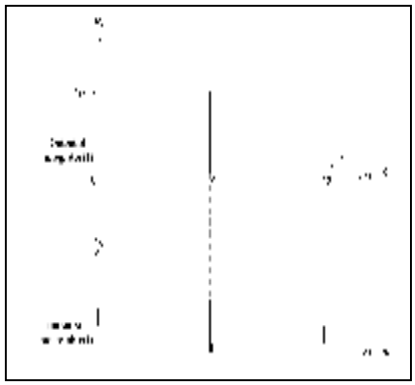

Figure.(3) The output signals of integrator (1) and monostable (1).

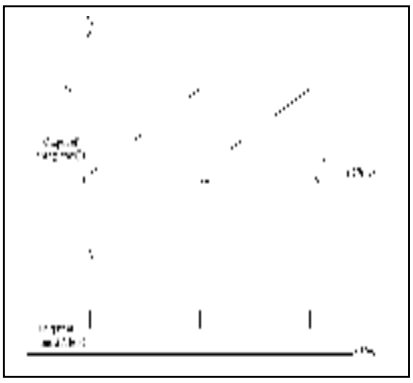

Figure.(4) The output signals of integrator (2) and monostable (2).

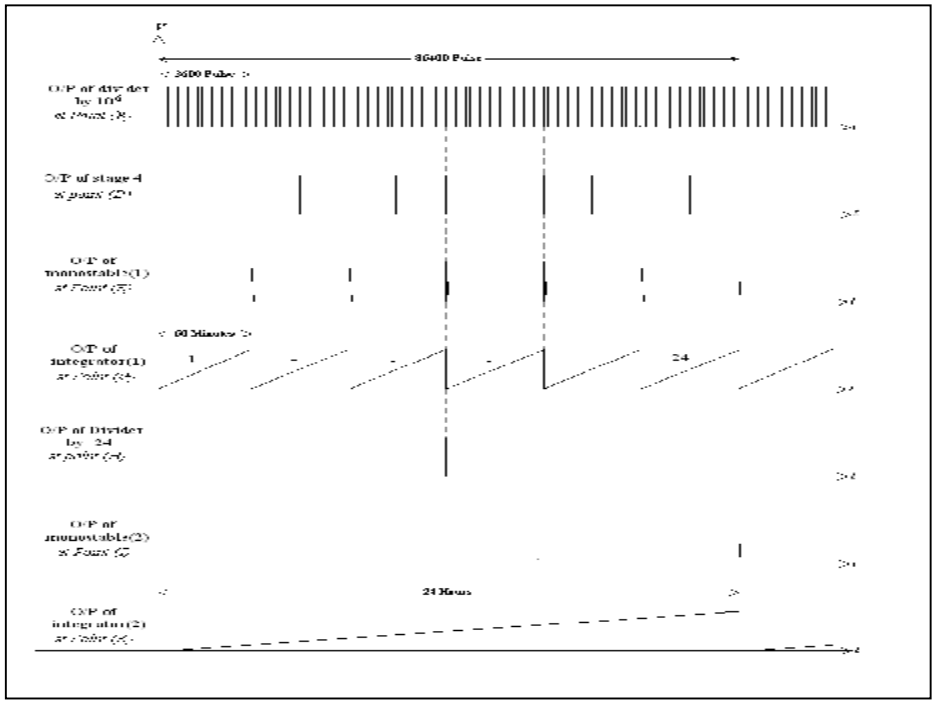

Figure.(5) The timing diagram of the proposed system.

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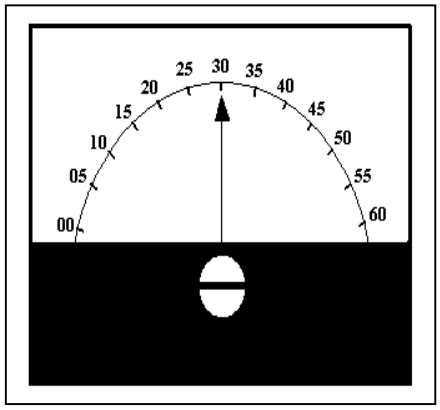

Figure.(6) The minutes indicator of the proposed system.

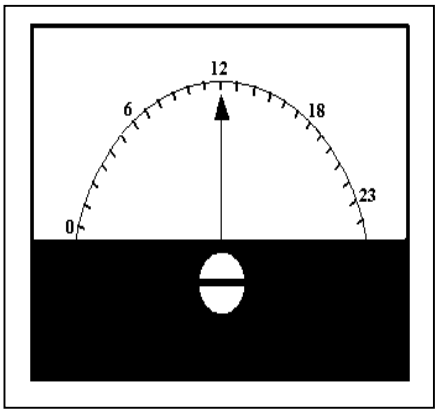

Figure.(7) The hours indicator of the proposed system.

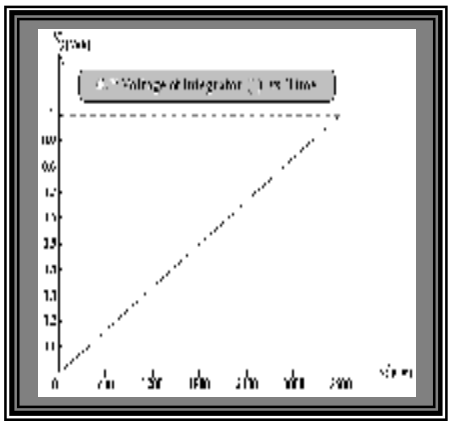

Figure.(8) Theoretical output results for the minutes stage of the proposed system.

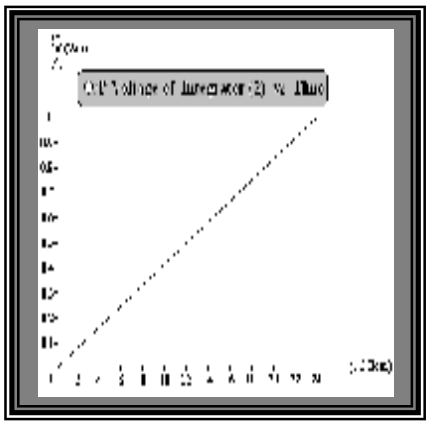

Figure.(9) Theoretical output results for the hours stage of the proposed system.

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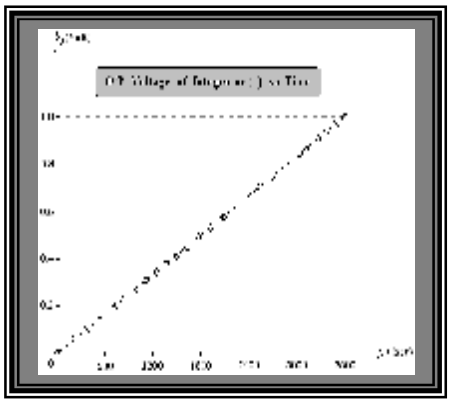


Figure.(10) Practical output results for the minutes stage of the proposed system

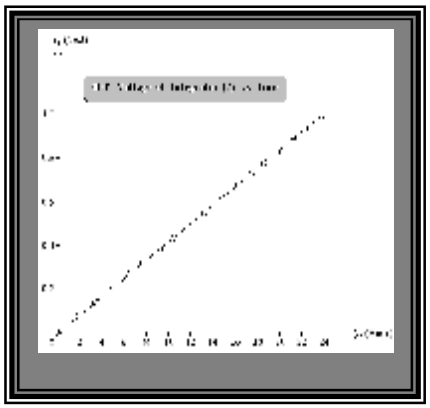
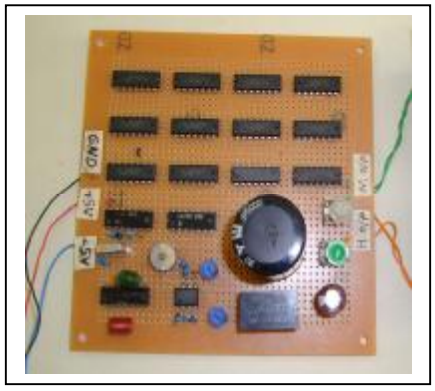


Figure.(11) Practical output results for the hours stage of the proposed system.



(a)

(b)

Figure.(12) (a) Printed circuit board of the proposed system without the indicators.
(b) Printed circuit board of the proposed system with the indicators.

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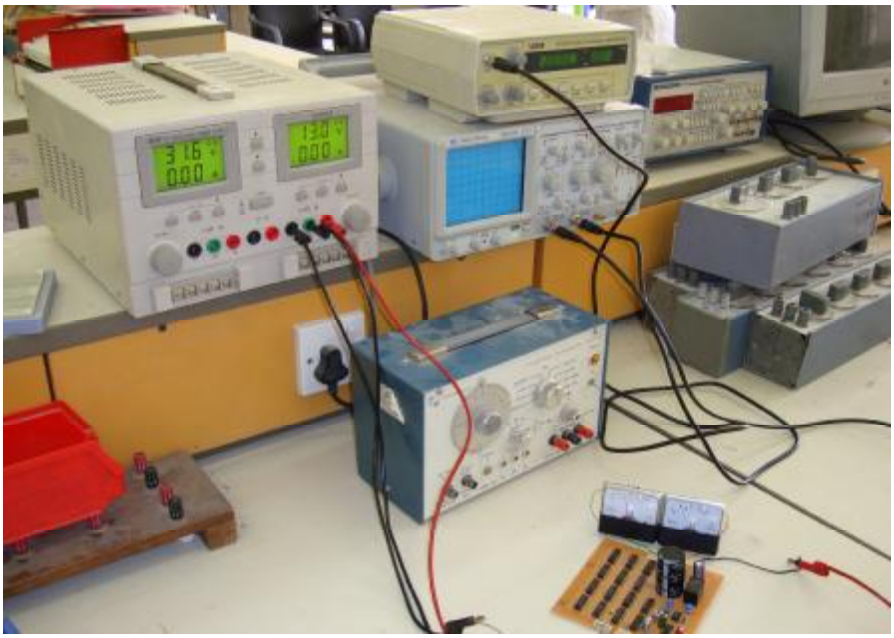

Figure (13) The proposed circuit board is tested in the laboratory.

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