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Design of DMD Nano Logic Gates With Strip Waveguides for Communication System

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HIGHLIGHTS

- plasmonic waveguides; optical logic gates; square ring resonator.

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ABSTRACT

COMSOL software is used to build and quantify optical logic circuits using plasmonic square ring resonators. An operation utilizing constructive and destructive control along with input port interferences as inputs results in the proposed gates. At 1010 nm resonance wavelength, the transmission threshold is 30% at a single interface, the ratio of input power to output optical power. All plasmonic gates are executed within a singular structure measuring 150 nm by 150 nm. The OR gate and the AND gate exhibit transmission rates exceeding 100%, with both reporting a rate of 221%. The OR and AND gates exhibit modulation depth (MD) values of 96.38 percent, whereas the NOR gate demonstrates a value of 99.8 percent, these optical gates are used in transceivers for communication systems

I. INTRODUCTION

The term "surface plasmon polariton" (SPP) is used to describe the waves produced at the metal-dielectric contact [1]. Among their many appealing features is the fact that they eliminate the diffraction limit for light waves in waveguides; consequently, SPP allows for the flow of light waves inside conduits with diameters that are half of the operational wavelength or smaller, drastically reducing device size [2]. Biosensing [3] and the installation of electrical circuits [4], [5], [6], [7] are only a few of the various uses for SPP. Propagation loss, also known as propagation length, is the largest obstacle for SPPs. SPPs can only travel a certain distance before their supporting power starts to degrade significantly. Various attempts have been made to find a balance between propagation loss and wave confinement, leading to the development of new waveguide structures such as metal-slot, dielectric-metal-dielectric (DMD), nanoparticle, channel, and metal-dielectric-metal waveguides [8] show in *Fig. 1*. Since only TM mode is supported by SPP waveguides [9], that mode is the only one considered

in this study. The transfer matrix approach [10] provides precise answers and pricing for analyzing plasmonic waveguide modes. There have been several recent developments in plasmonic logic gates, each with its own unique structure, resonance frequency, material, and transmission quantity [11], [12], [13].

Using a square ring resonator and silver strips, this study presents the design, analysis, and simulation of three plasmonic logic gates with identical structure, resonance frequency, and threshold.

Here is how this document is structured: The theoretic ideas and layout system are demonstrated in SectionII. SectionIII explain the suggested plasmonic logic gate architecture. In section IV, a review of relate literature is provided, and in section V, the study's findings and conclusions are presented.

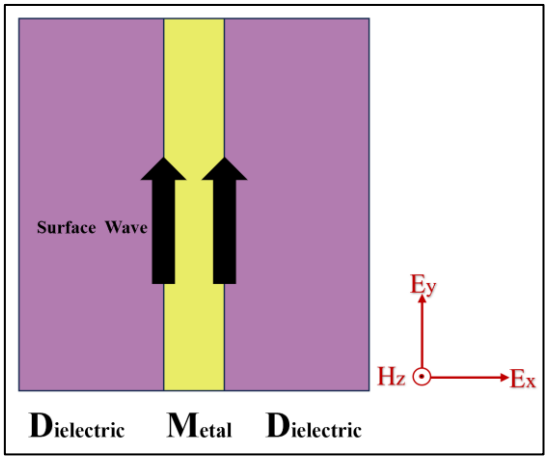

FIG. 1. DMD PLASMONIC WAVEGUIDE CONFIGURATION [8].

II. MATHEMATICAL DESCRIPTION OF THE MODEL

This work proposes the structures of plasmonic waveguides for gate design, utilizing silver as the metallic component and Zinc Oxide (ZnO) as the dielectric material. The plasmonic substructure measures 150 nm × 150 nm, comprising a single square silver resonator with outer and inner side lengths of 70 nm and 50 nm, respectively, along with four stripes each 10 nm wide. The ZnO occupies the residual portion of the structure, as illustrated in *Fig. 2*.

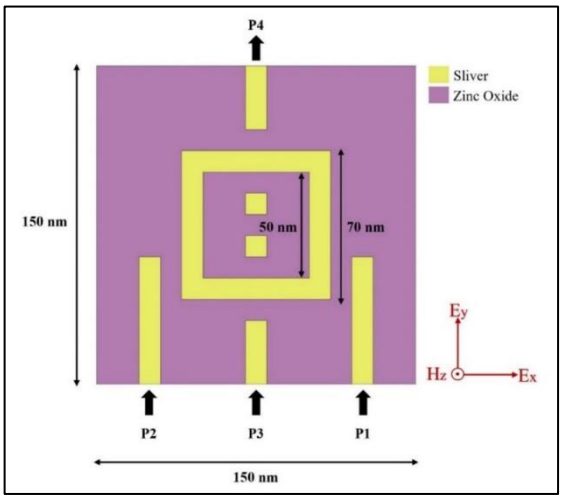

FIG. 2. THE COMPLETE PLASMONIC DESIGN.

Fig. 3 shows the four ports that make up the plasmonic logic gate. One port is for output, two are for input, and one is for control. Facet waves are excited by launched TM-polarized wave plane at the input and control ports. Data from Johnson and Christy [14] are utilized to demonstrate both the silver permittivity and the Refractive index of ZnO Material, which is 1.8. Both of these properties are demonstrated by the data. The resonance situation for the ring square resonator is computed in reference to [15].

$$J = m\,(\lambda/\mathrm{Re}\,(Neff)) \qquad m = 1,2,3,\ldots \tag{1}$$

Let J symbolize the whole length of the square, m represents the integer mode number, Neff identify the effective refractive index, and λ designate the resonance wavelength. The material type and structural dimensions are critical considerations in ascertaining the system's resonance wavelength; our system operates at 1010 nm. The efficacy of the plasmonic structure, as delineated in Equation 1, is contingent upon the properties of the used materials and the magnitude of the resonant wavelength. The transverse magnetic (TM) plane wave was introduced to define the plasmonic structure as [16]:

$$\varepsilon_m . k_d = -\varepsilon_d . k_m \times \tanh\left(\frac{k_m}{2} d_m\right) \tag{2}$$

Here, εm denotes the dielectric constant of the metal, εd signifies the dielectric constant of the insulator, dm represents the thickness of the metal, while km and kd are defined by Equations 3 and 4, which correspond to the wave numbers of the metal and dielectric, respectively.

$$k_m = (\beta^2 + \varepsilon_m \times {k_0}^2)^{1/2} \tag{3}$$

$$k_d = (\beta^2 + \varepsilon_d \times {k_0}^2)^{1/2} \tag{4}$$

$$k_\circ = 2\pi/\lambda \tag{5}$$

A numerical analysis to the equations of Maxwell is obtained by using the Finite Element Method (FEM). We used the convolution perfect matched layer (CPML) for the limitation condition of the aperture that is being considered.

The efficacy of the optical logic gates was evaluated using four criteria. Initially,the transmission (T) is the optical power ratio of output to input at a single port (either a control port or an input). The Contrast Ratio (CR) is the second factor, as illustrated in Table I. It is defined as the ratio of the optical power minimal for the state ON to the utmost optical power for the state OFF. The first criterion is given on Equation (7) [17] and the second in Equation (6) [18].

$$T = \text{Output power} \;/\; \text{Input power} \tag{6}$$

The transmission value is represented by the variable T. The output power is the optical power that is present at the output port during both the logic 1 and logic 0 states. The input power is the optical power that has been allocated to a specific control port or an individual port input.

$$\mathrm{CR} = 10 * \log (\mathrm{Pout}|\mathrm{ON})\mathrm{mn}/(\mathrm{Pout}|\mathrm{OFF})\mathrm{mx} \quad (7)$$

$Pout|OFF$ represents the greatest output power of the output port while it is in the logic 0 state, whereas $Pout|ON$ represents the minimum output power port of output when it is in the logic 1 state.

The third criterion, which also serves as the response to the query, is if the dimensions of the proposed structure yield the optimal outcome. Table II presents the MD, as referenced in [19] and [20]:

$$\mathrm{MD} = (\mathrm{TON}|\mathrm{mx} - \mathrm{TOFF}|\mathrm{mn}) / \mathrm{TON}|\mathrm{mx} \quad (8)$$

TON|mx denotes the peak transmission level attained during the ON state, whereas TOFF|mn signifies the lowest transmission level recorded during the state OFF.

TABLE I. VALUES OF THE CR [22].

CR (dB)	Description	Performance
Diminutive worth	Less	Lackluster and ineffective
Equal to or less than 4 dB	Less	Approval granted
bigger than 4 dB – 8 dB	Normal	Not very high
bigger than 8 dB – 12 dB	Normal	Effective and high-quality
bigger than 12 dB – 16 dB	greater	Effective and top-notch
bigger than 16 dB – 20 dB	greater	Effective and top-notch
bigger than 20 dB	A lot greater	Effective and top-notch

The ‘fourth’ standard is insertion ‘loss’ (IL), measured in decibels (dB), which denotes the decrease in signal intensity from the port of input to the transmission is minimum at the port of output when in the state ON, as illustrate by [21]:

$$\mathrm{IL} = 10 * \log (\mathrm{Pout}|\mathrm{ON})\mathrm{mn} / (\mathrm{Pin}) \quad (9)$$

TABLE II. VALUES OF THE MD [23].

MD	Description	Optimality in dimension
reduced by 10%	less	Lackluster and ineffective
less than 20% to 10%	less	Approval granted
less than 40% to 20%	Normal	Not very high
less than 60% to 40%	Normal	Effective and high-quality
less than 80% to 60%	greater	Effective and top-notch
less than 90% to 80%	Greater	Effective and top-notch
more than 90%	A lot greater	Effective and top-notch

One key component that can affect the optical power ratio at the output (T) is the port location, while another is the entering field's polarization and phase [24], [25]. Meanwhile, the basics of improving and eliminating interferences between the control light signal and the input light signals dictate the logic gates' performance [26], [27]. Assuming no change to other configurational elements like size, shape, material, or measurements, these two variables significantly impact performance.

III. PROPOSE OF PLASMATIC GATES

The structure in *Fig. 2* was hit by wave plane in the 800-2000 nm range at the input ports (when the ON state was present) and the control port (to activate the logic gates' functions). Our design shares a commonality among the AND and OR logic gates: they share ports. The input ports are number one

and two, the control port will be number three, and the output port will be number four. Table III illustrates that the output of an OR gate is logic 1 when a minimum of one input is in the ON state. This occurs when this condition is satisfied. It is possible to achieve this goal without having to make any adjustments to the phase difference between the ports.

TABLE III. THE T VALUES FOR THE OPTICAL OR GATE.

Inputs		**P-2**	**P-3**	**P-1**	**T**	**Output**
Logic off	Logic off	0 (0°)	1 (0°)	0 (0°)	0.08/0.3	Logic off
Logic off	Logic on	0 (0°)	1 (0°)	1 (0°)	0.79/0.3	Logic on
Logic on	Logic off	1 (0°)	1 (0°)	0 (0°)	0.79/0.3	Logic on
Logic on	Logic on	1 (0°)	1 (0°)	1 (0°)	2.21/0.3	Logic on

When the phase difference between the control signal and the input signals is zero degrees, the constructive phenomena between them causes the transmission in the OR gate to surpass 100% (2.21).

The transmission surpasses 100%, with a significant variance, as evidenced by the discrepancy between PMn |ON and PMx |OFF. This is especially noticeable when the input ports are activated. As a result, the OR logic gate exhibits a high and efficient CR [22], whereas the MD is both significant and optimal [28], as illustrated in Table IV.

TABLE IV. CR, MD, AND IL COMPUTATIONS FOR THE OPTICAL OR GATE ARE CURRENTLY BEING PERFORMED.

Output Power		CR	MD	IL
PMin |1	PMax |0			
0.79	0.08	9.94 dB	96.38 %	−1.02 dB

The OR gate is different from this. A unique structural feature of AND gates is that, like OR logic gates, their transmission levels go beyond 100% when both inputs are set to logic level 1, as illustrated in *Fig. 3*.

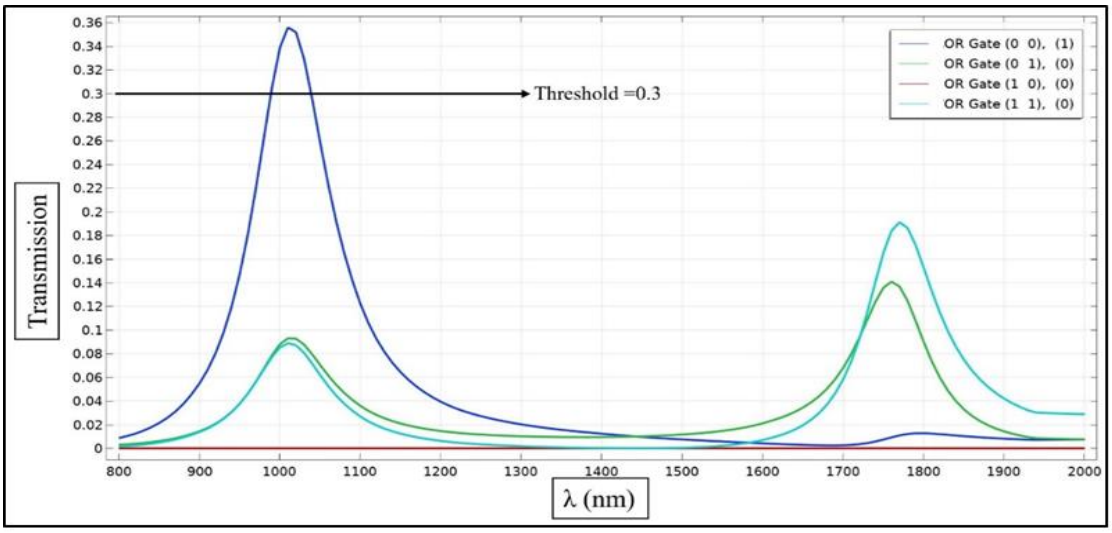

FIG. 3. THE SPECTRUM OF THE T VALUE OF THE OPTICAL OR GATE.

The AND logic gate only outputs logic 1 when both inputs are logic 1. Otherwise, it outputs logic 0. The AND logic gate creates destructive interference by creating a 180° phase difference between input ports when the inputs are opposite. This condition causes a transmission value below 0.3, resulting in a logic 0, while the control port remains ON , as illustrated in Table V.

TABLE V. OPTICAL AND GATE T VALUES.

Inputs		**P-2**	**P-3**	**P-1**	**T**	**Output**
Logic off	Logic off	0 (0°)	1 (0°)	0 (0°)	0.08/0.3	Logic off
Logic off	Logic on	0 (0°)	1 (0°)	1 (180°)	0.09/0.3	Logic off
Logic on	Logic off	1 (180°)	1 (0°)	0 (0°)	0.09/0.3	Logic off
Logic on	Logic on	1 (0°)	1 (0°)	1 (0°)	2.21/0.3	Logic on

The transmission surpasses 100%, with a significant variance, as evidenced by the discrepancy between PMn |ON and PMx |OFF. This is especially noticeable when the input ports are activated. As a result, the AND logic gate exhibits a high and efficient CR,MD and IL, as illustrated in Table VI.

The Spectrum of the T value of the optical AND gate, as illustrated in *Fig. 4*.

TABLE VI. AN OPTICAL AND GATE'S CR, MD, AND IL CALCULATIONS.

'Output Power'		CR	MD	IL
P Min|ON	P Max|OFF			
′2.24′	′0.09′	′13.9dB′	′96.38%′	′3.44dB′

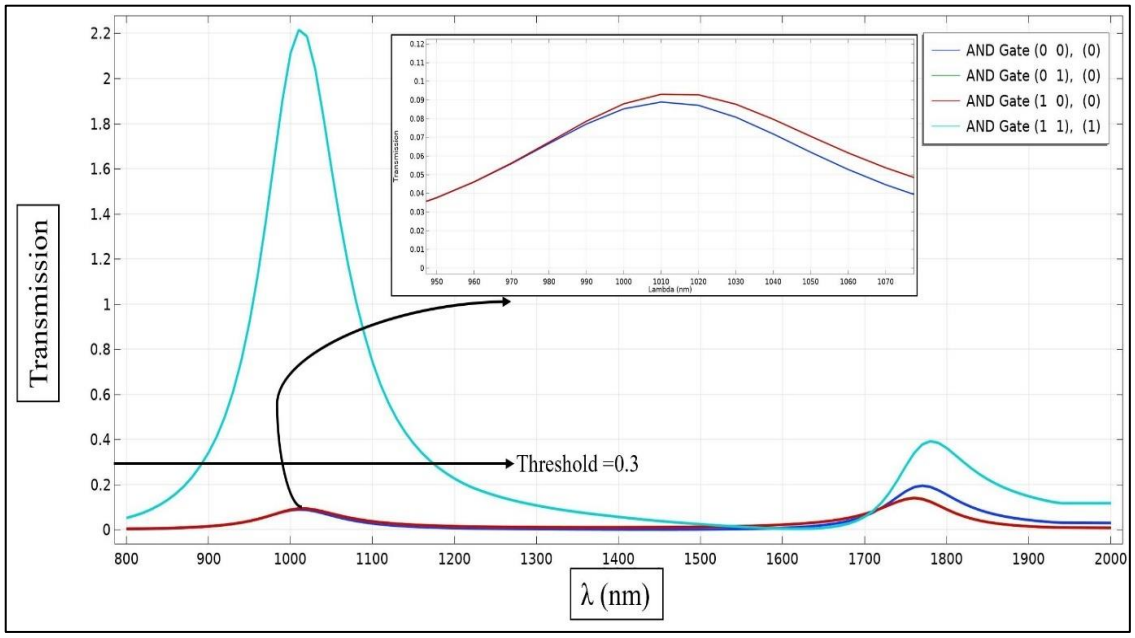

FIG. 4. THE SPECTRUM OF THE T VALUE OF THE OPTICAL AND GATE.

A NOR plasmonic logic gate will only produce a logic 1 output when both of its input terminals are set to logic 0. A phase difference of 180° was implemented between port 3 and port P2 to mitigate adverse interference in scenarios where the input ports were in opposing states (OFF-ON). The outcome yielded a transmission value of 0.09, which is below the established threshold of 0.3, resulting in a logic 0 at the output port. Similarly, harmful interference was identified as occurring due to a 180-degree phase shift when the input terminals were in opposite states (ON-OFF) as illustrated in Table VII.

TABLE VII. THE T VALUES ASSOCIATED WITH THE OPTICAL NOR GATE.

Inputs		P-2	P-3	P-1	T	Output
Logic off	Logic off	0 (0°)	0 (0°)	1 (0°)	0.355/0.3	Logic on
Logic off	Logic on	0 (0°)	1 (180°)	1 (0°)	0.09/0.3	Logic off
Logic on	Logic off	1 (180°)	0 (0°)	1 (0°)	0.0005/0.3	Logic off
Logic on	Logic on	1 (0°)	1 (90°)	1 (180°)	0.08/0.3	Logic off

The discrepancy between PMn |ON and PMx |OFF. This is especially noticeable when the input ports are activated. As a result, the NOR logic gate exhibits a high and efficient CR,MD and IL, as illustrated in Table VIII.

TABLE VIII. CALCULATIONS THE OPTICAL NOR GATE FOR THE CR, MD, IL.

Output Power		′CR’	‘MD’	′IL’
′P Min |ON	′P Max |OFF′			
0.355	0.09	6 dB	99.8 %	−4.5 DB

This section outlines the minimal transmission observed at the output port of our structure under all conditions for plasmonic logic gates, recorded at 0.0005 against a threshold value of 0.3. The Spectrum of the T value of the optical NOR gate, as illustrated in *Fig. 5*.

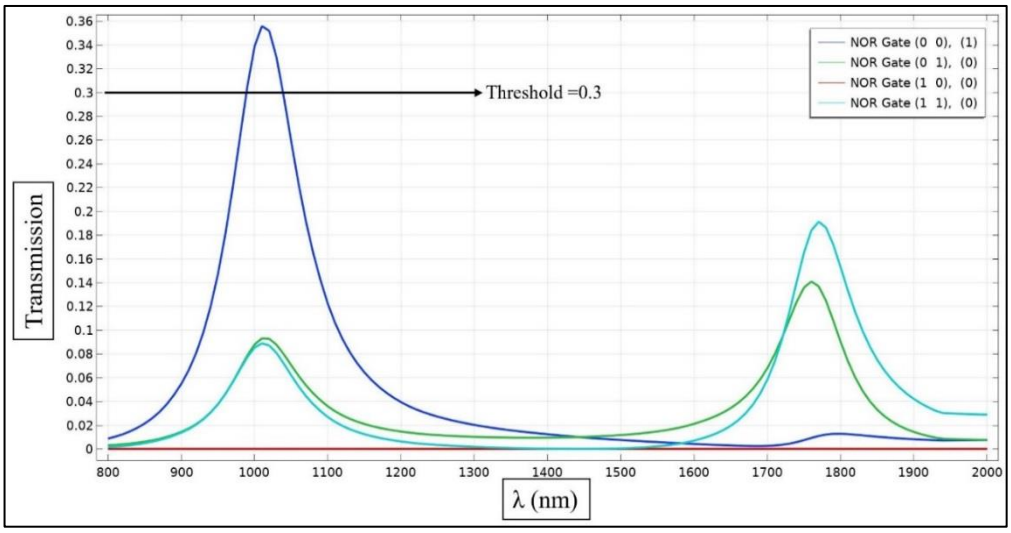

FIG. 5. OPTICAL NOR GATE T VALUE SPECTRUM.

IV. PROPOSED WORK VERSUS PREVIOUS WORKS

The proposed study is compared to a number of recent prior works show in *Fig. 6*, some of which are detailed in Table IX.

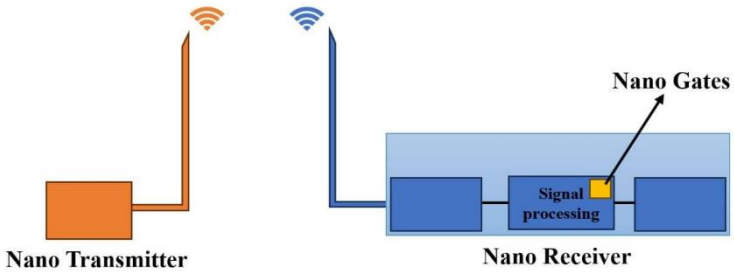

FIG. 6. NANO GATES IN RECEIVER.

TABLE IX. THE SUGGESTED VERSUS PREVIOUS WORKS.

Criteria	**This Work**	[15]	[12]	[11]	[29]
Method	FEM	FEM	FEM	FDTD	FEM
Number of gates	3 GS	7 GS	3 GS	4 GS	5 GS
Size	150 nm × 150 nm	400nm×400nm	17.12μm^2 19.6μm^2	1000nm×3200nm	200nm×400nm
λ	1010nm	1310nm	1550nm	1550nm	1550nm
Dielectric	ZnO	C2F4	SIO_2	SIO_2	Silica
Metal	Silver	Silver	Silver	Silver	Ag
Parameters	CR, MD and IL	CR, MD and IL	CR	CR	CR
Threshold	30 %	30 %	63%	20 %	30 %
Amplification	Yes	Yes	Yes	No	No

V. CONCLUSION

A novel plasmonic waveguide architecture is introduced in this work. The three binary logic gates—OR, AND, and NOR—could be implemented using this construction. By utilizing coupling theory and material properties, the gates may accomplish transmission at the output port. One way to manage the output port's transmission magnitude is to position the input and control ports in a certain way or change the phase of the light that hits them. The conclusion is that it is feasible to create Within the same structure, there are plasmonic logic gates that are enclosed. Some of these gates are capable of amplifying transmission. A transmission threshold value of 30% enables the output port to differentiate between logic 1 and logic 0. As a consequence, the gates began to operate at a wavelength of 1010 nanometers. These actualized gates are the building blocks of communication systems.

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