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Fabrication and Characterization of High Efficient CdS/Si Heterojunction Solar Cells

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Abstract

In the present paper, CdS/Si heterojunction solar cell has been made by vacuum evaporation of CdS thin film onto monocrystalline silicon substrate. XRD measurements approved that CdS film is a hexagonal Wurtzite structure. Electrical characterization of the cell shows that the carrier transport mechanism is consistent to the tunneling-recombination model. The junction of this combination was abrupt with 0.62 eV built-in potential. Spectral responsivity measurements demonstrated two distinct peaks, the first one was at 550 nm wavelength which corresponds to the CdS bandgap, while the second at 800 nm. The fabricated cell exhibits good performance with 6.3% conversion efficiency.

Keywords: CdS/Si Heterojunction, Solar Cell, Conversion Efficiency.

تصنيع ودراسة خلايا CdS/Si الشمسية الهجينة عالية الكفاءة

الخلاصة

في هذا البحث، تم تصنيع خلايا شمسية هجينة نوع CdS/Si وذلك بتبخير أغشية CdS الرقيقة على قواعد سليكونية أحادية البلورة. أظهرت قياسات الأشعة السينية أن الأغشية المحضرة ذات طور الفيرتزايت السداسي. بينت القياسات الكهربائية أن ميكانيكية نقل التيار عبر المفرق تنطبق على أنموذج الانتفاق-إعادة الاتحاد، وإن المفرق المصنع هو من النوع الحاد بقيمة جهد بناء داخلي مقدارها 0.62 eV. أظهرت قياسات الاستجابية الطيفية أن للمفرق قمتي استجابة الأولى تقع عند الطول الموجي 550 nm الذي يقابل فجوة الطاقة لغشاء CdS، أما الثانية فتقع عند الطول الموجي 800 nm. أبدت الخلايا المصنّعة أداء فولطائي ضوئي جيد بكفاءة تحويل مقدارها 6.3%.

Introduction

There has been considerable interest in recent years directed towards the development of heterojunction solar cells [1-3]. Such interest is based on the fact that these heterojunctions have a number of advantages over diffused p-n junction solar cells include [4]: (i) a lower junction-formation temperature, (ii) higher spectral response at short wavelengths, and (iii) many of deposited layers have the right indices of refraction to act as antireflection coating. In the last three decades, CdS/Si heterojunction solar cells have been reported to have power conversion efficiencies of 4% and greater [5-8]. These cells were considered as low–cost and high efficient photovoltaic devices. The cost reduction obviously will be in the junction–formation step and also in eliminating the antireflection layer.

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The aim of this paper is to present the results of the fabrication of n-CdS/p-Si heterojunction solar cell made by thermal resistive technique.

Experimental Procedures

Single-crystal silicon wafers of p-type conductivity with (111) orientation are used as substrates. They have a resistivity in the range of 1-5 □-cm and one face of the wafer is polished to the mirror-like surface.

Prior to deposition of CdS, these wafers were chemically etched in dilute hydrofluoric acid to remove native oxides.

Subsequently, after oxide removing, the wafers were scribed into individual pieces of 0.5 cm^2 sizes, then they were sent to vacuum chamber to fabricate the CdS/Si heterojunction.

The deposition of CdS films was carried out by vacuum evaporating of ultra-pure CdS powder (5N) onto silicon substrate. The evaporation was done by using Balzer coating system. Thickness of deposition film was about 300 nm which calculated from the gravimetric method.

After the deposition of CdS, frontal and back metal electrodes were formed by depositing 200 nm of In and Al respectively. The sensitive area was about 0.2 cm^2.

Spectral responsivity measurements of CdS/Si heterojunction detectors were made by using a monochromator (MODEL 746) in the range 400-1100 nm. The results were calibrated by measuring the power of each spectral line using a standard power meter.

J-V measurements were done under dark and illuminated conditions. The illumination was achieved by halogen lamp type "PHILIPS", 120W, which connected to a Variac and calibrated at AM1 illumination power density by a silicon power meter.

The crystalline quality of the grown layer was investigated with aid of XRD apparatus of the wavelength of 1.940 Kxu. After determining lattice constant of CdS epitaxial layer from the peak position of the XRD pattern, strains were calculated from the relation [9]:

$$\text{Strains}=(a_{CdS}- a_{XRD}/a_{CdS})\times 100\% \quad (1)$$

where a_{CdS}: Lattice constant of CdS from ASTM, a_{XRD}: Lattice constant of CdS epilayer determined from XRD pattern.

Results and Discussion

The XRD result pattern of CdS /Si heterostructure for as-deposited sample is shown in Figure 1. The sample shows polycrystalline phase. Reflection peaks from (100) plane, (002) plane, and (101) plane were observed. This orientation corresponds to the hexagonal phase (according to ASTM card No. 6-0314). Accordingly, evaporated CdS film shows Wurtzite structure.

The lattice parameter of (002)-oriented CdS film from ASTM-Card is 6.75 Å, while that obtained from XRD pattern is 6.74 Å. This will result in strains, The strain calculated from previous results was 0.14%.

Dark I-V characteristics of the fabricated heterojunction are presented in Figure 2. The outline of the curve exhibits poor-rectifying behavior (e.g. rectification factor about 20 at 1 V). The forward current varies exponentially while reverse current demonstrates soft breakdown behavior and can be described by two distinct regions; in the first one the

current is explained by a relation similar to that of the eqn. (I α V), in the second region the current can be depicted by the eqn. $I \alpha V^m$, where m<1.

A semi-log J-V plot under forward bias is presented in Figure 3. This figure shows that forward current consists of two regions. The first one represents the recombination current, while the second region represents the tunneling current, i.e. CdS/n-Si heterojunction obeys to the tunneling-recombination model. This result is not in contradiction with results obtained by other workers for CdS/Si heterojunction prepared by vacuum evaporation [10,11]. The saturation current density of the first region J_{S1} is determined by extrapolating J-V curve of this region to find its intercept with V=0. Thus, the ideality factor n is calculated by the following equation [12]:

$$n = \frac{q}{kT} \cdot \frac{\partial V}{\partial \ln(I_{f1} / I_{S1})} \quad (2)$$

where q/kT: reciprocal of the volt equivalent of temperature, I_{f1}: the forward current of the first region.

On the other hand, the saturation current density of the second region J_{S2} is determined by the extrapolation at the second region, then the value of A is extracted by the following equation [12]:

$$A = \frac{d \ln (I_{f2} / I_{s2})}{dV} \quad (3)$$

where I_{f2}: the forward current of the second region.

Figure 4 depicts the variation of the reciprocal of square capacitance versus reverse bias voltage. It is apparent that the junction is an abrupt type, and the intercept extrapolated to the voltage axis is the built-in voltage with the value of 0.62 eV. This value exhibits fair agreement with that prepared by vacuum evaporation technique [6].

Figure 5 presents spectral responsivity of the fabricated cell. It is noticed that the responsivity curve shows good band-pass behavior (window effect), and it is comprised of four distinct regions. The first region (corresponding to the blue spectral region) shows an increase in responsivity with wavelength, attains the maximum value at λ = 550 nm (the absorption edge of the CdS frontal layer). The lower responsivity at the shorter wavelength region may be due to the absorption of the light near the surface (shallow absorption depth), which has large amount of surface recombination of the photo-generated carriers. The second region of the plot shows a decrease in responsivity with a minimum value at λ = 600 nm, this could be attributed to a high degree of carrier recombination at the interface [13]. The third region shows an increase in the responsivity passing through the maximum value at λ = 800 nm corresponding to light absorption at transition region on silicon side. The fourth region shows that responsivity decrease reaching the absorption edge of the silicon 1.1 eV. The smaller responsivity at longer wavelength is ascribed to the carriers generated deep in the bulk of the silicon [14].

The photovoltaic performance under simulated AM1 condition of the cell is described in Figure 6. The curve is plotted in the fourth quadrant to represent the power extracted from the cell. It is seen from the figure that the rectangularity is low indicated the high value of series resistance that results from the high resistivity of

CdS layer. Low fill factor is expected from this figure.

Figure 7 demonstrates the variation of the output power (the power generated by the cell under simulated AM1) versus voltage across the load resistance. This figure reveals that CdS/Si heterojunction is a suitable device to produce high efficient solar cells.

Conversion efficiency of 6.3%, fill factor of 0.4, short circuit photocurrent density of 40 mA/cm^2, and open circuit photovoltage of 400 mV were obtained from Figures 6 & 7.

Conclusions

CdS/Si heterojunction solar cell showed high conversion efficiency. The high performance of this cell is coming from the suitability of CdS bandgap that lies at the interest spectral region of the solar spectrum. High resistivity of CdS layer which leads to low fill factor is the main problem of this cell, this problem can be solved by doping CdS layer with suitable dopant. Improving the cell efficiency by CdS doping is under progress.

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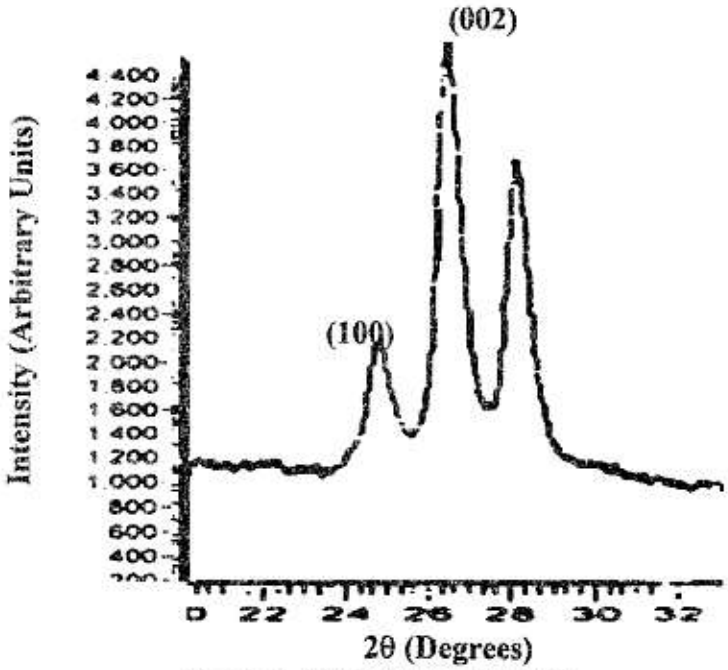

Figure 1. XRD Pattern of CdS film.

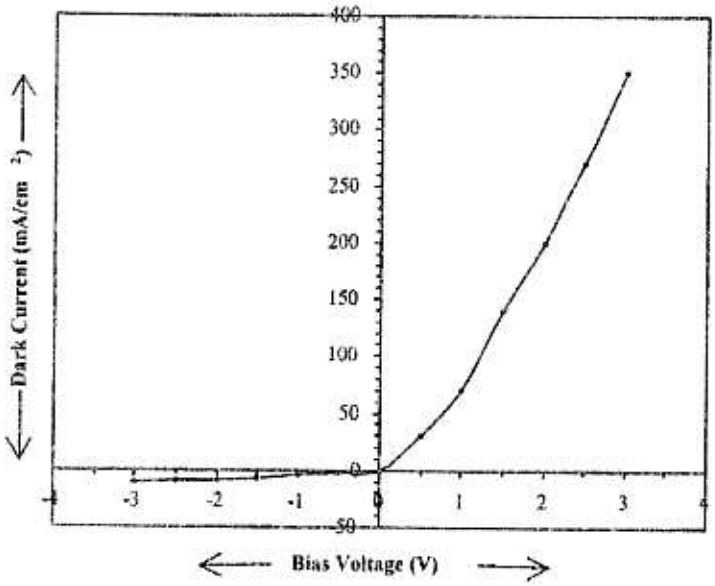

Figure 2. Dark J-V Characteristics.

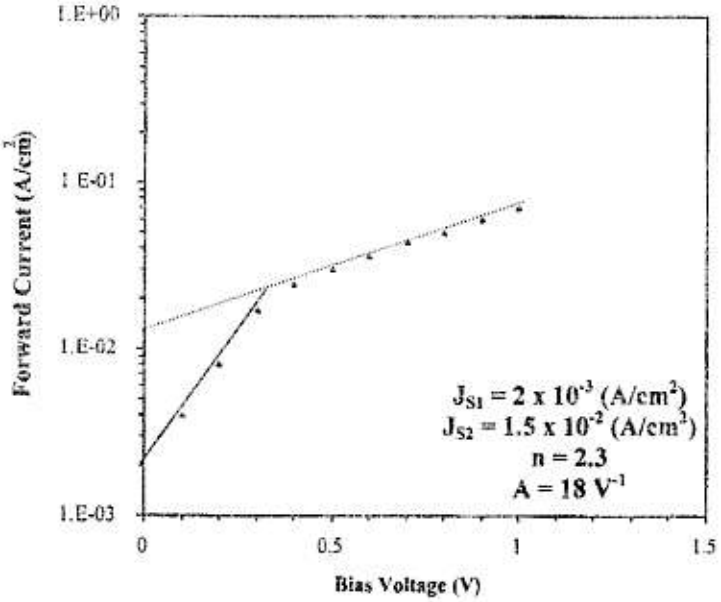

Figure 3. Semi-log J-V Curve.

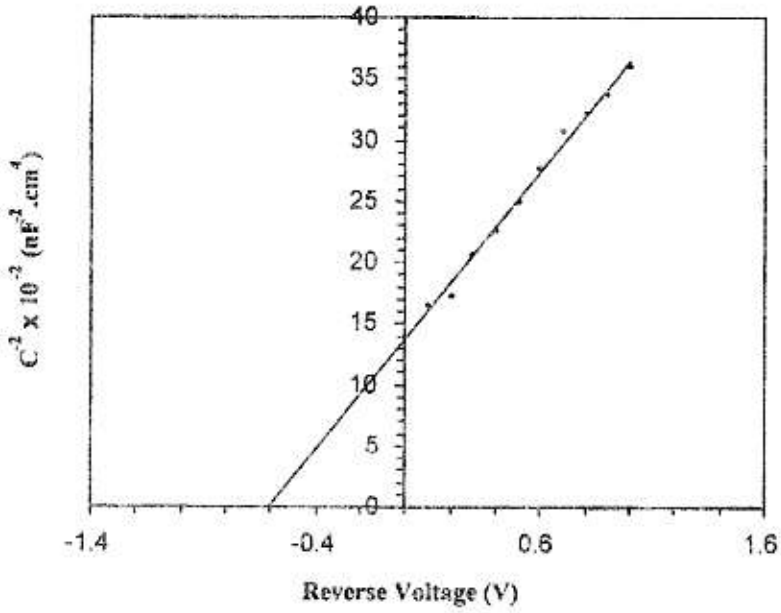

Figure 4. Reciprocal of Square Capacitance vs Reverse Voltage.

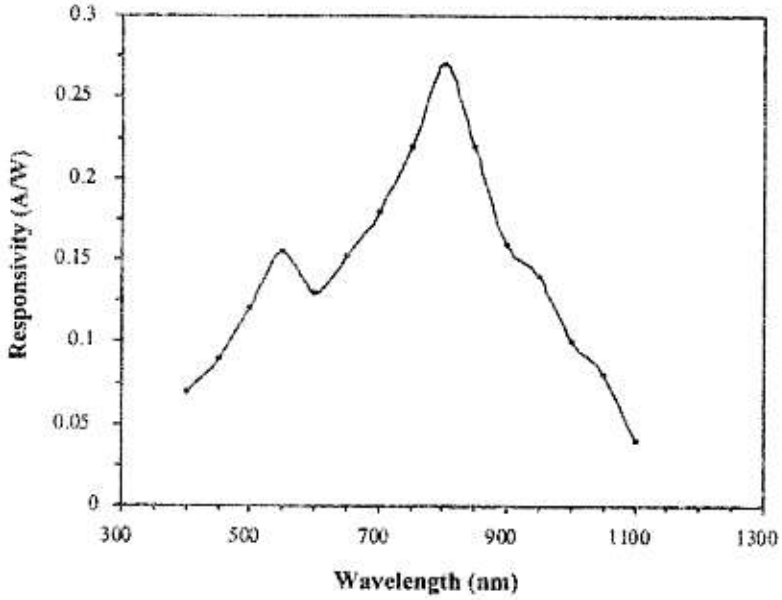

Figure 5. Spectral Responsivity Platform.

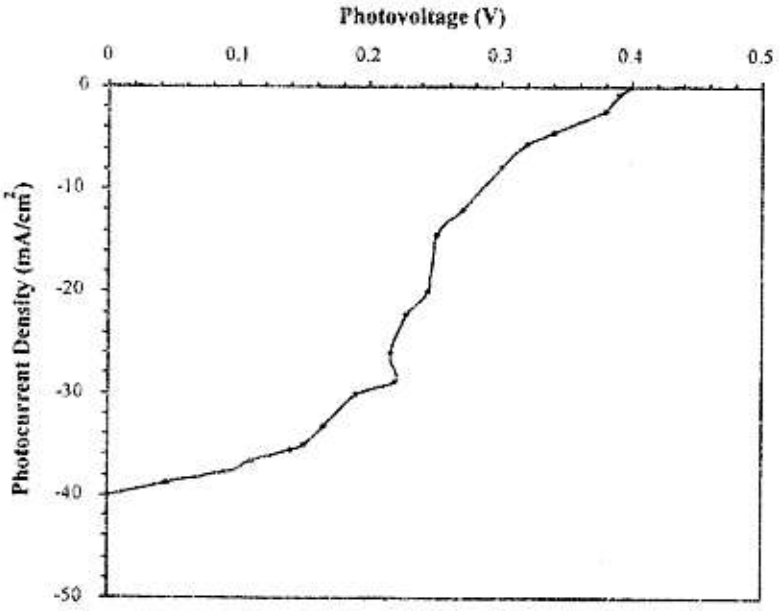

Figure 6. The Photovoltaic Performance of the Cell.

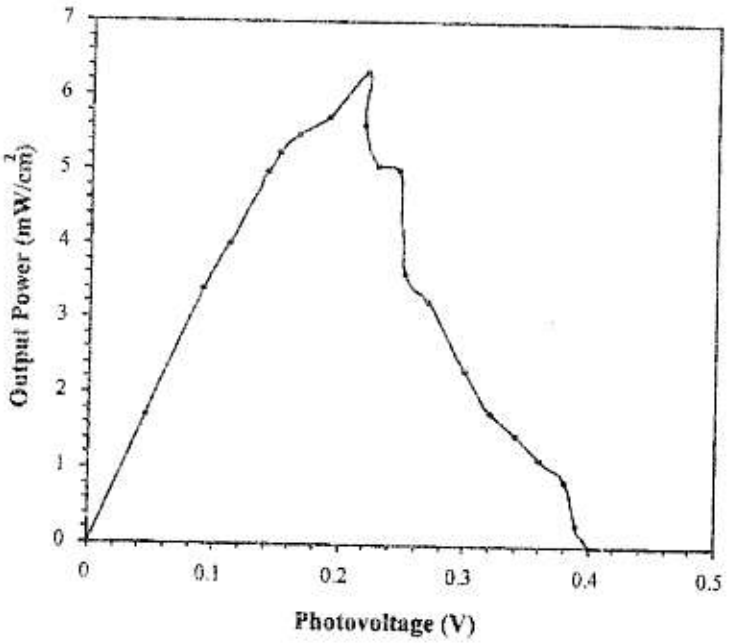

Figure 7. The Output power generated by the Cell.