ISSN: 2617-5517 (Print)
Al-Farabi Journal of Engineering Sciences
https://www.iasj.net/iasj/journal/392/issues
Published by Al-Farabi University College

Novel Design High-Throughput of Processor using Dual Computing Engine of Visible Light Communication (VLC) System for Text Transfer Based on Field Programmable Gate Arrays (FPGA)

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Abstract

An FPGA provides the user with a high level of flexibility for rapidly constructing and testing any hardware. Depending on the hardware to be implemented, it has a variety of gates. This paper investigates the of novel design architecture of a High-Throughput Processor using a dual computing engine of Visible Light Communication (VLC) system for text transfer based on Field Programmable Gate Arrays (FPGA) using a 128-bit AES algorithm combined with a UART module for the secure data text transceiver using the technology VLC system. In this work, we present a dual computing engine the design has dual processing of the processor data text size of each memory of the computing engine has 4046 words. The novel of this paper uses spatial and temporal parallelism behaviour to custom design a dual computing engine. The spatial and temporal parallelism behaviour custom design has dual data inputs and processing operates on a 50 Mhz clock technique via the VLC system. Finally, the striking results technique behaviour for design performs compared to the studies our design Frequency Maximum *Fmax* reach up to 173.34 MHz, time 5.76 µs and throughput of 2.772 Gbps. Furthermore, in the comparison between the proposed design and existing studies, our technique has higher throughput through its implementation of an FPGA DE1-SoC chipset Cyclone V SE 5CSEMA5F31C6N. Generally, the design successfully achieves its goal of testing.

Keywords: *FPGA, VLC system, Spatial and temporal parallelism, High throughput*.

1. Introduction

Researchers are pursuing Visible Light Communication (VLC) as an alternative communication system in the future. As a result of these conditions, a start-up company and several higher education institutions around the world encouraging research on VLC system technology are being developed [1]. It inspired researchers to develop its importance as a refuge in green energy and its most prominent applications are optical communication. Thus, the VLC system type of data can be used such as Video, audio, and digital images, which are among the most common multimedia. A VLC system displayed a loudspeaker with audio played directly from an SD card. Using visible light to transmit images and audio. The use of low-power LEDs for PC-to-PC image and text transfer [2]. Through a white LED, a simple text can be transmitted from PC to PC via optical wireless communication (OWC). The implementation of VLC using microcontroller technology is found in [3], [7]. Thus, there is a limit to the clock speed. VLC requires a DSP for higher throughput and low latency. In their proposal for high-speed VLC systems, they suggested the use of a field-programmable gate array (FPGA). Nevertheless, they did not use it in a real VLC system. Audio transmission systems have also been implemented using VLC technology.

According to the design's single computational engine can attain a maximum clock frequency of *Fmax* 170.97 MHz and a throughput of 1.367 Mbps [8], [9] the inner pipeline was used at two, three, or four stages on the Xilinx Virtex-5 FPGA with an *Fmax* of 576.07 MHz. High throughput is achieved by folded parallel architecture. The concept of folding can be used to improve area utilization while ensuring a high throughput whilst maintaining a high area utilization. Based on a Virtex-6 device from Xilinx, they are able to achieve an *Fmax* of 505.5 MHz. An implementation of Xilinx Virtex-5 hardware to implement the AES algorithm has been presented in more recent work [10], [11]. It has achieved a theoretical, *Fmax* of 671.5241 MHz and a throughput of 86 Gbps [12], [13].

This type of communication is widely used in serial data transmission etc. Serial data is converted into parallel data by the UART integrating circuit [14] - [16]. The AES encryption algorithm is used to encrypt each byte of data per clock cycle in the proposed design [17], [18]. The encrypted bytes are then serially shifted to the UART transmitter's input. For encryption and decryption, we use the AES-128 algorithm. 128-bit encrypted data is stored and transmitted in 47.2 seconds [19]. Iterative design principles are used in order to minimize the area for both encryption and decryption of AES-128. In the past few years, modulation and equalization technologies have greatly improved the throughput of VLC systems [20]. Research has been conducted on VLC systems, such as indoor positioning, and outdoor data stream transmission. Most studies on VLC systems focus on developing transceiver circuits that achieve higher data rates through different methods [21], [22]. Developing a higher layer of the VLC system received little attention. The motivation of this research is the novel design of a High-Throughput processor using a dual computing engine of a VLC system for text transfer based on Field Programmable Gate Arrays (FPGA). This paper focuses on verifying the possibility of increasing throughput using design behaviour spatial and temporal parallelism.

2. Method Custom Design of Dual Computing Engine Based FPGA

2.1 UART Transmitter Module

One of most basic transmitting and receiving for dual computing engine based VLC system is module UART. Here, to use UART is a serial communication has 8-bit

that converts parallel data into serial data for transmission, and then converts serial data input into parallel data output at the receiver end. Basic UART communication needs single signal line (RX, TX) to complete half-duplex data communication. TX is at the transmit side, the output of UART; RX is at the receiver side [14]. TX to send 8-bit need to add start bit, end bit to serial data each 8-bit, and total of bit will be 10 bits. Therefore, its benefits to distinguish between each transmission is a dividing line between the data set. The 128-AES algorithm has input 128-bit, to send a one character containing 8-bit, we need 16 bits able to send 128-AES algorithm encryption unit. For communication, there is an important prerequisite for controlling the traffic between the encryption and the sender The FIFO buffers of the TX_FIFO buffers is represented as back bone of computing engine. However, an FPGA does not contain a high language like Java or C++ the rest of the software [23], we need to design all components used VHDL is language hardware for platform FPGA, as shown in RTL viewer of URAT TX has been illustrated (“see Figure 1”).

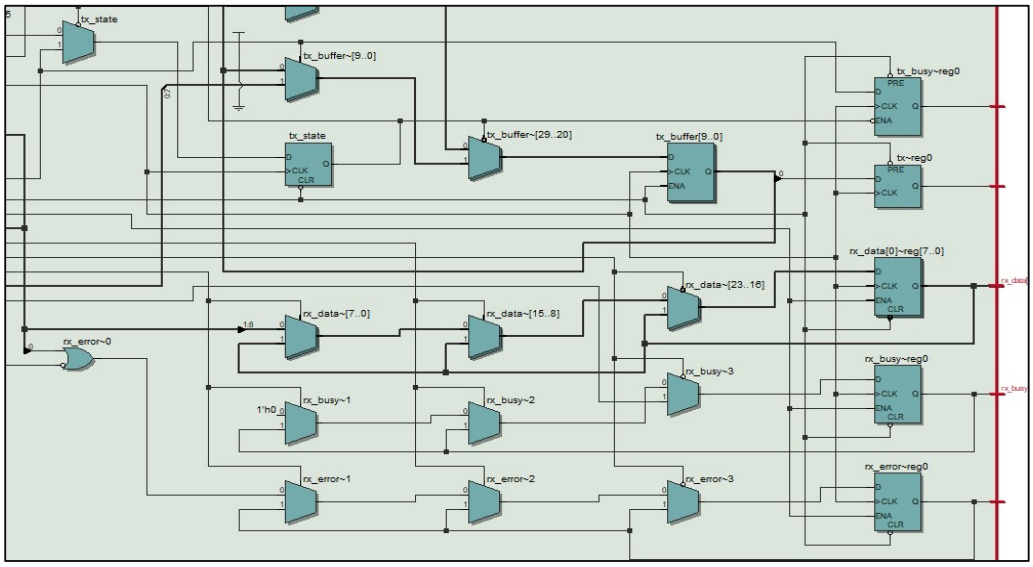


Fig. 1. RTL viewer TX UART Design.

2.2 UART RECEIVER MODULE

Here, RX receiver module that is performed the task of receiving the serial data 16-bit stream of data by RX_FIFO buffer into 128-bits AES decryption unit. Before that, the TX LED will send data as blinking high fast in which will not affected to human eye. Thus, the light detector will receive the serial data to RX, the RX remove the start bit, stop bit to getting original 8-bit data. The 128-bits AES decryption unit to return it to original value 8-bits is value represents one character, in RTL has been illustrated (“see Figure 2”).

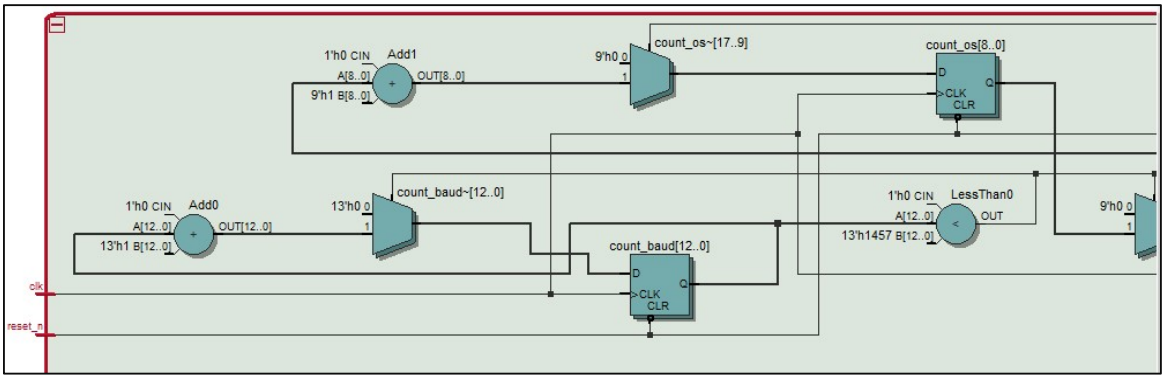
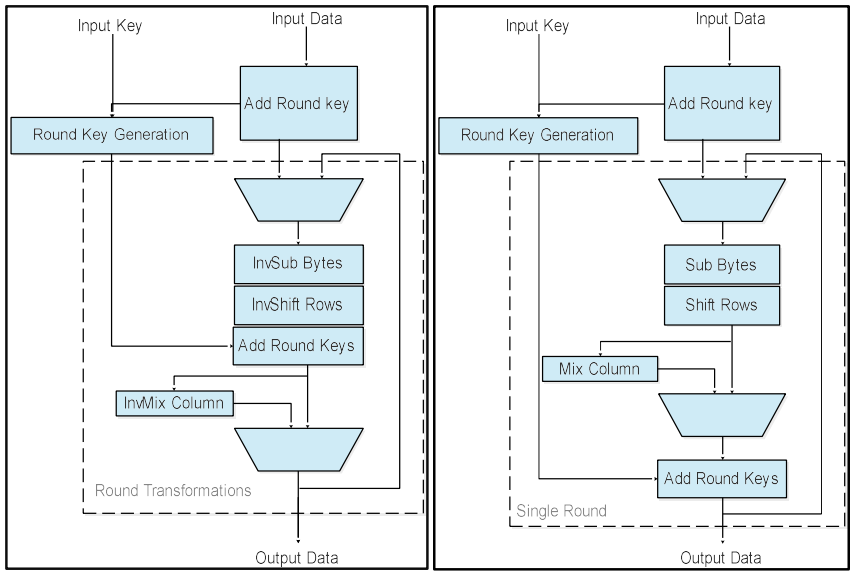


Fig. 2. RTL viewer RX UART Design.

2.3 Encryption 128-Bits AES Algorithm Function Module

In the first serial of parallel, has out shift registers are used to store the data bytes to encrypt each data packet during each clock cycle, then send them to the 128-bits AES Algorithm Encryption module. Through a serial out shift register, the 128-bit encrypted data is transmitted from the serial out shift register to the UART transmitter in parallel. The AES Encryption module is designed to perform the encryption operation on 128 bits of data using the AES algorithm, which is considered a symmetric block cipher in cryptography. A symmetric block cipher normally processes data blocks of 128 bits with three different key lengths, which are 128, 192 and 256 bits, based on the total length of the data block at hand [24]. This design is capable of supporting the encryption of 128 bits using AES Algorithm, as illustrated ("see Figure 3").



(A) (B)

Fig. 3. Block Diagram 128-bits AES Algorithm (A) Encryption and (B) Decryption.

SubBytes: in a SubBytes transformation, a state is replaced with the substitute of its byte within an s-box, and then it is transformed. In other words, an s-box can be seen as a table of invertible substitutions that are made up of a combination of two transformations [25] and [26] is a result of a combination of two transformations whose composition makes a box. The first step is to replace each byte in an affine transformation with its reciprocal, followed by it being rearranged accordingly:

ShiftRows: The transformations were applied to three rows of data at different offsets so that the bytes in the last two rows were shifted left over different offsets (the offset value is dependent on the row for which it is applied, e.g. the offset value for row 1 is 1, while the offset value for row 2 is 2, etc.).

MixColumns: In the MixColumns transformation, the state is transformed column-by-column, using a four-term polynomial to treat each column.

RoundKey: adding RoundKey to the state of a 128-bit state yields a simple bitwise XOR operation when the state and round key have the same 128-bit length. An input key with 128 bits has been extended to ten round keys of the same length by a generation unit. A round key can be generated by applying a process to a round key that has already been generated. A function module that performs the same functions as the decryption function

module can be used. During the decryption process, there are a number of different transformations are performed, including InvSub Bytes, InvShift Rows, InvMixColumns, and AddRound keys. This process of transformation is the inverse of the process of transformation that takes place in the encrypted data. In order to understand more about the process of AES-128 decryption.

2.4 VGA CONTROLLER

VGA controller is a module that controls Video Memory, Char ROM, and Shifts Register and generates synchronization signals ("see Figure 4"). As for the internal configuration, most of them are counters for timing adjustment [27]. Create, or Import peripheral created a VGA controller IP template, but only a template for the interface with the processor. The design needs to create everything for the VGA controller body. The character shall be displayed, and the number of displayed characters shall be 80x25 characters. The character structure is 8dotsx19 lines, and the character structure is 8dots x 16 lines. The remaining 3-lines are blank lines (not displayed). Therefore, the dot configuration of the entire screen is 640 dots x 475 lines. The correspondence between screen composition, character composition, and memory map. In a 32-bit processor like him at Micro Blaze, the memory address is assigned in bytes, but 32-bit (4 bytes) can be accessed simultaneously with one data read/write. Therefore, in the case of memory accessed in byte units, it will be arranged in 4 address skips. The video RAM Memory holds the JIS8 bit code of the characters displayed on the screen. Since the number of displayed characters is 80x25 characters, it is necessary to memorize 2,000 words with 8-bits. The character code of JIS8 bit code able to store 2,000 words with 8-bits. Character ROM is a memory that stores character information of characters. Since the JIS 8-bit code has 256 characters, if the composition of one character is 8dotsx16 lines, 8-bits of 4,096 words are required. In an 8-bit character code, the remaining 3-blank lines (non-display) are controlled by the next VGA Controller to realize non-display.

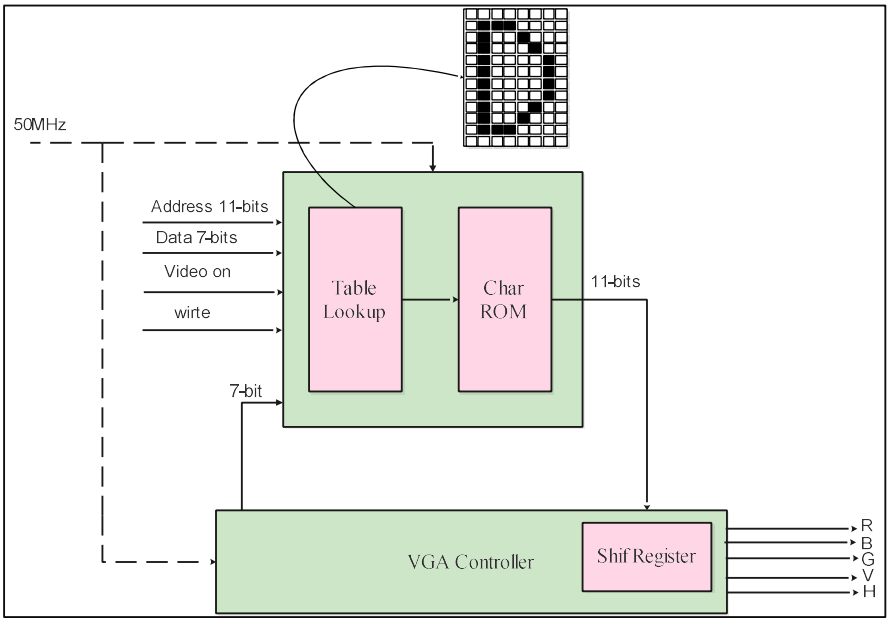


Fig. 4. Block Diagram VGA Controller.

3 PRINCIPLE OF SPATIAL AND TEMPORAL PARALLELISM

In this study [28] investigated the effects of the principle spatial and temporal parallelism mechanism present as duplicating the module task to processor data vertically and horizontally. Spatial parallelism is a feature that can be considered critical when it comes to latency and bandwidth. As an example of a parallel computing architecture that has been used in systems, the useful one is the one that has large blocks of logic that can be

executed in parallel, resulting in a series of processing being carried out simultaneously. Earlier studies have explored the impact of a concept known as spatial parallelism which states that each function has been divided into several parts and then each part will be processed by different processing elements as per the design [29] and [30]. The processor component that is used to carry out the processing task has not explicitly addressed its influence into several components based on the type of information that is being processed but rather is replicated to process each one separately. From interconnects used within a system to the entire functional units that are included within the system, the spatial parallelism feature can be exploited at many levels of the system construction. At the communication and interconnect level, parallelism at a spatial level is exploited to the fullest extent. It has been proposed to optimize the system by utilizing End-to-End or (Multiple Physical links) to achieve scalable features and lower costs for system components by using end-to-end or multiple physical links [31].

It is essentially a method of partitioning the processing tasks into several stages, which is what temporal parallelism is all about. In other words, application of the same mathematics to each unit of information, produces the same results as when it was approached sequentially. Basically, the task is partitioned in time, each step of the task applies to a separate unit of information, which is used to describe how the task is carried out. It is typical for an assembly line manufacturing process to be used as an example. Parallel processing creates pipelined structures in computing when temporal parallelism is used in computing. As a general matter, a pipeline will take a little longer to produce any given result than a pipelined system, as in practice, the pipeline produces the same result more slowly. In spite of this, the rate at which results are produced increases in proportion to the number of steps one divides the original task into, as the results are produced at a greater rate [32]. A space parallelism system used in interconnects and in communication levels represents a method of improving the throughput of a low-cost system using multiple computing engines linked together in spatial parallelism. In this architecture, when an event occurs, it must be determined that several functional units should be involved in detecting the reaction that occurs as a result of the event. They each have a specific number of actions to handle and are responsible for updating the status of those actions in parallel. They are all responsible for different reactions. In a fully stochastic simulation using FPGA architecture [33] and [34] has harnessed spatial parallelism. The presented architecture has a performance advantage that is over 12-30 times greater than that of the existing simulator designs and implemented on FPGA boards, which is what is compared here. Here, for this architecture implementing the dual computing engines in parallel, there should be an improvement in the throughput of the dual computers. There are, however, some downsides to this improved performance, such as that it takes time for unrolling and will increase throughput of the required FPGA less resources are required to achieve (“see Figure 5”).

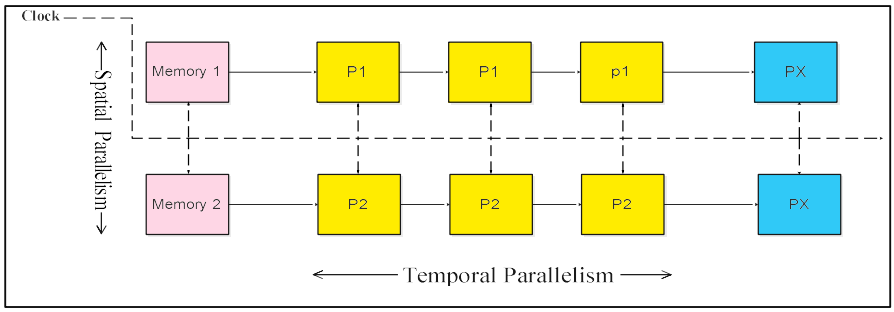


Fig. 5. Block diagram behaviour spatial and temporal parallelism.

4. Novel Design Dual Computing Engine for High-Throughput of Processor

Novel design dual computing engines, were every computing engine content three main components are URAT, 128-bit AES algorithm (encrypt and decrypt), FIFO and VGA controller. The spatial and temporal parallelism principle, to novel design dual computing engines has dual processing data text to handle by FPGA DE1-SoC to increase the throughput based VLC system has been suggested. The spatial and temporal parallelism behaviour is present in the parallel processing to novel design dual computing engines use FPGA. The design count of the processors present in the system, the system of FPGA would always try to divide his task on the basis of the number of components were present in the system. All processors here are tightly coupled and are packed in one design the following ("see Figure 6").

Parallel processing includes dual processors, which use a dual bus to access individual memory. Here, all the engine processors present in the system have an individual memory. When executing the method spatial and temporal parallelism improves throughput and data processing speed and is implemented in the use of one of the most important VLC system applications. Thus, the study [35-37] explained single computing engine has a basic experiment that shows how dose fixed performance for the VLC system single processor. Through the implementation of this method for novel dual computing engine in this research. According to the design behavior of the hardware and allows the restructuring of computing in an easier and less complex way. With consideration combining the less speed of implementation with the largest increase in throughput are the two most important elements to implement any custom design.

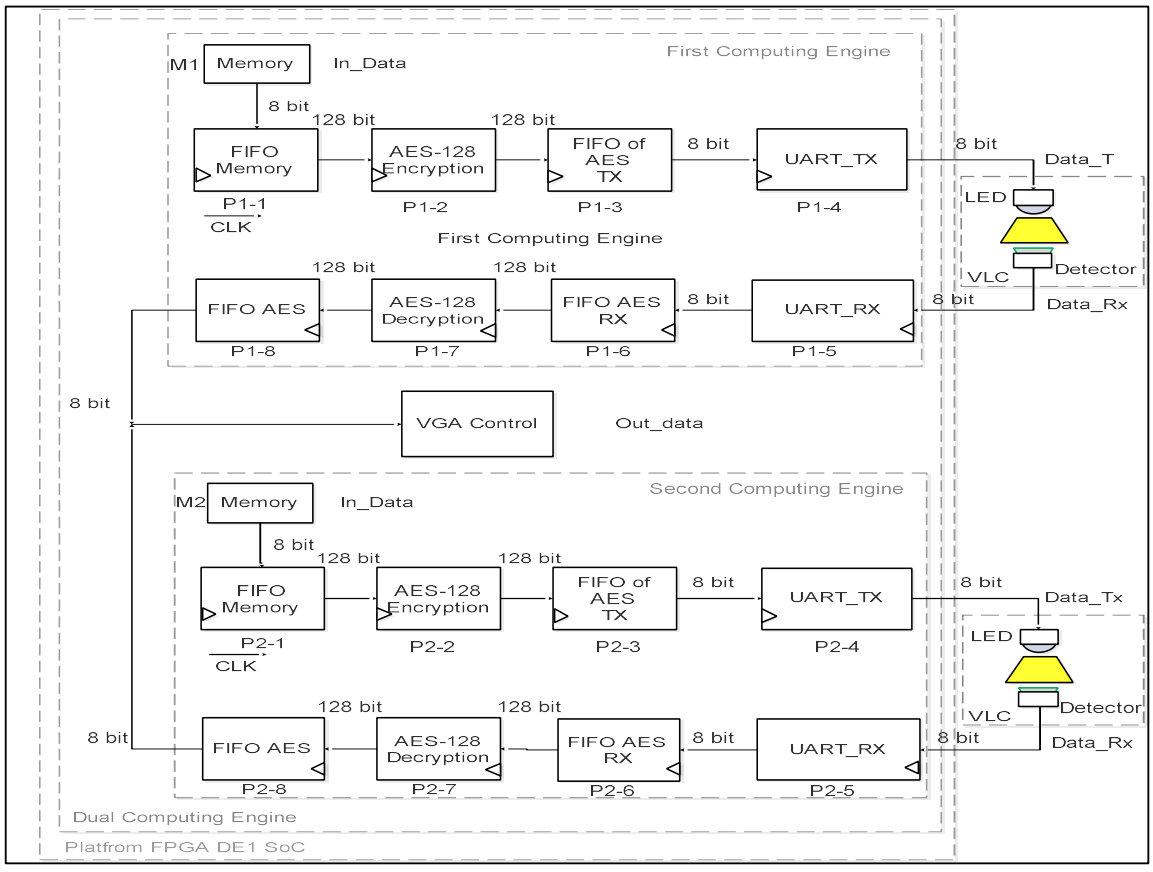


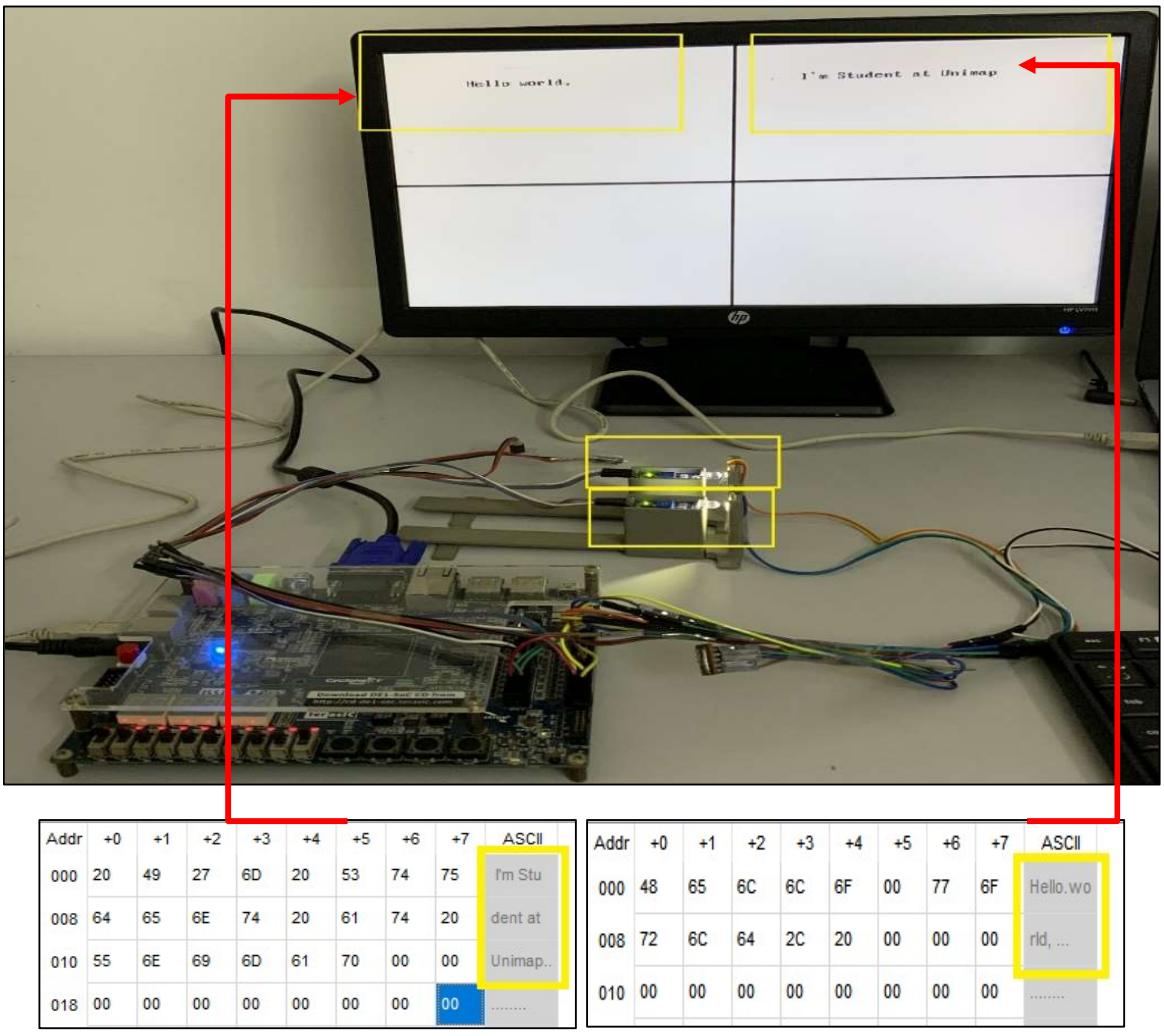
Fig. 6. Block diagram of Dual-Engine.

Each computing engine has a main URAT, 128-bit AES algorithm (encrypt and decrypt) transceiver via a VLC system. The bus memory is divided into two parts first M1 is based in FPGA architecture where the nine start from processors P1-1 to P1-9 for component computing engine using a single bus. Either, the second computing engine memory M2, when the processor from P2-1 to P2-9 of nine processors for data text. Following this strategy can allow us to have as many processors as needed for design.

5. RESULTS AND ANALYSIS

This paper presents the implementation of the key length of the 128-bit AES algorithm combined with UART in order to create a computing engine using the key length. The implementation of the 128-bit AES algorithm was carried out by Altera through the Cyclone V FPGA DE1-SoC. It was created, placed, and routed using Intel® Quartus® Prime Software 15.1 release which was used to synthesize, place, and route the VHDL core of this design, in which explicit directives were used to map loop unrolling through parallel processes for the 128-bit AES algorithm module for dual computing engines when mapping loop unrolling through parallel processes. In order to measure the number of slice registers, *Fmax*, throughput technique and Altera's tool was used. According to this functional novel design of dual computing engine of short text Sentence, the text that has been (“see Figure 7”), has divided text, into two groups. One of the saved first memory is (Hello world,) and the second memory saved another part of the data text (I'm student at unimap). The engine's ability to process data transfer through the VLC system. Then shown output to VGA after recovering, the behavior paves the way for increased security by dividing the data that can send through the light. On the other hand, implementing spatial parallelism to process the data dual computing engine of short text sent via VLC system. We found that realized VLC coding achieves better results in terms of speed/area, and the clock frequency can reach 173.34 MHz.

We found that process one input per cycle in actual operation, and the time processing rate is 5.76 μs. The proposed method in this study tended to have an inordinately higher proportion of throughput rate of 2.77 Gbps. without adversely impacting, the implementation, part of the calculation process is optimizing according to the characteristics of the FPGA. Recent observations suggest that the performance of our system. Our findings provide conclusive evidence that this is associated with several logic elements which used a dual computing engine was used more than 12,074 logic elements.



(A) (B)

Fig. 7. Dual computing engine of Short Text Sentence performance result (A) RAM Text_Dual_Enginle_Simple_1, and (B) RAM Text_Dual_Enginle_Simple_2.

The size word 8-bit of memory and number of word 256-bit, RAM Text_Dual_Enginle Simple_1 the input (*Hello world,*) saves at first memory the number of data has been used 12 words that value has sent via VLC system. RAM Text_Dual_Enginle Simple_2 the data save, second memory (*I'm Student at Unimap*) the number of data have used 21 words. In ("see Table 1"), the time of quest analysis of this novel design dual computing engine of short text sentence.

Table 1. Time of quest analysis dual computing engine of short text Sentence.

FPGA	Results
Frequency Maximum (*Fmax*)	173.34 MHz
Time	5.76 µs
Logic Element	12,074
Memory Bit	1,252,352
Throughput	2.772 Gbps

For completeness' sake, we have also contrasted the outcomes of our best method for analysing spatial and temporal parallelism behaviour with recently published cutting-edge findings. Since the majority of current work utilises the Altera Cyclone V DE1-SoC FPGA as the

target device, we developed our design on this FPGA for that reason. We evaluated the outcomes of our method and current research using a number of area and performance factors. Demonstrates how various approaches' throughputs may be compared. We also compare the frequencies of various implementation strategies since an implementation scheme's frequency might provide insight into the critical route delay of the implementation. Displays the frequency comparison of several approaches ("see Figure 8"). The approach provides the best frequency results among the available procedures, as can be observed. Finally, we make a throughput comparison between the current approaches and the suggested technique while utilising fewer FPGA resources. The 2770 Mbps DE1-SoC solution is 123.98% faster than the proposed 60 Mbps implementation [38]. Either the study [39] is slower than the 105.54 Mbps FPGA by 70.27% and another proposed [40] 10 Mbps is 11.27% slower.

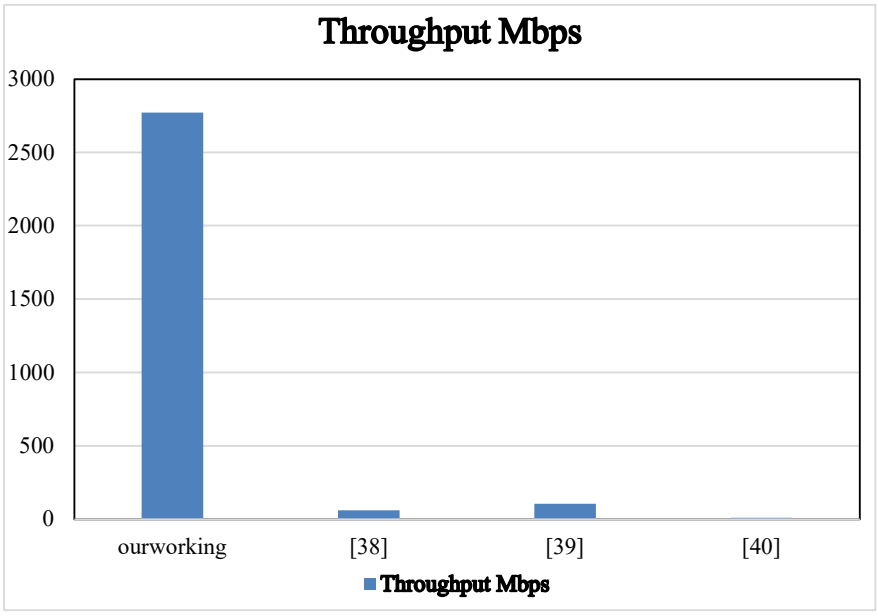


Fig. 8. Comparison of performance result studies.

6. Conclusions

Our findings provide conclusive evidence that this dual computing engine modern architecture in filed communication to control mange stream of data via VLC system. An effective architecture for dual computing engines has been given in this paper. This design uses the 128-bit AES algorithm and UART as implementation approaches to deliver secure text data transmission. This innovative method could provide a high enough degree of security for serial transmission through UART. Using an Altera Cyclone V SE 5CSEMA5F31C6N device, it only needs 12074 slices. A unique dual computing engine architecture that uses a VLC system and an FPGA board to transport brief text material has been introduced. We use hardware TX to RX communication using a one-way scenario tool.

Nevertheless, it demonstrates that our effort was effective since the LED didn't flicker and the received brief text could be extracted without being filtered by outside light impacts. The distance will then be too close, and only visible light communication will be possible. We have leveraged optimizations in this method, such as loop unrolling, to provide spatial parallelism to our architecture. Additionally, various FPGA resource mappings must provide various outcomes. Experimentation has shown that sequential implementations often provide high-performance outcomes. It was shown that effective use of the computational capabilities of FPGAs produces superior performance outcomes, and in one specific situation, a frequency as high as 173.34 MHz is attained. The most effective strategy, as determined by a comparison of various study methods, yields the highest results in terms of frequency and throughput 2.772 Gbps, ultimately producing the best area-delay trade-off. Due to the usage of the FPGA DE1-SoC in our system, a high-speed VLC system is made possible

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