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Zigbee Transceiver Under Fading Based on OQPSK

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Abstract

This work presents the design and modeling of a ZigBee transceiver system operating at a frequency of 2.4 GHz. In addition, the system employs offset quadrature phase shift keying (OQPSK) modulation to modify the pulses, employing a half-sine wave. This modifies the range of the broadcast signal to align with the channel's bandwidth. This study aims to address the issue of inter-symbol interference (ISI) and multipath disruption. The ZigBee wireless sensor network is designed to meet the requirements of IEEE 802.15.4 standards, focusing on facilitating short-range communications. This optimization aims to minimize costs, power consumption, and data rate. The aspects listed above provide significant challenges for technical progress aiming to achieve sufficient performance in real-time scenarios while effectively managing a cost-effective bit error rate (BER). By utilizing DSSS as a dissemination technique, the proposed system reduces the impact of noise while simultaneously increasing the signal frequency and energy. The input signal is converted to binary, enabling a maximum data rate of 250 kbps. The evaluation of the ratio between the Bit Error Rate (BER) and Signal-to-Noise Ratio (SNR) for three distinct wireless channel models, specifically Rician, AWGN, and Rayleigh, while considering the presence of multipath received signals, offers significant insights on the system's performance during transmission modes. The statistic known as the bit error rate (BER) holds significant importance in the assessment of data security inside a digital communication system.. According to the findings, AWGN has the lowest BER, whereas Rayleigh and Rician have the highest. A modest output delay of 0.4 μs is associated with Rician, and its BER is reduced compared to AWGN and Rayleigh.

Keywords: Transceiver, OQPSK modulation, AWGN channel, Multipath Rayleigh Fading Channel, Recian Chanel, Bit error rate.

1. **Introduction**

The attention has mostly been on merging progress in wireless communications and electronics with establishing networks that include low-cost, energy-efficient, and versatile sensors. Although compact, these sensors can collect, interpret, and transmit data via RF channels. [1].
ZigBee technology has gained traction in many sectors and has found applications in several wireless personal area networked systems. It may be found in many places, including home automation, intelligent energy, healthcare, telecom applications, industrial process monitoring and control, and commercial building automation. [2,3].
The ZigBee Alliance oversees the ZigBee protocol, while IEEE controls IEEE 802.15.4. Using the IEEE 802.11b network standard as its foundation, it resembles TCP/IP. The ZigBee

Alliance software defines the application, security, and network layers. According to IEEE802.15.4 (hardware) [4], the physical and media access control layers are described. With its increased dependability and expanded range, ZigBee wireless mesh networking finds several uses in wireless control and monitoring. Lastly, smaller batteries with longer life spans are possible because of reduced power usage. ZigBee technology may function in three separate frequency bands, determined by the geographical coverage. Unlicensed Industrial, Scientific, and Medical (ISM) radio channels create the global standard of 2.4 GHz. The frequency band of 902-928 MHz (915 MHz) is utilized in Europe and Northern America. The bit rates exhibit a broad spectrum, spanning from 20 kilobits per second at 868 megahertz to 250 kilobits per second at 2.4 gigahertz [5, 6, 7].

Offset Quadrature Phase Shift Keying (OQPSK) or Staggered QPSK (SQPSK) is a modified variant of QPSK used for modulation. This change effectively mitigates signal phase shifts by introducing a delay of half a cycle, resulting in a significant advantage. The signal may be sent using four separate orthogonal phases facilitated by the carrier. [8, 9, 10].

Many things impact the wireless medium in real time, including interference, path loss, and Doppler shift. These factors influence wireless communication's data rate, range, and dependability [11]. Obtaining a transceiver device capable of functioning in such environments is crucial. One of the most formidable challenges in constructing a digital transceiver system is attaining sufficient performance in real-time circumstances. The quantification of the ratio of lost bits during transmission to the total amount of bits delivered is a critical metric for these systems, known as the bit error rate (BER).. Therefore, it is imperative to assess the efficacy of the digital system in addressing these difficulties.

In this study, the Zigbee transceiver model is designed and simulated utilizing the IEEE 802.15.4 standard and specifications, with a specific emphasis on the 2.4 GHz frequency bandTwo crucial criteria of this standard are the OQPSK modulation technique, which utilizes a half-sine wave for pulse shaping, and the DSSS for spreading. These standards assess system performance in AWGN fading channels with respect to bit error rate (BER).

Accordingly, the researcher plans to examine the necessary criteria for constructing Zigbee transceiver systems, including the modulation mechanism and the external noise. While other researchers have suggested transceiver systems, R. Kanna (2011)[12] devoted his attention to creating a Zigbee transceiver. The only difference between the input and output bit streams was a little delay of 1.5 microseconds. In 2014[13], P. K. Agarwal developed a Zigbee wireless communication system transceiver. Theoretically, MSK may achieve a bandwidth efficiency of 2 bits/s/Hz in Mat-lab Simulink, according to an analysis of the presented model. In 2015[11], K. Gorantla and V. V. Mani used the DSSS approach to analyze a Zigbee transceiver while it traversed an AWGN channel. After 6 dB, the BER performs poorly as EblNo grows. Without using any mathematically challenging blocks, X. Wang was able to construct and test a Zigbee wireless transceiver in 20 [14]. In theory, MSK can only use two bits/s/Hz of bandwidth efficiently. A little delay of 1.5µsec is the only exception. A Zigbee transceiver was successfully constructed using Simulink by V. A. Mardiana and T. Adiono in 2017 [15]. The received signal had a small degree of latency equivalent to 1.5 µsec. From an Eb/No range of 1dB to 8dB, the performance analysis revealed promising outcomes. In 2018, E. Kadhum and R. Haitham[1] discussed using OQPSK modulation in a Zigbee transceiver system and how it was tested for BER in the presence of AWGN.

2. **Proposed System design**

One of the most complex parts of building a digital transceiver system is getting it to work well in real time. Given the significance of the BER measure, it must be used to assess the digital system's efficacy in such situations. As shown in Table 1, the following criteria are considered while simulating a Zigbee transceiver: a 2.4 GHz system that adheres to IEEE 802.15 standards; the system's performance is assessed using BER in an AWGN channel.
The transmitter's essential features include modulation, baseband waveform shaping, serial-to-parallel conversion, symbol-to-chip and bit-to-symbol mapping, and more. The receiver section also shows the steps for de-spreading, converting a parallel signal to a serial one, and converting an RF signal to a baseband signal. Figures 1 and 2 show the primary characteristics of the suggested channel, receiver, and transmitter models.

The IEEE 802.15.4 Standard for a ZigBee Transceiver Operating at 2.4 GHz [16]

Configuration settings	Values
Data transfer speed	250kbps
Frequency of operation	2.4GHZ
amount of channel	16
Spacing between channels	5MHZ
Chip rate	2Mbps
Pulse shaping	Half sine
Spreading technique	DSSS
Method of modulation	OQPSK

2.1 ZigBee Transmitter Design Model

Figure 1 depicts how a radio transmitter with a complicated modulation scheme and appropriate pulse shaping may be developed precisely, cost-effectively, and efficiently using essential components.

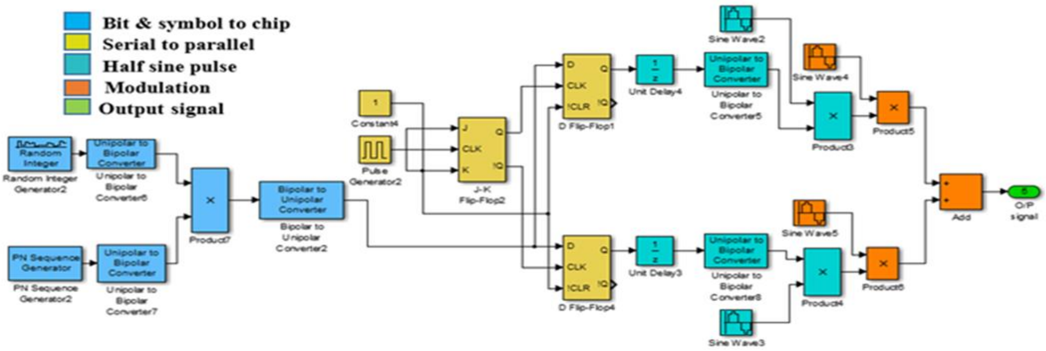

Figure 1 shows the fundamental structural design of the proposed transmitter and channel.

To set up a ZigBee transmitter, follow these steps.

• Firstly, it is necessary to prepare the input bit stream. In this stage, it is imperative to carry out the bit-to-symbol and symbol-to-chip mapping procedures. Initially, verify that the input data stream is capable of meeting the data rate and chip rate requirements specified by IEEE 802.15.4. The input stream is generated by a single random number. It has a data transmission rate of 250 kilobits per second. Upon converting the input data of 250 kbps into a symbol, the symbol rate is then decreased to 62.5 kbpsA PN sequence generator is utilized to generate the Pseudo Noise code.. Figure 1 displays a direct sequence spread spectrum (DSSS) with a data rate of 2Mbps and a chip sequence incorporating pseudo-random noise (PN). In order to optimize transmitter efficiency within a multipath environment, the objective of this strategy is to increase the frequency of the input data stream to 2 Mbps. [17, 18].

• • The next stage involves converting the data from serial to parallel. The encoded data is divided into two distinct portions, namely in-phase and quadrature, prior to the process of modulation. Figure 1 depicts the procedure for generating clock pulses that are both even and odd by employing a JK-flip flop in a toggling condition. In-phase data is generated by the positive output (Q), whereas quadrate data is created by the negative output (N). The aforementioned process is iterated for every clock pulse, as depicted in Figure 1 [12]. After the conversion from serial to parallel, the data rate of both the In-phase and Quadrature data is 1Mbps. The bandwidth efficiency is enhanced as it allows for the simultaneous transmission of two bits.

• Thirdly, shape the half-sine pulse and perform the modulation process. Notwithstanding this, below is the equation for the OQPSK modulation signal: [1]:

$$S(t) = \frac{A}{\sqrt{2}}\left[I(t)\cos\ 2\pi f_c t - Q(t - \tfrac{\pi}{2})\sin\ 2\pi f_c t\right] - \infty < t < \infty \qquad (1)$$

Given that previous research has mainly concentrated on the second channel, it is possible to modify the equation to postpone the first channel of OQPSK without diminishing the system's effectiveness. The OQPSK modulation signal equation may be reformulated in the following manner:

$$S(t) = \frac{A}{\sqrt{2}}\left[I\left(t - \frac{\pi}{2}\right)\cos 2\pi f_c t - Q(t)\sin 2\pi f_c t\right] \ - \infty < t < \infty \qquad (2)$$

Although the power density and error output of both techniques are identical, the act of delaying the I-phase channel by T/2 seconds serves as a preventive measure against interference in OQPSK modulation. The reason for this is because OQPSK leads to a maximum phase conversion of /2, while QPSK induces a phase displacement of . The process of pulse shaping involves the multiplication of a half-sine wave with the output of In-phase and Quadrature data. Pulse shaping, a pre-modulating filter, is used to adjust the transmitted signal spectrum to match the channel bandwidth in order to prevent multipath and ISI effects. Prior to transmission over the channel, the aforementioned signals undergo amplification with a 2.4 GHz carrier frequency, followed by the application of In-Phase and Q-signals [19] [7].

2.2 ZigBee Receiver Design Model

Zigbee receiver implementation is step-by-step, as seen in Figure 2 below.

• Initially, the signals are demodulated through the process of multiplying the in-phase data at the receiver side with a cosine carrier signal operating at 2.4GHz, and the quadrature data with a sine carrier signal operating at 2.4GHz. The term used to describe this process is RF to baseband conversion. Subsequently, we produce modulated signals in both the I-channel and

Q-channel. The output signals on the transmitter side are pulse-shaped through the utilization of half-sine pulse-shaping signals. [15].

- The second step involves the conversion of analog signals to digital signals, followed by a decision-making process. This process entails passing the outputs of two distinct signal types, namely in-phase and quadrature, through an analog low pass filter. The purpose of this filter is to separate the baseband signal from the high-frequency harmonics. The implementation of a circuit that selectively permits the transmission of low frequencies while impeding the propagation of high frequencies enables the utilization of a cutoff frequency of 500 kHz for the purpose of noise reduction. Verify the binary representation of the data value by employing a comparator and a zero-order hold circuit.
- In this step, the process of de-spreading and parallel-to-serial conversion is employed. Specifically, a parallel-to-serial converter is utilized to combine the in-phase and quadrature data, which are essential for generating serial data [20]. The serial data obtained from the transmitter is de-accelerated by employing the designated chip rate and PN sequence. In order to maintain synchronization with the transmitter sequence, a delay transport factor and rate transition are incorporated subsequent to the PN sequence. [14,21].

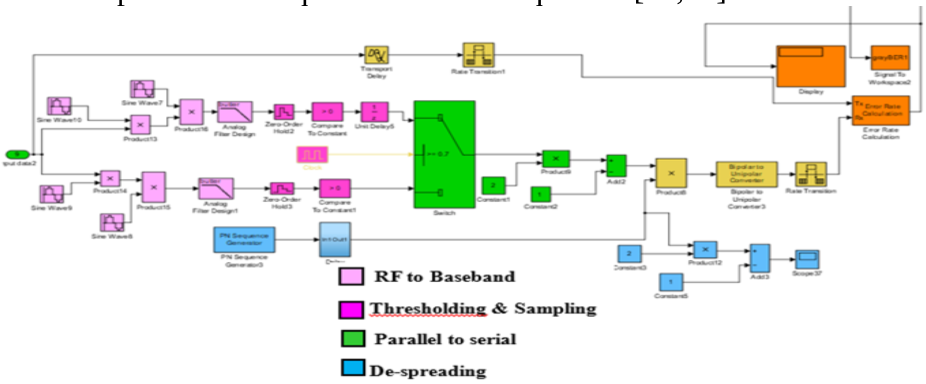

Figure 2 shows the proposed receiver and channel design basic structure Model**.**

3**. Result and Discussion**

In order to showcase the feasibility of constructing radio transmitter and reception systems utilizing advanced modulation techniques and appropriate pulse shaping methods in a dependable and cost-efficient manner, the transmitter and receiver models were constructed in MATLAB/Simulink, incorporating crucial components. Figure 3 illustrates the signal waveforms of the input sequence, PN sequence generator, and DSSS spectrum.

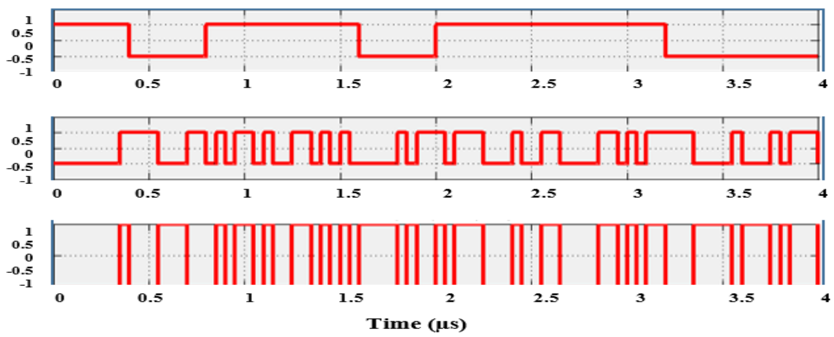

Figure 3 Input, PN sequence, and DS spectrum.

A half-sine wave, created by multiplying a half-sine wave of 0.5 MHZ with a half-sine wave of 0.5 MHZ, is applied to the NRZ-formatted output data of the in-phase and quadrature channels. Figure 4 displays the output of each channel as a consequence of generating half-sine pulses.

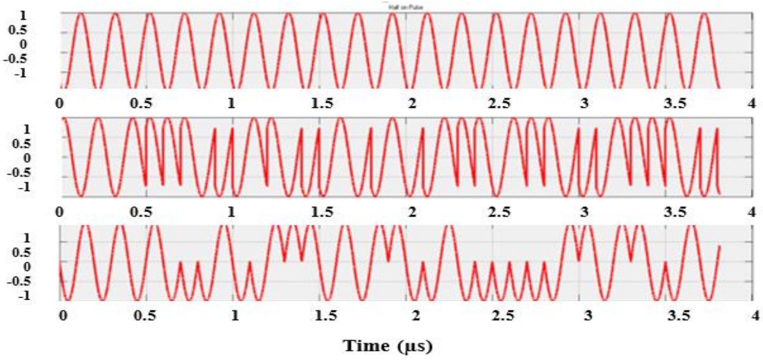

Figure 4 in-phase and quadrature patterns observed during a half-sinusoidal pulse.

The modulation process was performed by multiplying the In-phase data by a carrier frequency of a 2.4 GHz sine wave. The Quadrature data underwent multiplication using a 2.4 GHz cosine wave. Figure 5 illustrates the direct combination of the I-channel and Q-channel data to form the final modulated signal.

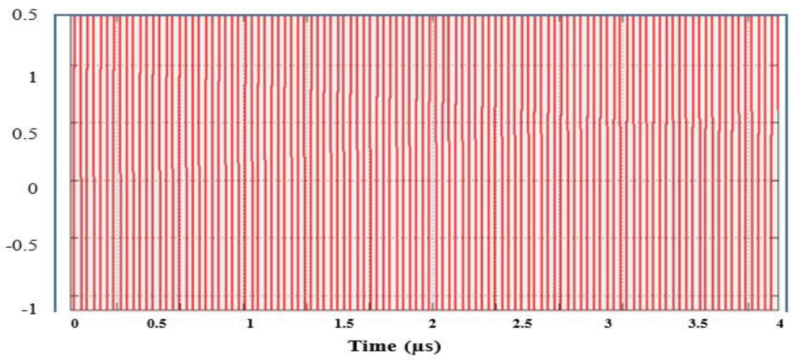

Figure 5 status of the signal on the Transmitter side.

The receiver performed a demodulation operation at 2.4 GHz to transform the received RF signal into a baseband waveform. The In-phase data was multiplied by a sine wave carrier signal, whereas the Quadrature data was multiplied by a cosine wave carrier signal. Figure 6 depicts the data subsequent to the process of demodulation.

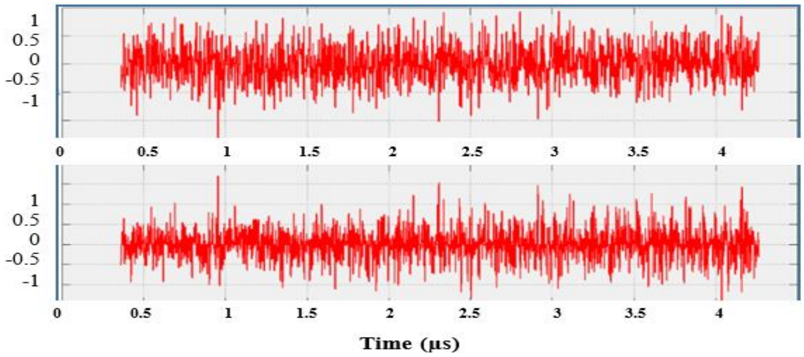

Figure 6 Data after demodulation.

To achieve half-sine pulse shaping on the transmitting end, a half-sine wave with a frequency of 1MHz is used to multiply the demodulated data. A third-order analog Butterworth low-pass filter was utilized to restore the original data, operating at a frequency of 500 MHz. A circuit including a comparator and a zero-order hold was employed to implement the ADC converter for sampling and thresholding. To streamline the dissemination of the ultimate digital signal, the In-phase and Quadrature data were initially merged using a switch operating at a clock frequency of 2 MHz and the process of converting from parallel to serial, as seen in Figure 7.

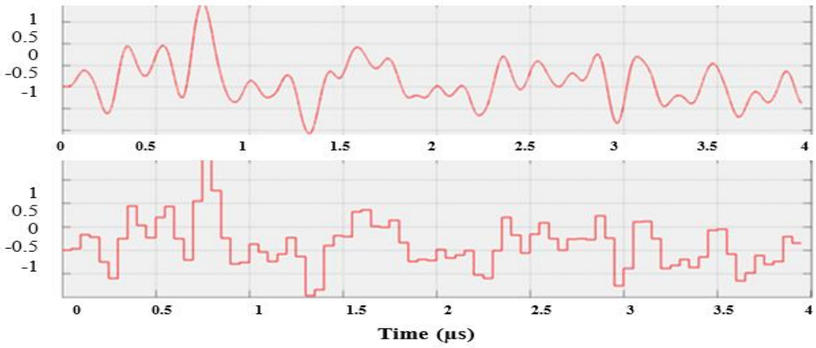

Figure 7 Filter with a low pass and ADC converter.

The de-spreading process is concluded by multiplying the final serial signal by the chip rate of the PN sequence generator which is 2Mbps. A delay transport factor of 0.4 µs was implemented in the transmitter following the PN sequence at the receiver end to generate an identical signal to accomplish synchronization. In addition, as illustrated in Figure 8, the data was effectively retrieved.

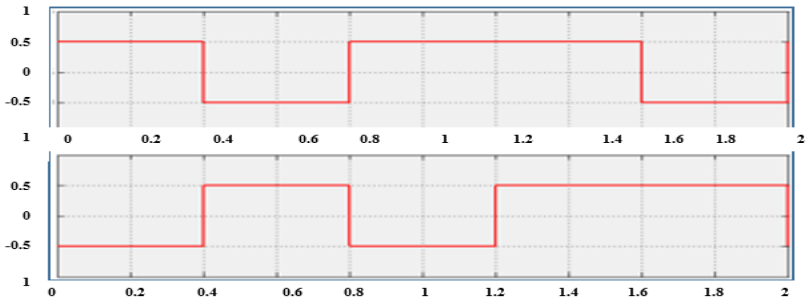

Figure 8 The output data from the received signal.

BER decreases in direct proportion to any increase in SNR. Hence, to assess the performance of the proposed system, the BER versus Eb/No ratio is computed while the AWGN channel is in a multipath Rayleigh and reciprocal state. Furthermore, MATLAB's BER Analysis Tool (BERTool) computes the BER to the Eb/No or signal-to-noise ratio (SNR). MATLAB functions and Simulink models are subjected to Monte Carlo and theoretical simulations to evaluate their performance. BER values were calculated for AWGN using Eb/No values ranging from -8 dB to 10 dB, and for multipath Rayleigh and reciprocal fading channels using Eb/No values ranging from -8 dB to 15 dB. Figures 9, 10, and 11 illustrate the bit error rate (BER) curves for the system, respectively.

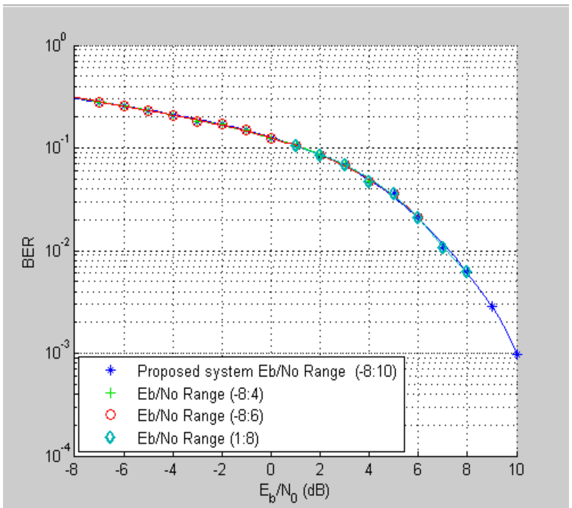

Figure9 BER curve with an AW GN channel.

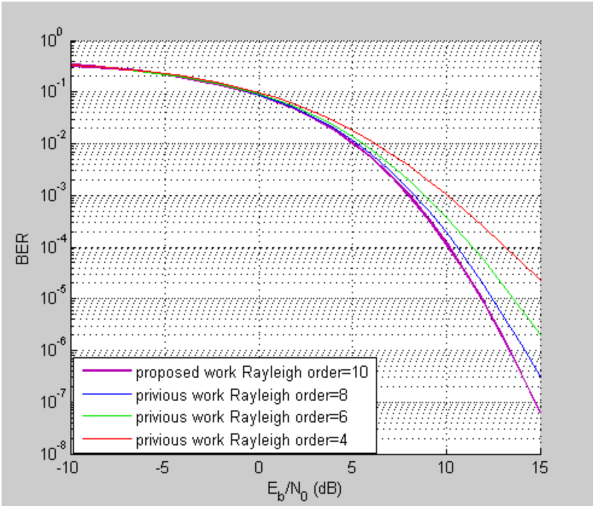

Figure 10 BER curve with a Rayleigh fading channel.

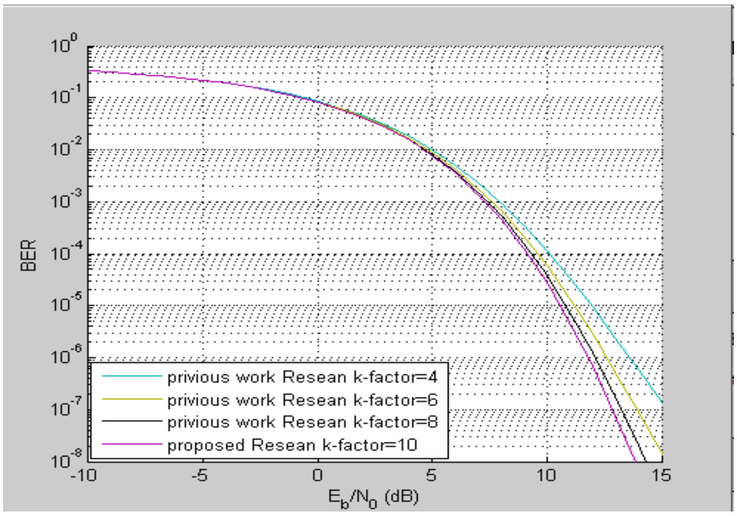

Figure 11 BER curve with a Recian fading channel.

An additional advantage of utilizing the DSSS method is the further reduction of interference effects. Moreover, a direct conversion method into the receiver design successfully achieved cost reduction and power efficiency objectives. Furthermore, the results show that the system performance achieves the desired BER that is equal to 0.001 when Eb/No = 10 dB in AWGN channel, 2.99 micro when (order = 10, Eb/No= 15 dB) in Rayleigh channel, 0.530 nano when (K-factor= 10, Eb/No = 15 dB) in Recian channel as an example, in comparison to that given by [1, 11, 15,7].

4. **Conclusion**

Utilizing MATLAB/Simulink, the 2.4 GHz Zigbee Transceiver is designed and simulated by IEEE 802.15.4 standards. Based on the simulation outcomes, it can be concluded that the input and output signals are indistinguishable, with the output latency increasing by no more than 0.4 seconds when compared to the signal period at 250 kb/sec.

The direct sequence spread spectrum approach effectively mitigates additional interference effects. In real-time operations, the utilization of half-sine pulse shaping is an efficient technique for mitigating abrupt phase changes and various obstacles in the transmitted signal. These aforementioned benefits may serve as the foundation for future endeavors aimed at establishing a connection between MATLAB/Simulink and System-on-Chip (SoC) using Field Programmable Gate Arrays (FPGA Kits) or Verilog HDL, as well as validating the code that has been tested.

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