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90 nm Current Mirror Based Transimpedance Amplifiers for Fiber Optic Applications

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ABSTRACT

This research displayed the new design of a 90 nm CMOS technology transimpedance amplifier (TIA) with current mirror executed. The goal and challenge in this research are to arrive at low consumption of power while activating other required performances. Integrated circuits CMOS(Complimentary Metal-Oxide Semiconductor) tend to be the best technology achieving the desired level of integration with appropriate speed, cost, and gain for this were used. The proposed transimpedance amplifier (TIA) consists of a common-gate (CG) topology with a current mirror to increase TIA gain and common-source (CS) TIA with the active feedback resistor. In addition, to verify the proposed TIA performance, circuit simulations are done in NI Multisim 14.1 using 90nm CMOS technology parameters. Therefore, the simulation results of the proposed TIA for 90 nm CMOS technology indicate a transimpedance gain of 66.63 dBΩ with -3dB frequency bandwidth of around 1.0 GHz for input capacitance of 250 fF, input-referred noise of 25.413 pA/√Hzand with the power consumption of only 1.08mW at 1V supply voltage. This low power consumption and supply voltage are the main emphases of this work in comparison with other research literature.

Keywords: Common-gate (CG) amplifier; Common-source (CS) amplifier; Active feedback.

INTRODUCTION

Transimpedance amplifier (TIA) circuits in optical fiber networks play an important role in the optical fiber networks (Ota and Swartz, 1990). Besides long-haul fiber optic networks, optical communications are rapidly expanding into shorter distance, lower cost applications (Phang and Johns, 2001). The TIA must meet rigid specifications such as low input impedance to relatively high photodiode efficiency and thus achieve wide bandwidth, low noise to optimize receiver sensitivity, low cost area and low power consumption (Hassan and Zimmermann, 2012).

Besides, the scaling of the CMOS (Complementary Metal-Oxide Semiconductor) procedure to the range of nanometers enables the design of low-cost and high speedanalog CMOS circuit. However, the stacking of circuits is limited by the supply voltage scaling in nanometer CMOS technologies. It, therefore, limits gain and speed overall (Muller and Leblebici,2007). CMOS technology process combines devices formed by n-channel and p-channel in such a way to reduce the standby current by orders of magnitude relative to pure NMOS and PMOS implementations. No direct current can pass from V_{DD} to ground as a CMOS appreciable current can rise during switching transients, and hence, a current exists only during small fraction of time during device operation (Pimbley *et al.*,1989).

Current Mirror

This paper presents an optical receiver based on an NMOS current mirror. This current mirror input was used to execute feedback current amplifiers which are capable of sensing the input current with low input resistance and amplifying it at a high impedance node, at the output (Hassan and Zimmermann., 2012). In Fig. (1), we note that the drain-gate voltage of the ambient M_1 is zero; therefore, the channel does not exist at the drain, and we see that the two transistors M_1 and M_2 operates in the saturation region if the threshold is positive. The current that flows in the drain of M_1 is mirrored to the drain of M_2 (Gray, 2001).

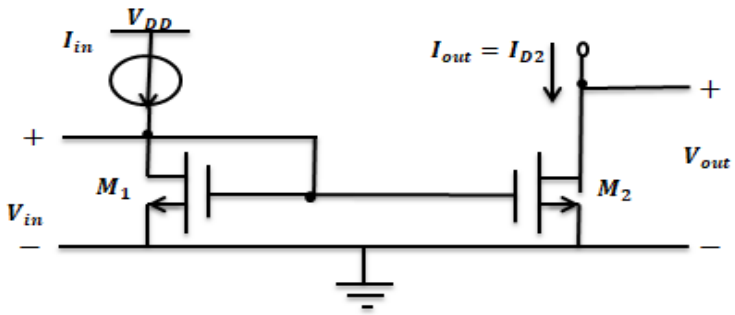

Fig. 1: A simple MOS current mirror

Common-Gate Amplifier

The common-gate (CG) amplifier is shown in Fig. (2a), the common-gate senses the input at the source and generates the output at the drain. The gate is connected to the DC voltage to establish proper operating conditions.

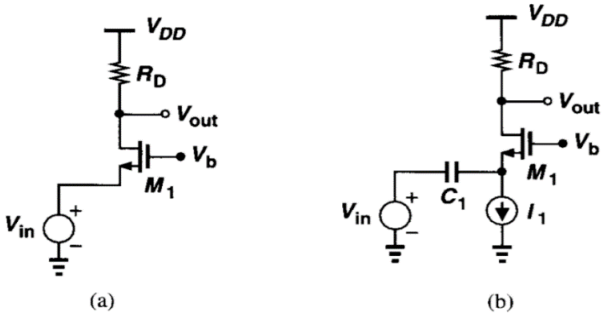

Fig. 2:(a) (CG)with direct coupling at input.(b) (CG)stage with capacitive coupling at input

We see that M_1 bias current flows through the source of the input signal. In illustrated figure (2b), M_1can be biased by a constant current source, with the signal being capacitively connected to the circuit (Razavi, 2001). If the input increases by a small value, ΔV, the gate-source voltage of M_1 decreases by the same number, thus decreasing the drain current by $g_m \Delta V$ and increasing V by $g_m \Delta V R_D$.Then the voltage gain is positive and equal to:

$$A_\upsilon = g_m R_D \qquad (1)$$

If I_D or R_D is high enough, we can get a high gain, but the drain voltage, $V_{DD} - I_D R_D$, still has to be above $V_b - V_{TH}$ to make sure M_1 is saturated (Razavi, 2014).

The Design of Proposed (TIA) Circuit

In this section, we will present the design of the transimpedance amplifier (TIA) structure with current mirror implemented in a low-voltage (1V) and 90 nm CMOS technology as shown in Fig. (3). The proposed TIA topology involves a common-gate (CG) TIA and common-source (CS) TIA, with active feedback resistor and the current mirror to increase the gain in transimpedance. This work is a development of previous research (Phang, 2001). In this work, NI Multisim 14.1 Software was used to simulate the proposed transimpedance amplifier. It is based upon PSpice circuit solver engine which enable circuits to be solved on mathematical conversion point.

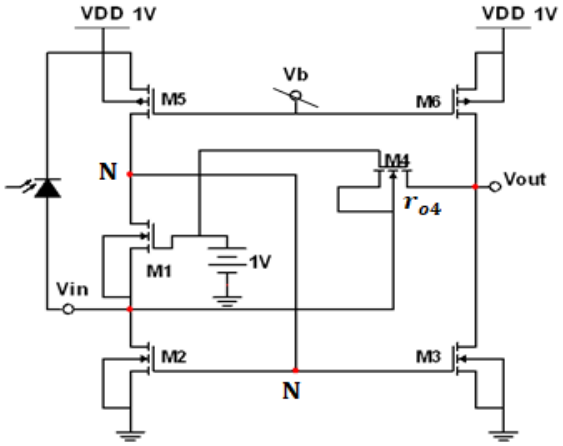

Fig. 3: Proposed low-voltage optical preamplifier

When the light is incident on the photodiode, it will convert the light into a suitable current. The input capacitance (250 fF) built in was attached parallel to the photodiode. The input capacitance is inversely proportional to the bandwidth frequency as the input capacitance increases, the bandwidth frequency decreases and this is due to the photodiode limitations that affect input capacitance.

Additionally, the circuit output is connected to another capacitance (250 fF output load capacitance) built in. The current from the photodiode would then move through the M_1NMOS transistor representing the common-gate (CG) amplifier operating in the saturation region.

Therefore, the signal exiting in the drain terminal for M_1 passes through the node Nwhich in turn passes the signal through the gates of each of the M_2 and M_3 NMOS transistors representing

the common source (CS) amplifier. As a result, the current in the M_3 transistor will be similar to the current in the M_2 transistor, then this current is called "current mirror" as previously stated and used to bias the NMOS transistor. After the signal is released from the M_3 transistor drain terminal, the current passes through the M_4 NMOS transistor (act as a resistor), representing a common-gate amplifier. Then M_4 transistor becomes a part of the feedback stage (negative feedback) by which the voltage at the output is converted into a current back to input, which is unprecedented here and for the first time, in addition, an active feedback loop connected to the input node was used, which ensures that there is no real resistance but built in NMOS channel resistance. Then, the amplification stage of the signal will be completed. Fig. (3) also shows that there are two PMOS transistorsM_5 and M_6 which function as "current sources" as used to maintain the current stability in the circuit.

Now, after reviewing the circuit operation we will look at the internal variables for each type of NMOS and PMOS transistor as shown in (Table 1).

Table 1: Parameters of NMOS and PMOS transistors

Model Parameter	Description	n-channel	p-channel	Units
L	Length	0.09	0.09	µm
W	Width	0.27	0.18	µm
V_{TH}	Threshold voltage	0.1	-0.8	V
K_P	Transconductance parameter	1.73	1.78	mA/V^2
LAMBDA	Channel length modulation	0.027	0.022	1/V
R_D	Drain ohmic resistance	2	1	Ω
R_S	Source ohmic resistor	2	1	Ω
CBD	Zero-bias Bulk Drain capacitance (CBD)	1e-14	1e-14	F
CBS	Zero-bias Bulk Source capacitance (CBS)	1e-14	1e-14	F
CGSO	Gate-Source overlap capacitance (C_{GSO})	1.5e-7	6.066e-9	F/m
CGDO	Gate-Drain overlap capacitance (C_{GDO})	6.2e-9	6.066e-9	F/m
CGBO	Gate-Bulk overlap capacitance (C_{GBO})	1e-9	1	F/m
T_{OX}	Oxide thickness (T_{OX})	2e-8	9.7e-9	m
U_0	Surface mobility	100	50	cm^2/V^2

After entering and simulating these variables for the NMOS and PMOS transistors, we obtained the best results as shown in the low voltage (1V) supply (Table 2) concluding: high gain, wide bandwidth, low power consumption, and low noise at high frequencies.

Table 2: Simulated results

Technology	90nm CMOS (V_{TH}: 0.1V NMOS and 0.8V PMOS)
Input Capacitance	250 fF
Supply Voltage	1V
Gain	66.63 dBΩ
Bandwidth	1.0GHz
Power Consumption	1.08 mW
Input-Referred Noise	25.413/√Hz

Analysis of the Proposed Design

For circuit analysis, we will use the optical preamplifier small signal circuit as an illustration in Fig. (4). First of all, there are some simplifications were made: The main parasitic have been collected together into admittances Y_{in}, Y_N, Y_L and Y_f as follows:

$$Y_{in} = sC_{in} = s(C_{PD} + C_{gs1} + C_{db2}) \quad (2)$$

$$Y_N = sC_N = s(C_{gs2} + C_{gs3} + C_{db1} + C_{dbp5}) \quad (3)$$

$$Y_L = sC_L = s(C_{out} + C_{dbp6} + C_{db3}) \quad (4)$$

$$Y_f = {}^{1}/_{r_{o4}} + sC_f \quad (5)$$

Where C_{PD} is the photodiode capacitance, C_{out} is the capacitance of output load, while C_{gs} and C_{db} are gate-to-source and drain-to-bulk parasitic capacitances respectively within the circuit.

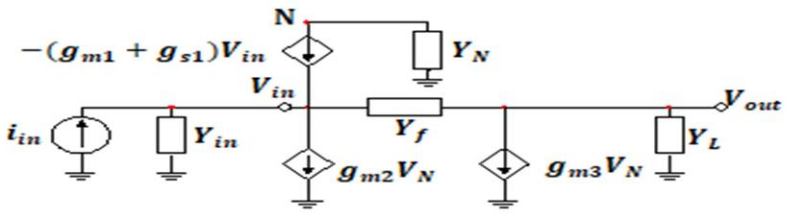

Fig. 4: Small-signal circuit of the transimpedance amplifier

Now, we can draw the TIA Signal Flow Graph (SFG) as shown in Fig. (5) for proposed schematic circuit design. This figure shows how the SFG circuit structure reflects that of the circuit. We may redraw the SFG as shown in Fig. (6) to explain the loops in a feedback form. We note that the TIA consists of the following feedback loops: L_1, is the loop (transconductance feedback) for the common gate topology of transistor M_1, while, L_2, is a loop (feedback) that passes from the input node to the gate of M_2 conducting to M_1. As for loop, L_3, it is around transistor M_3 through resistor r_{o4}.

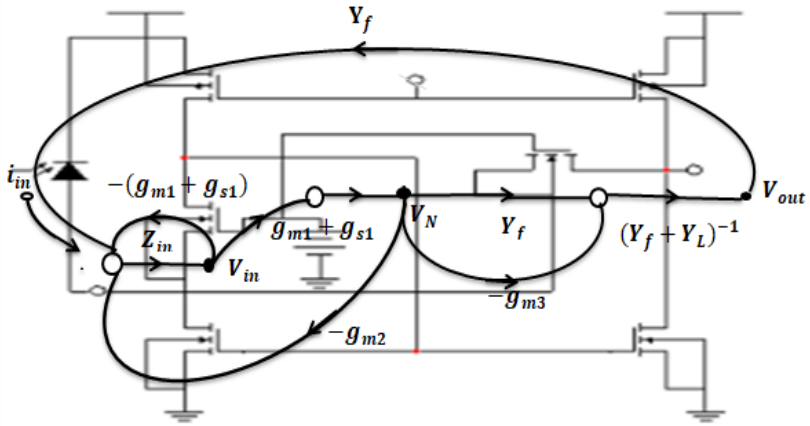

Fig. 5: Simplified SFG for the signal path

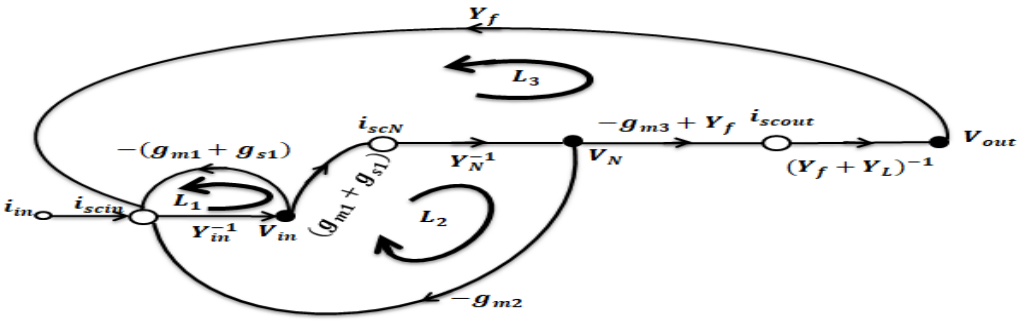

Fig. 6: Feedback loops within SFG clarifying signal path within the TIA

Now, we can derive the circuit's transimpedance gain from Fig. (6) by using Mason's Direct Rule:

$$\frac{v_{out}}{i_{in}} = \frac{p_1\Delta_1}{\Delta} \qquad (6)$$

Where p_1 is the forward Transimpedance path from i_{in} to v_{out},

$$p_1 = \frac{(g_{m1}+g_{s1})(-g_{m3}+Y_f)}{Y_{in}Y_N(Y_f+Y_L)} \qquad (7)$$

While $\Delta_1 = 1$, and Δ is equal:

$$\Delta = 1-(L_1+L_2+L_3) \qquad (8)$$

By combining for the admittances equations Y_{in} , Y_N ,Y_L , and Y_f , it is possible to obtain the following formula for the (ACgain) transimpedance gain:

$$\frac{v_{out}}{i_{in}}(s) = \frac{-g_{m3}+g_{ds4}+sC_f}{a_3s^3+a_2s^2+a_1s+a_0} \qquad (9)$$

And the coefficients of the denominator are given by:

$$a_3 = \frac{C_{in}C_N}{(g_{m1}+g_{s1})}[C_f+C_L]$$

$$a_2 = \frac{C_{in}C_Ng_{ds4}-C_f^2}{(g_{m1}+g_{s1})}+C_N[C_f+C_L]$$

$$a_1 = C_Ng_{ds4}+g_{m2}[C_f+C_L]+\frac{C_f}{(g_{m1}+g_{s1})}[g_{m3}-2g_{ds4}]$$

$$a_0 = g_{ds4}\left[g_{m2}+\frac{(g_{m3}-g_{ds4})}{(g_{m1}+g_{s1})}\right]$$

Where g_{ds4} is the transconductance between the drain to source for M_4 transistor and equals:

$$g_{ds4} = \frac{1}{r_{o4}} \qquad (10)$$

Note that at (DC gain), the transimpedance gain becomes:

$$\frac{V_{out}}{i_{in}}(0) = -\frac{g_{m3}+g_{ds4}}{a_0} \qquad (11)$$

Bandwidth Modeling

As we know, bandwidth and sensitivity are the critical performance characteristics of any optical preamplifier. The bandwidth is worked out through the circuit frequency response. We'll improvise a simple model of the input impedance of the proposed TIA in the process. We can estimate the proposed TIA bandwidth. To find this approximation, the simplification of the SFG circuit and the identification of the dominant terms in each branch are included. From Fig. (7), we note that the first initiation of simplification, and the feedback loop locally around v_{in} and i_{scin}

were eventually reduced. We notice according to equation (9) that the transimpedance gain is proportional to $(-g_{m3} + g_{ds4})$, and so g_{m3} is not too smaller than Y_f, therefore we cannot neglect Y_f; but C_f only at high frequencies is typically very small and can be neglected at this stage, so we can make the approximation that:

$$-g_{m3} + Y_f = -g_{m3} + {}^{1}/_{r_{o4}} + sC_f = -g_{m3} + {}^{1}/_{r_{o4}}$$

From i_{scout} to i_{scin}, branches are combined at:

$$(Y_f + Y_L)^{-1} \times Y_f \approx \frac{1}{(Y_f + Y_L)} \times Y_f = \frac{1}{1 + sr_{o4}C_L}$$

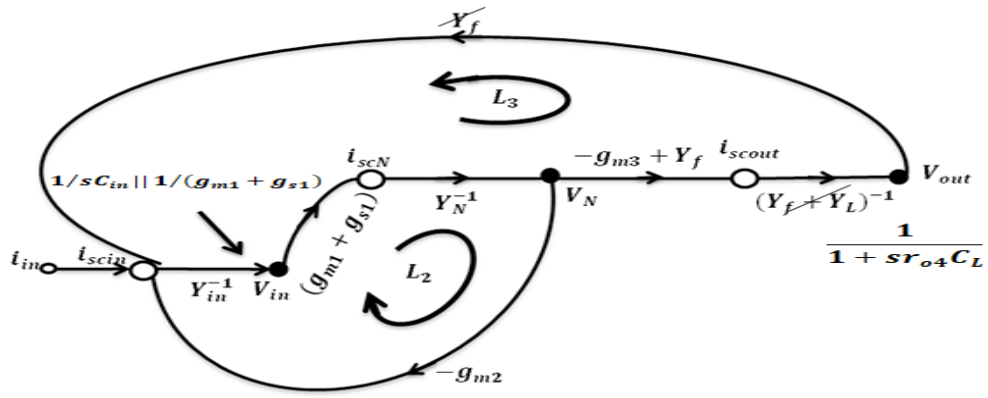

Fig. 7: Simplified SFG for the signal path

As such, we can minimize the entire SFG, as shown in Fig. (7), which can be schematically depicted in Fig. (8) when collapsed.

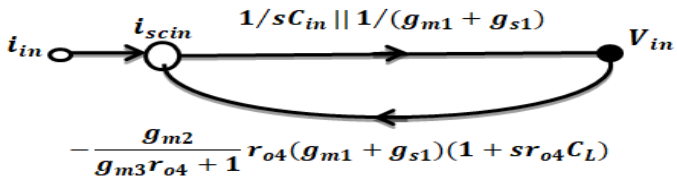

Fig. 8: Simplified SFG from previous figure

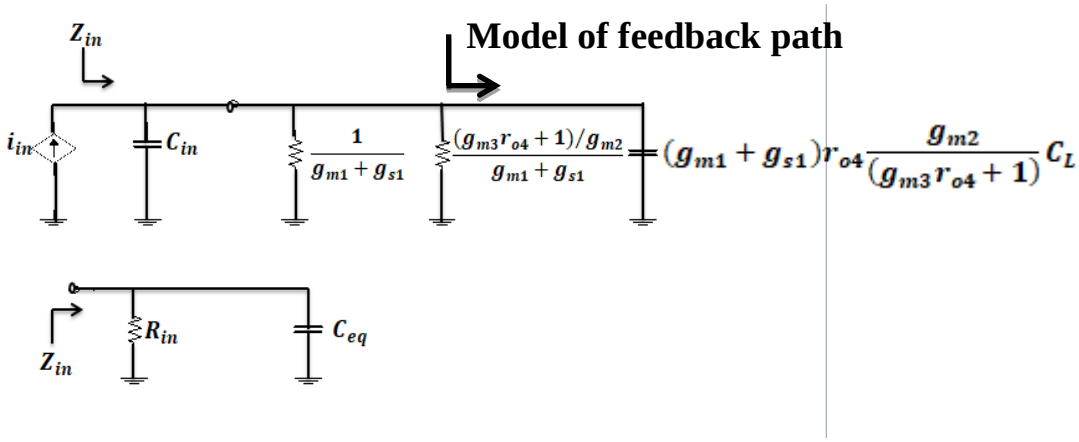

Fig. 9: Input impedance representation of the proposed TIA.
(a) Complete. (b) Lumped model.

We infer an important result from the input representation because it tells us that Resistor-Capacitor network can model the input of the TIA preamplifier, and that the pole (dominant) is simply the reversal of RC time constant given by:

$$\omega_{p1} = \frac{1}{R_{in} C_{eq}} \quad (12)$$

To find the bandwidth from equation (12), we must extract R_{in}, which represents the TIA's input resistance and is typically low, and then we must find equivalent C_{eq} for this proposed design of the circuit.

Where:

$$R_{in} = [(g_{m1} + g_{s1})\left(1 + \frac{g_{m2}}{(g_{m3} r_{o4}+1)}\right)]^{-1} \quad (13)$$

$$C_{eq} = C_{in} + (g_{m1} + g_{s1}) r_{o4} \frac{g_{m2}}{(g_{m3} r_{o4}+1)} C_L \quad (14)$$

By substituting equation (13) and (14) into equation (12) obtain:

$$\omega_{p1} = \frac{(g_{m1}+g_{s1})(1+g_{m2}/(g_{m3} r_{o4}+1)}{C_{in}+(g_{m1}+g_{s1}) C_L r_{o4} \frac{g_{m2}}{(g_{m3} r_{o4}+1)}} \quad (15)$$

We know that, bandwidth, gain and noise are important requirements for circuit design, with design pre-requisites such as supply voltage and input capacitance influencing each.

The simulated TIA came at low supply voltage (1V) with short channel 90 nm CMOS (V_{TH} : 0.1V NMOS and – 0.8V PMOS) and alongside other parameters as noted as in (Table 1). So, as shown in Fig. (10), we obtained the best results, where the transimpedance gain was 66.63 dBΩ while -3dB bandwidth was around 1.0 GHz.

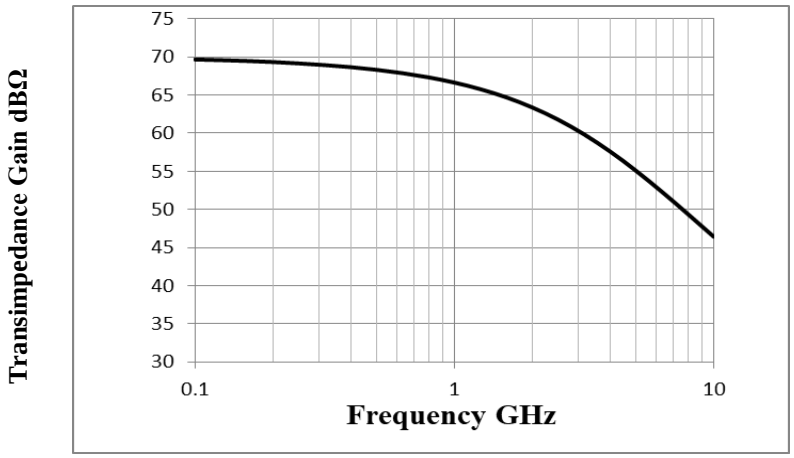

Fig. 10: Transimpedance gain of the proposed TIA

Noise Analysis

The noise characteristics of the transimpedance amplifier regarding the noise current spectral density referred to input or the corresponding reference noise current spectral density are of extreme importance for evaluating the sensitivity of the entire front-end optical receiver (Sackinger, 2005), (Vanisri and Toumazou,1995). As we know, a TIA sensitivity is constraint by its efficiency noise performance. At high TIA bandwidth, the dominant noise is the thermal noise. Fig. (11) illustrates the thermal noise sources found within the TIA with low voltage.

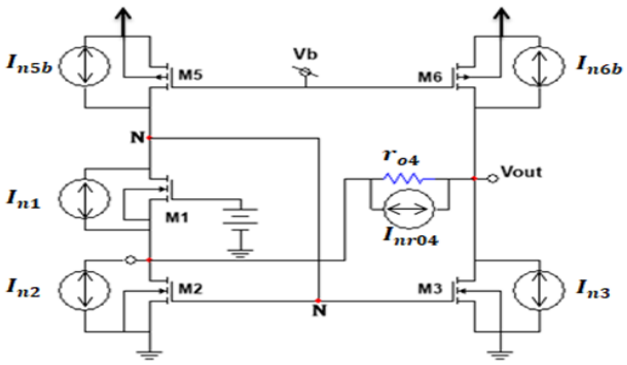

Fig. 11: Noise sources within the proposed transimpedance amplifier

This process can be achieved by transforming each noise term in the SFG back to the input node i_{scin} (Ochoa,1999). This analysis was shown in Fig. (12).

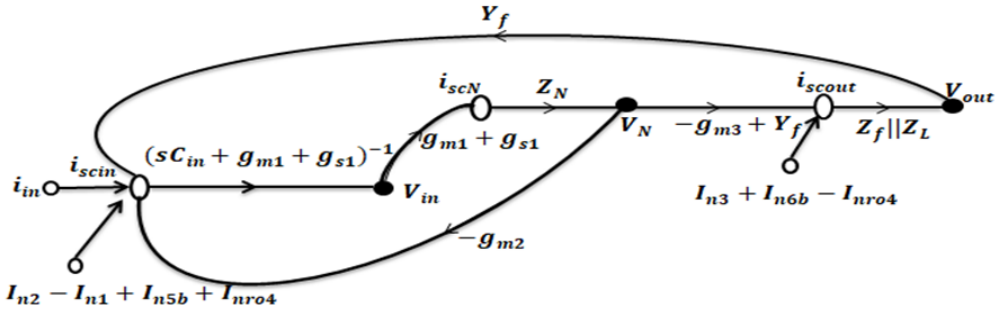

Fig. 12: Intrinsic noise sources in SFG for the transimpedance amplifier

$$I_{n1in}^2 = |\frac{1}{(sC_{in}+g_{m1}+g_{s1})^{-1}(g_{m1}+g_{s1})} - 1|^2 I_{n1}^2 \qquad (16)$$

$$= |\frac{sC_{in}}{(g_{m1}+g_{s1})}|^2 I_{n1}^2 \qquad (17)$$

Equation (17), showed that the noise fraction of I_{n1}^2 can be ignored at low frequencies where: $sC_{in} \ll (g_{m1} + g_{s1})$

An injected noise current into node **N** is equivalent to a current as if it is injected at the circuit input. This will lead to the fact that at DC, the net noise fraction of I_{n1} is zero, and effectively negligible. As a result, cascade configuration devices such as M_1 do not give out large noise at low frequencies (Buchwald,1995). Regarding I_{n2}, we see that this noise represents also input-referred, so

$$I_{n2in}^2 = I_{n2}^2$$

The noise current fraction I_{n5b}, (similar to the noise component of I_{n1}) is injected into node i_{scN}, making its contribution (*i.e* input-referred) as

$$I_{n5bin}^2 = |\frac{1}{(sC_{in}+g_{m1}+g_{s1})^{-1}}|^2 I_{n5b}^2 \qquad (18)$$

$$= |1 + \frac{sC_{in}}{(g_{m1}+g_{s1})}|^2 I_{n5b}^2 \qquad (19)$$

We note that from equation (19) for much of the passband,

$I_{n5bin}^2 \approx I_{n5b}^2$

As a consequence, noise currents entering into node **N** are effectively input-referred. This means that node **N** is from a noise perspective virtually identical to the input node.

$I_{n3} = I_{n6b}$

Finally, to calculate the TIA optical preamplifier's total input-referred noise current density, by integrating the effects of all of the individual noise components we get:

$$I_{ni}^2 = I_{n2in}^2 + I_{n5bin}^2 + I_{n3in}^2 + I_{n6bin}^2 + I_{nro4in}^2 \quad (20)$$

$$I_{ni}^2(s) = I_{n2}^2 + I_{n5b}^2 + \left|\frac{r_{o4}\, g_{ds4}\left[g_{m2} + \frac{(g_{m3}-g_{ds4})}{(g_{m1}+g_{s1})}\right]}{(-g_{m3}+g_{ds4})(1+g_{m3}/g_{m2})(1+sR_{out}C_L)}\right|^2 (I_{n3}^2 + I_{n6b}^2) + \left|\frac{r_{o4}\, g_{ds4}\left[g_{m2} + \frac{(g_{m3}-g_{ds4})}{(g_{m1}+g_{s1})}\right]}{(-g_{m3}+g_{ds4})(1+g_{m3}/g_{m2})(1+sR_{out}C_L)}\right|^2 I_{nro4}^2 \quad (21)$$

Where the constituent parameters are:

$I_{n2}^2 = \gamma 4KT g_{m2}$

$I_{n5b}^2 = \gamma 4KT g_{m5b}$

$I_{n6b}^2 = \gamma 4KT g_{m6b}$

$I_{nro4}^2 = \frac{4KT}{r_{o4}}$

Whereas K is Boltzmann's constant ($1.38\times 10^{-23} JK^{-1}$) and T is the absolute temperature in Kelvin and γ is the excess noise factor and g_m is the transconductance of the device.

By using NI Multisim 14.1 simulation and achieving the best results at the maximum gain level, the input-referred noise current density is reduced and its flatness across the passband is equal to $25.413\ \mathrm{PA/\sqrt{HZ}}$ as shown in Fig. (13).

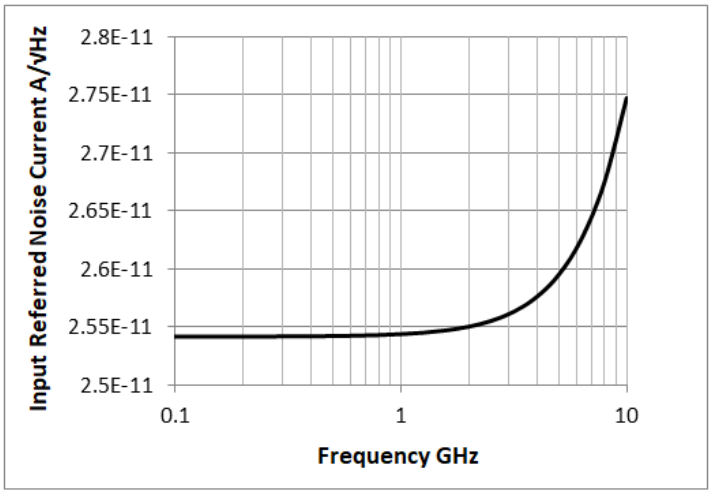

Fig. 13: Simulated input-referred noise of proposed TIA

Finally, (Table 3) illustrates the performance of the proposed (TIA). The main goal of this research is to operate the low-voltage circuit and reduce the power consumption of the proposed (TIA) circuit, and as is evident from (Table 3), the proposed (TIA) circuit topology consumes significantly less than other designs published. It is the principal goal of the proposed research.

Table 3: Performance comparison between the proposed TIA and other design works

Researchers	Technology (CMOS) nm	Supply Voltage V	Input Capacitance Pf	Gain dBΩ	Bandwidth GHz	Power Cons. mW	Input Noise pA/√Hz
(Seifouri *et al.*,2017)	0.18µm	1.8	0.3	59	7.9	18	23
(Abd-elrahman *et al.*,2016)	130	1.5	0.2	56.65	7	1.95	7.5
(Hassan and Zimmermann,2012)	40	1.1	0.5	57.5	6.6	16.4mA	20
(Zohoori *et al.*,2018)	90	1	200fF	40.5	7	1.4	20
(Phang and Johns,2001)	0.35 µm	1	1	210kΩ	50MHz	1	11
This Work 2020	**90**	**1**	**250fF**	**66.63**	**1.0**	**1.08**	**25.413**

CONCLUSION

In this paper, a new design topology is reported for the transimpedance amplifier (TIA) for use in an optical communication. A TIA with low voltage and high gain and low power consumption and low noise is designed based on the novel topology and then, the proposed design is simulated with 1V 90nm CMOS technology and with current mirror and active feedback employing CG amplifier to extend the transimpedance gain and bandwidth. The simulation results show the transimpedance gain of 66.63 dBΩ with a bandwidth of around 1.0 GHz and photodiode parasitic capacitance of 250fF. Average input-referred noise current spectral density is equal to 25.413PA/√Hz.

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اسناد مرآة التيار لمكبرات الممانعة البينية 90 nm في تطبيقات الألياف البصرية

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الملخص

عرضنا في هذا البحث تصميم جديد لمكبر الممانعة البينية (TIA) مع مرآة التيار تم توظيفها بتقنية(90 nmCMOS). الهدف والتحدي في هذا البحث هو الوصول الى استهلاك منخفض للقدرة أثناء تلبية الأداء الازمة الأخرى. تميل الدوائر المتكاملة (أشباه الموصلات ذات الأكاسيد المعدنية المتكاملة CMOS) الى أن تكون أفضل تقنية تحقق المستوى المطلوب من التكامل مع سرعة التطبيق التكلفة والربح لهذا تم استخدامها. مكبر الممانعة البينية (TIA) المقترح يتكون من مكبر الترانزستور ذو البوابة–المشتركة (CG TIA) ومرآة التيار وذلك لزيادة الربح في مكبر الممانعة البينية (TIA)، ومكبر الترانزستور ذو المصدر–المشترك (CS TIA) مع تغذية استرجاعية فعّالة (تعمل كمقاومة). بالإضافة الى ذلك، للتحقق من أداء مكبر الممانعة البينية (TIA) المقترح تم تنفيذ عملية المحاكاة للدائرة في برنامج (NI Multisim 14.1) باستخدام معاملات تقنية (90nm CMOS) وبالتالي تشير نتائج المحاكاة لمكبر الممانعة البينية (TIA) المقترح لتقنية (1V 90 nm CMOS) الى أن ربح الممانعة البينية($66.63\text{dB}\Omega$) تردد عرض نطاق الحزمة ($-3\text{dB}\Omega$)(1.0GHz) لمتسعة دخل (250fF) مرجعية ضوضاء الدخل (25.413pA/√Hz) وقيمة استهلاك القدرة (1.08mW) عند فولتية مسلطة (1V). هذا الاستهلاك المنخفض للقدرة والفولتية المسلطة هو التركيز الرئيسي لهذا العمل بالمقارنة مع المؤلفات البحثية الأخرى.

الكلمات الدالة: مكبر ذو البوابة–المشتركة (CG)، مكبر ذو المصدر- المشترك (CS)، التغذية الاسترجاعية الفعّالة.