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COMPREHENSIVE ANALYSIS OF COST FUNCTION IN QUANTUM-DOT CELLULAR AUTOMATA

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ABSTRACT

In the last five decades, the design of digital systems in nano-scale has attracted the attention of researchers. Quantum-dot Cellular Automata is a new method of binary representation at the nano level. Many circuits have been designed with this nanotechnology, most of them looking to reach optimality. QCA circuits, like other technologies, have evaluation metrics such as circuit area, delay, and cell count. Recently, an additional metric called circuit cost, has been proposed as a differentiation metric, and this evaluation metric has been introduced in various approaches. In this paper, the previous approaches of cost function are studied and evaluated, then new generalized form cost function is invented.

KEYWORDS

QCA Technology, Quantum-dot Cellular Automata, Cost function, Full adder, Nano Circuits.

1. INTRODUCTION

The researchers paid special attention to the QCA technology as it could represent the future technology of smart devices if the intimidations and challenges of this technology are eliminated. QCA technology was discovered in the early nineties of the last century by a team from the University of Notre Dame by lent et al (Lent et al, 1993). The QCA cell, which consists of four holes (dots) and two electrons, is the basic building block of this technology. The two electrons inside the cell can move from one dot to another, but they are not allowed to escape outside the cell. The movement of electrons inside the cell is governed by the electrons of neighbouring cells depending on the principle of electron repulsion. The electron tries to take the farthest possible path from the neighbouring electron, so the cell has only two polarizations, which is either -1 or +1. This property was exploited to represent binary numbers, where polarization -1 was considered a binary number 0 and polarization +1 was considered a binary number 1. After that, the team decided to build logic gates, with a majority gate built of five cells, from which the rest of the gates were reached and most of the electronic circuits were built. The QCA technology has differentiation factors that determine the capabilities of the circuits that have been built, and we can consider them criteria for evaluating the circuits, including the area of the circuit, the number of cells needed, the delay, in addition to the cost. Cost is an important metric for evaluating the circuits as it is extracted from other factors. The cost function has been put forward in several ways, each serving specific research. Researchers choose some factors that make the proposed research prominent and important, and neglects the rest of the factors, which are no less important than the chosen factors. In this research, these functions are studied and discussed, whichever comes close to comprehensiveness, to serve as a basis for future studies.

2. BACKGROUND

In QCA circuits, the quantum cell is the basic building block. Each square-shaped cell has four dots. Two electrons are injected into each cell, and these electrons have the ability to change its position, jumping between dots, eventually settling in a diagonal position due to columbic repulsion. Cell polarization is shown in Fig. 1. The two polarizations of cell P = +1 and P =-1, respectively, can represent binary digits 1 and 0. By establishing a collection of cells in an array, QCA wire and logical functions can be implemented. The binary data was sent from the input cell to the output cell using a QCA wire, as shown in Fig. 2. Because the QCA wire is made up of an array of cells, the data are transmitted toward the output cell using the electron-repulsion principle.

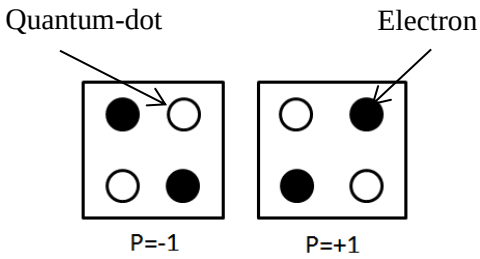


Fig 1. Cell Polarization.

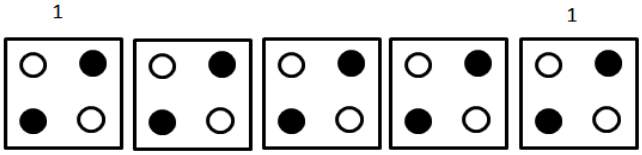


Fig 2. QCA wire

The majority gate can be used to perform the primary logic gates AND and OR by setting one of the inputs to 0 and 1, respectively. The majority gate is so important in QCA, and various researchers have focused on it, such as (Kassa and Nagaria, 2016;Labrado and Thapliyal, 2016; Bagherian Khosroshahy et al., 2017; Moaiyeri et al., 2017;Zhang et al., 2018; Deng et al., 2019; Abdullah-Al-Shafi et al., 2020; Ali Hussien et al., 2020; Majeed et al., 2022). Fig. 3 shows the majority gate configuration introduced in QCA. The majority gate functionality illustrated in Table 1. In QCA circuits, inverters with majority gates represent fundamental blocks. Two structures of inverters were introduced in QCA, as shown in Fig. 4.

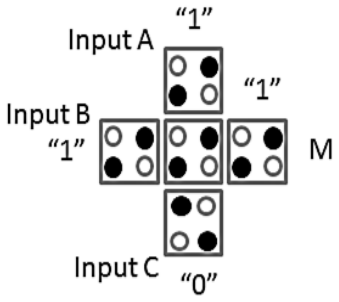


Fig 3. Majority-gate structure.

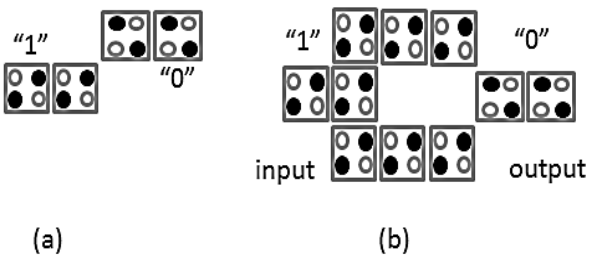


Fig 4. QCA inverter (a) corner structure (b) robust structure

Table 1: Majority gate functionality table

	A	B	C	Output
AND gate	0	0	0	0
	0	0	1	0
	0	1	1	1
	0	1	0	0
OR gate	1	1	0	1
	1	1	1	1
	1	0	1	1
	1	0	0	0

The clock is electrical signal applied to all cells to ensure data flow from the input to the output and it is also important for synchronization issues. The clocking signal controls the barriers between the dots inside the cells, which decide to allow or prevent electrons from tunnelling between dots (Majeed et al., 2021, Majeed, 2021, Frost et al., 2004). To ensure adiabatic cell switching, the clock signal has four phases (switch, hold, release and relax). As shown in Fig.5, the QCA circuit can be separated into four zones, each with four phases.

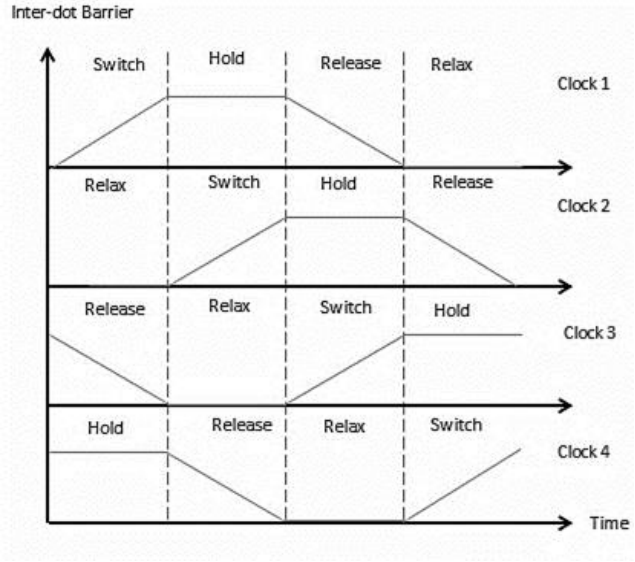


Fig 5. Clock signal in QCA technology

3. RELATED WORK

In the realm of Quantum-dot Cellular Automata (QCA) circuits, the selection of an optimal cost function is paramount and depends on the specific objectives and characteristics of the circuit under consideration. Various cost functions cater to distinct sides of QCA performance, ranging from energy dissipation and error rates to switching activity and fault tolerance metrics. The choice of the most suitable cost function is inherently tied to the priorities of the application, whether it is energy efficiency, computational accuracy, or robust fault tolerance. Notable contenders include energy dissipation for minimizing power consumption, error rates for assessing computation accuracy, and switching activity for dynamic power considerations.

Additionally, hybrid cost functions that amalgamate multiple metrics offer a comprehensive evaluation approach. The quantum-specific nature of QCA circuits introduces unique considerations, prompting the inclusion of a quantum cost function that encapsulates quantum gates and entanglement effects. The decision-making process involves a nuanced evaluation of trade-offs, scalability concerns, and application-specific goals, emphasizing the need for a judicious selection aligned with the intricacies of the QCA circuit at hand. Researchers are encouraged to explore a spectrum of cost functions, considering their applicability in optimizing QCA circuits for evolving future nanocircuits.

There are different metrics presented previously to measure the circuit quality specified for QCA forms. The first cost function (Method 1) was presented in 2011 by M. Gladshtein (Gladshtein, 2011) as detailed in Equation1.

$$\text{Circuit cost} = \text{Area} \times \text{Delay} \times \text{Power} \quad (1)$$

Although this function took the power consumption into consideration, it neglected many other important metrics. This function is considered also in (Ahmad et al., 2017).

Another method (Method 2) to calculate the circuit cost was presented in 2014 by W. Liu et al (Liu et al., 2014) as detailed in Eq. 2. This function takes four parameters into account (3-bit majority, inverter, crossover and delay). It is considered a good attempt to evaluate circuits, although it neglected many other parameters. This function was considered in (Naz et al., 2021, Majeed Ali et al., 2019).

$$\text{Circuit cost} = \left(M^k + I + C^l\right) \times T^p \quad (2)$$

where M is the number of majority gates, *I* denotes the number of inverters, *C* denotes the number of crossovers where for multilayer crossing each cross must be multiplied by 3, T denotes the circuit delay, and k, l, p denote the exponential weightings for majority gate count, crossover count, and delay, respectively.

A different method (Method 3) to calculate the cost function was proposed in 2016 by (Gladshtein, 2011) as detailed in Eq.3.

$$\text{Circuit cost} = A \times L^2 \quad (3)$$

where A is the circuit area and L is the circuit latency (delay). This equation was considered in (Song et al., 2020, Abutaleb, 2018, Wang and Xie, 2018).

The above cost functions did not cover the 5-bit majority gate. This feature was covered in 2017 by the method (Method 4) proposed by M. B Khosroshahy (Khosroshahy et al., 2017) as detailed in Eq. 4.

$$\text{Circuit cost} = [(M_3 + F \times M_5)^k + I + C^l] \times T^p \quad (4)$$

where M3 denotes the number of three-input majority gates, M5 denotes the number of five-input majority gates, and F denotes the ratio of the number of cells in the five-input majority

gate to the number of cells in the three-input majority gate. I denotes the number of inverters, C is the number of single-layer crossovers, and T denotes the circuit's delay in terms of clock phases. Furthermore, K, L, and P are the exponential weightings which equal to 2 for the circuit have same priority of parameters. This above function is considered also in (Heydari et al., 2019).

Another function (Method 5) was suggested by (Edrisi Arani and Rezai, 2018) in 2018 as detailed in Eq. 5.

$$\text{Circuit cost} = \text{Area} \times \text{Delay} \tag{5}$$

In 2019, D. Bahrepour et al (Bahrepour and Maroufi, 2019) introduces a different function (Method 6) to calculate the circuit cost as detailed in Equation 6. The complexity circuit represents the number of cells to accomplish the circuit, and Delay is the circuit latency (clock phases required to transfer cell polarization from the input cell to the output cell). This cost function was used in (Singh and Sharma, 2020, Majeed and Alkaldy, 2022).

$$\text{Circuit cost} = \text{Area} \times \text{Complexity} \times \text{Delay} \tag{6}$$

In same year H. R. Roshany et al (Roshany and Rezai, 2019) introduced another cost function (Method 7) as detailed in Eq. 7. This function is also used in (Deng et al., 2020, Maharaj and Muthurathinam, 2020).

$$\text{Circuit cost} = \text{A} \times \text{L} \tag{7}$$

where A is the circuit area and L is the latency.

In 2021, Majeed et al (Majeed and Alkaldy, 2021) introduced a deferent function (Method 8) to calculate the circuit cost. This cost includes more parameters than the above methods as detailed in Eq. 8.

$$\text{Circuit cost} = \text{CLF} \times \text{Complexity} \times \text{Area} \times \text{Delay} \tag{8}$$

where CLF is the cell and layout factor:

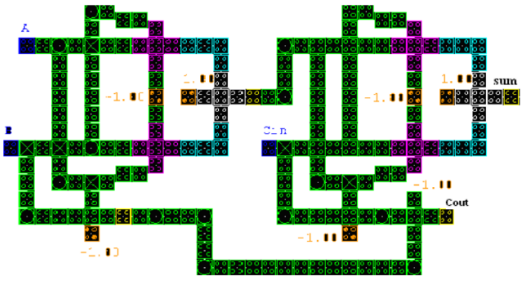
CLF = 1: for one-layer with normal cell;

= 2: for one-layer with normal and rotated cells;

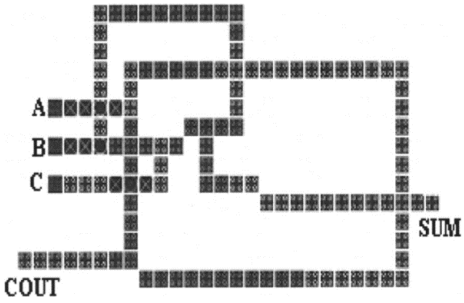
= 3: for multi-layer with normal cell;

= 4: for multi-layer with normal and rotated cells

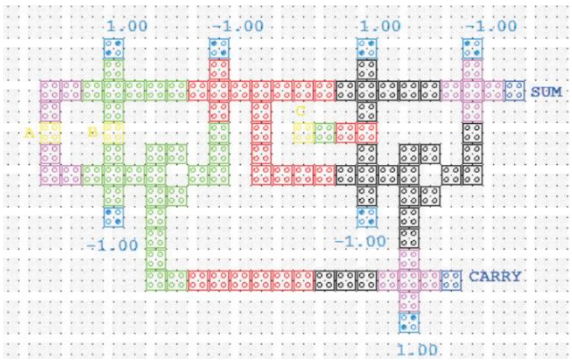
Suppose that we try to apply the above equations to specific set of QCA circuits. The full adder (FA) is taken as a benchmark circuit for different previously introduced structures of FA, as shown in Fig. 6. In this case, no two results will be similar, as depicted in Table 2 to Table 9, and this is evidence that each researcher has his own way of finding or choosing the function from among those available that suits the proposed circuit. Hence, the idea of creating a universal equation was imposed on all researchers so that its result is decisive and indisputable, bringing together all the essential standards of implementing QCA circuits.



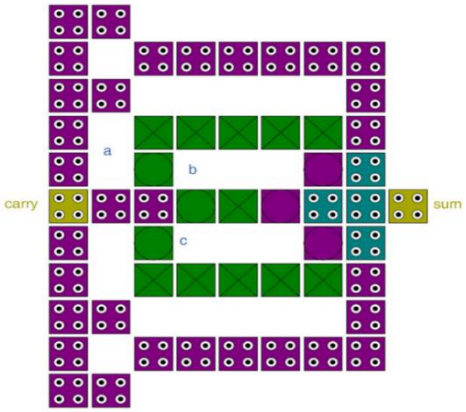
(a) (Lakshmi and Athisha, 2011)



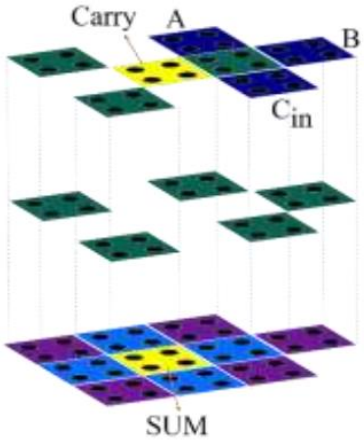
(b) (Teja et al., 2008)



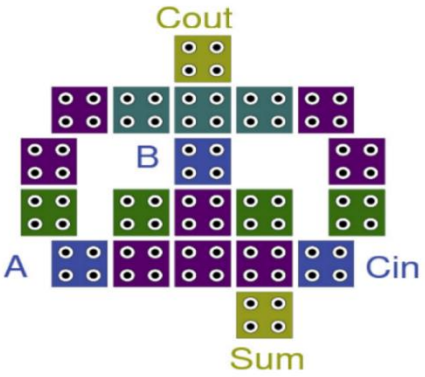
(c) (Ajitha et al., 2015)



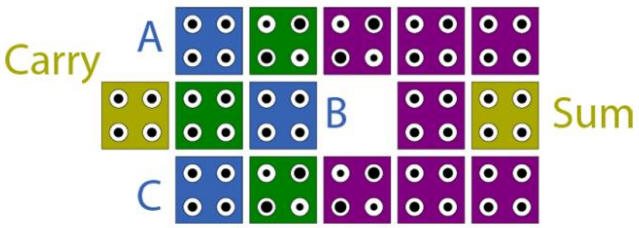
(d) (Navi et al., 2010)



(e) (Seyedi and Navimipour, 2017)



(f) (Ahmadpour et al., 2018)



(g) (Majeed and Alkaldy, 2022)

Fig. 6. Different structures of QCA-FA used to calculate the cost function in many methods

Table 2. Cost function claculation (in method 1) for many QCA-FAs

Ref	Area μm²	No. of cells	Crossover type	Number of crossings	Latency clock zone	Maj3	Maj5	Inverter	Power (meV) (1Ek)	(Cost function) $Area \times Delay \times Power$
(Lakshmi and Athisha, 2011)	0.2	192	Multilayer	5	2	9	0	4	NA	NA
(Teja et al., 2008)	0.04	124	Multilayer	3	1	3	0	3	NA	NA
(Ajitha et al., 2015)	0.14	105	Without	0	1.25	7	0	2	NA	NA
(Navi et al., 2010)	0.04	73	Multilayer	6	0.75	1	1	2	NA	NA
(Seyedi and Navimipour, 2017)	0.01	22	Multilayer	3	0.75	1	1	2	NA	NA
(Ahmadpour et al., 2018)	0.016	20	Without	0	0.75	2	0	4	31.93	0.38316
(Majeed and Alkaldy, 2022)	0.007	15	Without	0	0.5	1	0	0	36.21	0.12673

Table 3. Cost function claculation (in method 2) for many QCA-FAs

Ref	Area μm²	No. of cells	Crossover type	Number of crossings	Latency clock zone	Maj3	Maj5	Inverter	Power (meV) (1Ek)	(Cost function) $(M^k + I + C^l) \times T^p$
(Lakshmi and Athisha, 2011)	0.2	192	Multilayer	5	2	9	0	4	NA	1240
(Teja et al., 2008)	0.04	124	Multilayer	3	1	3	0	3	NA	93
(Ajitha et al., 2015)	0.14	105	Without	0	1.25	7	0	2	NA	79.687
(Navi et al., 2010)	0.04	73	Multilayer	6	0.75	1	1	2	NA	185.625
(Seyedi and Navimipour, 2017)	0.01	22	Multilayer	3	0.75	1	1	2	NA	48.937
(Ahmadpour et al., 2018)	0.016	20	Without	0	0.75	2	0	4	31.93	4.5
(Majeed and Alkaldy, 2022)	0.007	15	Without	0	0.5	1	0	0	36.21	0.25

Table 4. Cost function claculation (in method 3) for many QCA-FAs

Ref	Area μm²	No. of cells	Crossover type	Number of crossings	Latency clock zone	Maj3	Maj5	Inverter	Power (meV) (1Ek)	(Cost function) $A \times L^2$
(Lakshmi and Athisha, 2011)	0.2	192	Multilayer	5	2	9	0	4	NA	0.8
(Teja et al., 2008)	0.04	124	Multilayer	3	1	3	0	3	NA	0.04
(Ajitha et al., 2015)	0.14	105	Without	0	1.25	7	0	2	NA	0.218
(Navi et al., 2010)	0.04	73	Multilayer	6	0.75	1	1	2	NA	0.022
(Seyedi and Navimipour, 2017)	0.01	22	Multilayer	3	0.75	1	1	2	NA	0.0056
(Ahmadpour et al., 2018)	0.016	20	Without	0	0.75	2	0	4	31.93	0.009
(Majeed and Alkaldy, 2022)	0.007	15	Without	0	0.5	1	0	0	36.21	0.0017

Table 5. Cost function claculation (in method 4) for many QCA-FAs

Ref	Area μm²	No. of cells	Crossover type	Number of crossings	Latency clock zone	Maj3	Maj5	Inverter	Power (meV) (1Ek)	(Cost function) $[(M_3 + F \times M_5)^k + I + C^l] \times T^p$
(Lakshmi and Athisha, 2011)	0.2	192	Multilayer	5	2	9	0	4	NA	1240
(Teja et al., 2008)	0.04	124	Multilayer	3	1	3	0	3	NA	93
(Ajitha et al., 2015)	0.14	105	Without	0	1.25	7	0	2	NA	79.687
(Navi et al., 2010)	0.04	73	Multilayer	6	0.75	1	1	2	NA	188.437
(Seyedi and Navimipour, 2017)	0.01	22	Multilayer	3	0.75	1	1	2	NA	51.75
(Ahmadpour et al., 2018)	0.016	20	Without	0	0.75	2	0	4	31.93	4.5
(Majeed and Alkaldy, 2022)	0.007	15	Without	0	0.5	1	0	0	36.21	0.25

Table 6. Cost function claculation (in method 5) for many QCA-FAs

Ref	Area μm²	No. of cells	Crossover type	Number of crossings	Latency clock zone	Maj3	Maj5	Inverter	Power (meV) (1Ek)	(Cost function) $Area \times Delay$
(Lakshmi and Athisha, 2011)	0.2	192	Multilayer	5	2	9	0	4	NA	0.04
(Teja et al., 2008)	0.04	124	Multilayer	3	1	3	0	3	NA	0.04
(Ajitha et al., 2015)	0.14	105	Without	0	1.25	7	0	2	NA	0.175
(Navi et al., 2010)	0.04	73	Multilayer	6	0.75	1	1	2	NA	0.03
(Seyedi and Navimipour, 2017)	0.01	22	Multilayer	3	0.75	1	1	2	NA	0.0075
(Ahmadpour et al., 2018)	0.016	20	Without	0	0.75	2	0	4	31.93	0.012
(Majeed and Alkaldy, 2022)	0.007	15	Without	0	0.5	1	0	0	36.21	0.0035

Table 7. Cost function claculation (in method 6) for many QCA-FAs

Ref	Area μm^2	No. of cells	Crossover type	Number of crossings	Latency clock zone	Maj3	Maj5	Inverter	Power (meV) (1Ek)	(Cost function) $Area \times Complexity \times Delay$
(Lakshmi and Athisha, 2011)	0.2	192	Multilayer	5	2	9	0	4	NA	7.68
(Teja et al., 2008)	0.04	124	Multilayer	3	1	3	0	3	NA	4.96
(Ajitha et al., 2015)	0.14	105	Without	0	1.25	7	0	2	NA	18.375
(Navi et al., 2010)	0.04	73	Multilayer	6	0.75	1	1	2	NA	2.19
(Seyedi and Navimipour, 2017)	0.01	22	Multilayer	3	0.75	1	1	2	NA	0.165
(Ahmadpour et al., 2018)	0.016	20	Without	0	0.75	2	0	4	31.93	0.24
(Majeed and Alkaldy, 2022)	0.007	15	Without	0	0.5	1	0	0	36.21	0.0525

Table 8. Cost function claculation (in method 7) for many QCA-FAs

Ref	Area μm^2	No. of cells	Crossover type	Number of crossings	Latency clock zone	Maj3	Maj5	Inverter	Power (meV) (1Ek)	(Cost function) $Area \times Latency$
(Lakshmi and Athisha, 2011)	0.2	192	Multilayer	5	2	9	0	4	NA	0.4
(Teja et al., 2008)	0.04	124	Multilayer	3	1	3	0	3	NA	0.04
(Ajitha et al., 2015)	0.14	105	Without	0	1.25	7	0	2	NA	0.175
(Navi et al., 2010)	0.04	73	Multilayer	6	0.75	1	1	2	NA	0.03
(Seyedi and Navimipour, 2017)	0.01	22	Multilayer	3	0.75	1	1	2	NA	0.0075
(Ahmadpour et al., 2018)	0.016	20	Without	0	0.75	2	0	4	31.93	0.012
(Majeed and Alkaldy, 2022)	0.007	15	Without	0	0.5	1	0	0	36.21	0.0035

Table 9. Cost function claculation (in method 8) for many QCA-FAs

Ref	Area μm^2	No. of cells	Crossover type	Number of crossings	Latency clock zone	Maj3	Maj5	Inverter	Power (meV) 1Ek)	(Cost function) $CLF \times Complexity \times Area \times Delay$
(Lakshmi and Athisha, 2011)	0.2	192	Multilayer	5	2	9	0	4	NA	230.4
(Teja et al., 2008)	0.04	124	Multilayer	3	1	3	0	3	NA	14.88
(Ajitha et al., 2015)	0.14	105	Without	0	1.25	7	0	2	NA	18.375
(Navi et al., 2010)	0.04	73	Multilayer	6	0.75	1	1	2	NA	6.57
(Seyedi and Navimipour, 2017)	0.01	22	Multilayer	3	0.75	1	1	2	NA	0.495
(Ahmadpour et al., 2018)	0.016	20	Without	0	0.75	2	0	4	31.93	0.24
(Majeed and Alkaldy, 2022)	0.007	15	Without	0	0.5	1	0	0	36.21	0.0525

From the above eight methods, we can see that method 8 is better than the others in that it takes more parameters into consideration. But it missed Two important metrics: the level of polarization and power consumption, which are critical factors in QCA circuits. It is worth noting that circuits that do not have a high level of polarization, the signal cannot continue correctly if we want it to connect to other circuits. In other words, the signal decays as soon as one or more cells are added to the output cell. Therefore, the authors here suggest a new method to calculate the cost function as follows:

$$\text{Circuit cost} = \frac{\text{CLF}\times \text{Cell count}\times \text{Area}\times\text{Delay}\times\text{power}}{\text{PL}} \quad (9)$$

Where: CLF is the cell and layout factor:

CLF = 1: for one-layer with normal cell;

= 2: for one-layer with normal and rotated cells;

= 3: for multi-layer with normal cell;

= 4: for multi-layer with normal and rotated cells

PL: is the polarization level of the circuit.

Power: is the circuit power consumption in (meV)

The proposed method is used to calculate the cost function for the selected test bench full adder designs as shown in Table 10.

Ref	Method 1	Method 2	Method 3	Method 4	Method 5	Method 6	Method 7	Method 8	Method 9
(Lakshmi and Athisha, 2011)	NA	1240	0.8	1240	0.04	7.68	0.4	23.04	NA
(Teja et al., 2008)	NA	93	0.04	93	0.04	4.96	0.04	14.88	NA
(Ajitha et al., 2015)	NA	79.687	0.218	79.687	0.175	18.375	0.175	18.375	NA
(Navi et al., 2010)	NA	185.625	0.022	188.437	0.03	2.19	0.03	6.57	NA
(Seyedi and Navimipour, 2017)	NA	48.937	0.0056	51.75	0.0075	0.165	0.0075	0.495	NA
(Ahmadpour et al., 2018)	0.38316	4.5	0.009	4.5	0.012	0.24	0.012	0.24	1.8391
(Majeed and Alkaldy, 2022)	0.12673	0.25	0.0017	0.25	0.0035	0.0525	0.0035	0.0525	0.0998

Its clear from the above results that Fig 6-g is the best circuit since it resulted the minimum cost in all methods but if the cost function is intended to be the QCA equvelant to the CMOS PDP (Power Delay Product) the proposeed method will represent the best equivelant due to its

enclusion to the most influansing parameters in circuit performance which provides optimized matrix for the tevchnology.

4. CONCLUSION

The results of this research demonstrate the importance of cost function analysis in Quantum-dot Cellular Automata (QCA) technology and its impact on circuit performance. Using the cost metric as an additional evaluation tool makes it possible to better determine the efficiency and distinctiveness of the designed circuits. QCA offers the potential to improve the performance of digital systems at the nanoscale, and the cost function emerges as an effective criterion for optimizing circuit design and cost. This research reflects continued interest in developing QCA technology and expanding our understanding of the effects of the cost function on nanoscale digital circuit design. A better understanding of these aspects will contribute significantly to the development of more efficient and sustainable technologies in the future. The proposed cost function in this paper represents good option to inherit the CMOS PDP matric to optimize QCA nano circuits.

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